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Charge Spreading Effect of Stored Charge on Retention Characteristics in SONOS NAND Flash Memory Devices

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This research investigates the impact of charge spreading on the data retention of three-dimensional (3D) silicon-oxide-nitride-oxide-silicon (SONOS) flash memory where the charge trapping layer is shared along the cell string. In order to do so, this study conducts an electrical analysis of the planar SONOS test pattern where the silicon nitride charge storage layer is not isolated but extends beyond the gate electrode. Experimental results from the test pattern show larger retention loss in the devices with extended storage layers compared to isolated devices. This retention degradation is thought to be the result of an additional charge spreading through the extended silicon nitride layer along the width of the memory cell, which should be improved for the successful 3-D application of SONOS flash devices.

Keywords: NVM, SONOS, Retention, Charge migration

1. INTRODUCTION

The NAND flash memory market is continuously growing by the successive introduction of mass data storage applications in portable electronic devices, such as USB memories and solid state drives for tablet PCs and laptops [1]. The cell price is a key factor in the field of mass data storage application. To meet this market demand, higher bit density and lower bit cost in the memory cell must also be considered. Until now, it has been possible to reduce the bit cost and increase the bit density through the linear scaling down of the cell size, which has been achieved with the help of advanced lithography [2]. Recently, however, the NAND Flash memory industry has faced the scaling limitation of the conventional floating gate (FG) NAND cell. For a promising solution as the alternative technology to replace FG flash memory, the charge trap type flash memory, like Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) device has been focused since it provides simpler process steps than FG [3], lower cell-to-cell coupling [4], and virtual immunity to stress-induced leakage current (SILC) [5].

Nowadays, several three-dimesional (3D) flash cells such as BiCS [6], P-BiCS [7], TCAT [8], VG-NAND [9] and SMArT [10] have emerged to satisfy the memory demands for high density and low cost. Most of these devices have gate-all-around cells with the channel and charge storage layer runs along the cell string. In addition, in 3D flash cells it is evident that the SONOS gate structure has been adopted. This is because the superior vertical scalability of the SONOS structure is suitable for 3D memory. It also has other merits as previously mentioned. However, in the 3D SONOS structure, the charge trapping layer is not isolated but shared in the cell string as shown in Fig. 1; this can create the additional leakage path for the stored charge. That is, the stored carriers can migrate out from the programmed cell to the other cells. Therefore, the charge migration in the nitride layer can affect the data retention characteristics in 3D SONOS Flash memory cells. This spreading of the trapped charge has been studied as the lateral charge migration in the multi-bit NOR-type SONOS flash memory structure in particular. In this structure, the local profile of the trapped charge is important to distinguish the cell state [11,12]. How-

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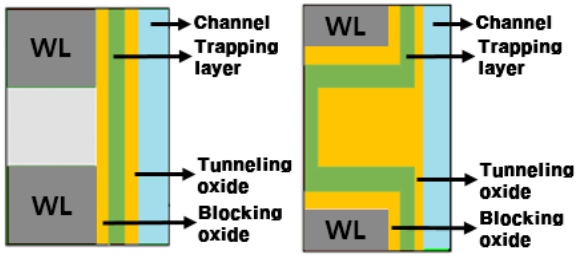

Fig. 1. The charge trapping layer structure of (a) BiCS 3D NAND and (b) TCAT 3D NAND.

ever, even in NAND flash, the intra-nitride migration can be a serious problem due to the continuous trapping layer structure in the 3D scheme.

In this study, the planar SONOS structure memory cells with various nitride extension lengths were fabricated. To analyze the retention behavior of the fabricated devices, we assume that the charge loss of the memory cell consists of the two loss components. The one component is the vertical charge loss component of the charge storage layer through the tunneling oxide or the blocking layer and the other is lateral charge migration through the extended charge storage layer along the width direction of the memory cell. In this experiment, to focus on the lateral charge migration, the vertical loss is suppressed, which is possible when the tunneling oxide and blocking oxide are of high quality and their thickness is enough to prevent the trap-assisted and/or direct tunneling during the retention mode.

2. EXPERIMENTS

To fabricate SONOS structure cells for application in non-volatile memory (NVM), the 7nm silicon dioxide (SiO_2) dielectric for tunneling oxide was thermally grown on a prime grade p-type Si substrate with high-purity oxygen gas via a dry oxidation furnace. The silicon nitride (SiN) as a charge trapping layer and the SiO_2 blocking layer were deposited by low-pressure chemical vapor deposition (LPCVD). The 4 nm, 6 nm, 8 nm SiN charge storage layer and 10 nm blocking oxide layer are considered in this study. In addition, the 100 nm titanium (Ti) electrode was adopted for the memory cells. In previous reports on the fabrication of 3D SONOS flash memory, the gate stack or ONO films are formed by a deposition method such as LPCVD [6]. It is assumed in this experiment that the charge loss mechanism can be revealed regardless of the detailed deposition methods.

In order to investigate the impact of lateral charge migration on data retention, different gate structures were fabricated using a lithography mask as shown in Fig. 2 with the device structure. The gate length and width used in this study were 100 and 100 μm, respectively. In addition, the charge-trapping layer was extended to 10 μm (Ext. 10), 25 μm (Ext. 25), 50 μm (Ext. 50), and 75 μm (Ext. 75) in every direction of gate electrode. In the case of the extended charge trapping layer, the gate etch was stopped on the blocking oxide layer while the charge trapping layer was etched self-aligned with the gate electrode area in the reference devices.

Retention was measured on fabricated capacitors using a Hewlett Packard 4284A precision LCR meter. Retention characteristics for the programmed state were obtained by monitoring the flat band voltage shift (ΔV_{FB}) with respect to its initial value and retention tests were performed at 100℃, 150℃, 200℃, and 250℃.

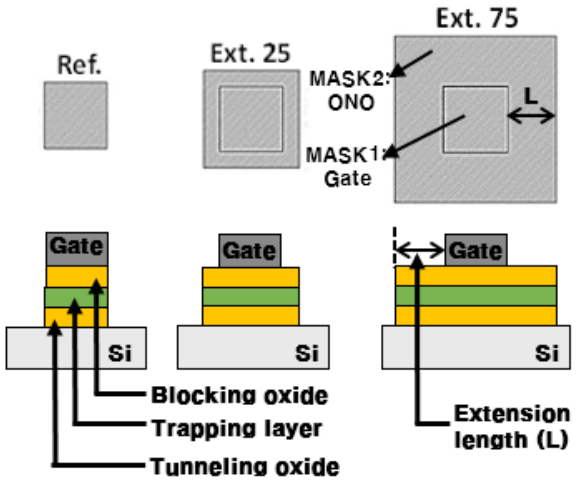

Fig. 2. Lithography mask layout to fabricate the test device with a cross-sectional view of the device. Here, Ext. 25(or 75) means the extension length of the charge-trapping layer is 25 um (or 75um). In the case of Ref., the charge-trapping layer was etched and self-aligned with the gate electrode area and extension length of 0 um.

3. RESULTS AND DISCUSSION

Figure 3 shows the program characteristics of the reference device and the device with the extended charge-trapping layer. The memory window of the fabricated devices was extracted from the flat-band voltage shift (ΔV_{FB}) after a gate voltage sweep from +30 V, +24 V, and +20 V. The different gate voltages were used to maintain the same memory window. However, devices with SiN that was 4nm-thick showed poor program characteristics and could not be matched. This is because a 4nm-thick SiN layer is so thin that it has a small charge trap site [13,14], which can also cause the large variation in the amount of ΔV_{FB}. When SiN is both 6nm and 8 nm, the devices with the extended trapping layer show a larger memory window than the reference device and ΔV_{FB} increases with the extension length. The reason for this result is thought to be due to the fringe field effect of the extended SiN devices. Furthermore, the over-etching issue can occur during the wet etching process of the gate electrode in the reference devices, which can in turn lower program efficiency.

The retention characteristics were observed to verify the effect of the stored charge lateral migration. Accelerating the loss

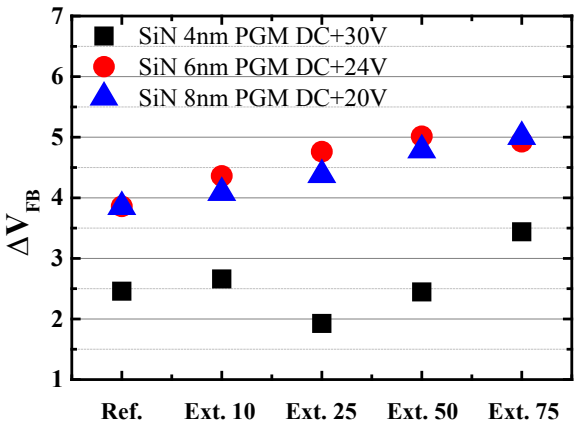

Fig. 3. Program characteristics of fabricated devices with various charge trapping layer thickness, 4/6/8 nm according to the SiN extension length.

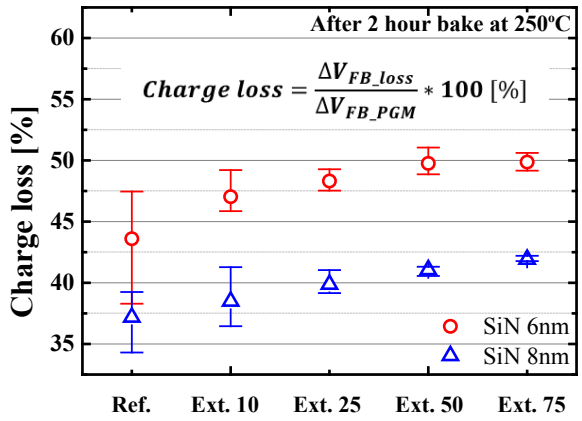

Fig. 4. The extracted percentage of charge loss from the retention characteristics on fabricated devices with various charge trapping layer thicknesses (6 nm and 8 nm).

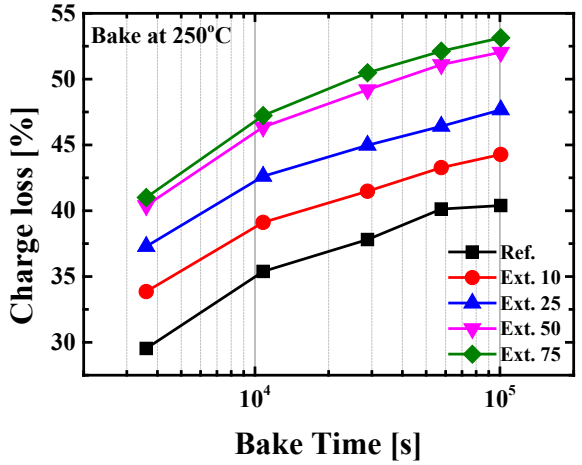

Fig. 5. The transition of charge loss on 6nm-thick SiN devices at 250℃ as a function of bake time.

of stored charge in the memory cell, the ΔV_{FB} with respect to its initial value was monitored after baking for 2 hours at 250℃. In order to compensate for the difference of the memory window between the devices, the percentage of charge loss in the fabricated devices were calculated and the result is shown in Fig. 4. The equation used to calculate the percentage of the charge loss is displayed in the inset of Fig. 4. For 4nm-thick SiN devices, the charge loss variation appears too high to be illustrated. This variation is likely due to the above mentioned lack of a charge trap site. As shown in Fig. 4, 6nm-thick SiN devices represent worse retention than 8 nm-thick SiN devices. It is considered that this different retention loss behavior could be the distance from the trapped charge and the vertical leakage path [15] even if we neglect the vertical loss. In the case of 8 nm-thick SiN devices, the discharge path is long enough and it shows less charge loss. Another explanation could be the difference in the trap energy depth in SiN according to the process condition, which affects the lateral migration/spreading speed. It is clear, however, that the extended SiN devices show the tendency that the charge loss increases as the extended SiN area increases in both SiN thicknesses. This verifies the phenomenon of the lateral migration of the trapped charge in the SiN layer.

Then, we conducted a detailed analysis on SiN 6nm-thick devices to observe long time retention behavior.

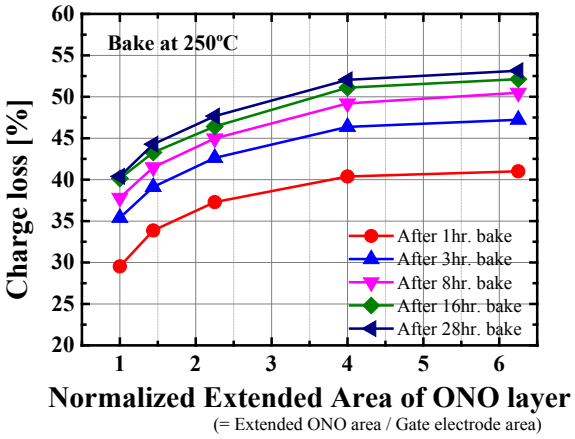

Fig. 6. Comparison of charge loss transients measured in the SiN 6nm-thick devices at 250℃ along normalized extended charge tra[[omg layer area by gate electrode area.

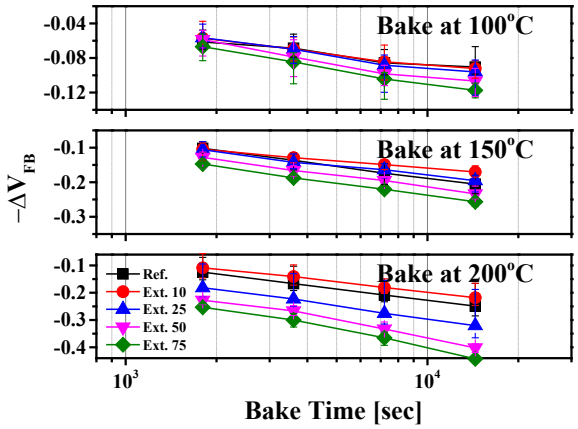

Fig. 7. Retention transients measured in SiN 6nm-thick devices at 100℃, 150℃, and 200℃.

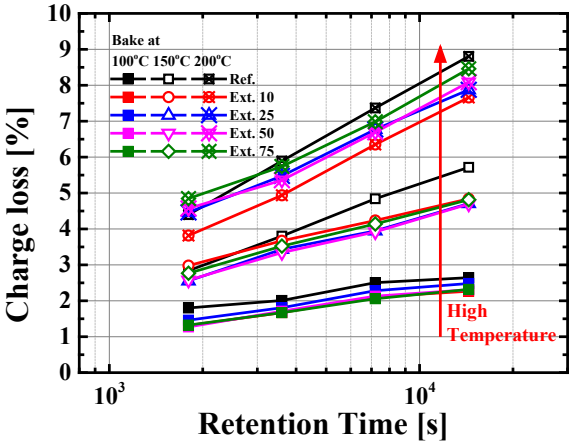

Fig. 8. The extracted percentage of charge loss from the retention transients on SiN 6nm-thick devices at 100℃, 150℃, and 200℃.

Figure 5 shows the percentage of charge loss in SiN 6 nm-thick devices at 250℃. The ΔV_{FB} with respect to its initial value was monitored for 28 hours to maximize the possibility of charge migration. At the all-sampling point, the charge loss

increases as the extended SiN area increases. Considering that leakage components in the vertical direction of the memory cell are assumed to be negligible or at least the same because of the gate electrode area, the thickness of the tunnel oxide layer and the blocking oxide layer are the same for all devices, differences in the charge loss are likely due to the lateral migration of the trapped charge in the SiN layer along the horizontal direction of the memory cell. To identify the relationship between charge loss and lateral migration of the trap charge in the SiN layer, the extended degree of the charge storage area is normalized by the area of the gate electrode. Through this, we were able to compensate for the vertical loss component that is present in all devices. Fig. 6 shows a comparison of charge loss transients measured in the 6 nm-thick SiN devices at 250℃ along a normalized value of the extended degree of the charge storage layer. The higher the normalized values, the more the loss of the charge stored in the SiN layer increases. Several researchers have reported that the stored charge can spread via the charge-trapping layer and the retention performance of charge trap memories can be affected [16-18]. Accordingly, from the result of Fig. 6, the charge loss of the stored charge in the SiN layer is likely due to the lateral migration component because the loss component in the vertical direction is ignored by normalization.

To determine the relationship between the bake temperature and the charge loss, retention transients were additionally measured at various temperatures: 100℃, 150℃, and 200℃ and the results are shown in Fig. 7. As before, the percentage of the charge loss was extracted from the retention characteristics on 6nm-thick SiN devices at 100℃, 150℃, and 200℃ and the results were compared in Fig. 8. As the temperature increases, the amount of retention loss also increases. In particular, at 200℃, the relationship between the extended area of the SiN layer and the charge loss becomes apparent, which means the horizontal movement of the stored charge in the SiN layer becomes dominant at temperatures of more than 200℃.

4. CONCLUSIONS

In this study, SONOS structure test devices were fabricated and the charge retention characteristics were investigated to analyze the impact of charge spreading in the trapping layer on the data retention. The charge loss in the programmed cell was monitored with respect to its initial value after the programmed cells were baked at an accelerated temperature. The results of the experiment reveal the effect of lateral charge migration when the SiN charge-trapping layer extends beyond the gate electrode. Apart from the vertical loss component, the additional charge losses due to the lateral migration component increase as the extended SiN layer area increases. These results should be considered in the design of 3D SONOS devices where the charge-trapping layer runs continuously along the cell string.

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