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A New Cascaded Multilevel Inverter Topology with Voltage Sources Arranged in Matrix Structure

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Abstract – The paper unleashes a new idea to arrive at reduced switch count topological structures configured in the form of a matrix for a cascaded Multi level inverter (CMLI). The theory encircles to minimize the number of switches involved in the conduction path and there from acclaim reduced input current distortion, lower switching losses and electromagnetic interference. The focus extends to standardize the number of power devices required for reaching different levels of output voltage from the same architecture. It includes appropriate pulse width modulation (PWM) strategy to generate firing pulses and ensure the desired operation of the power modules. The investigative study carries with it MATLAB based simulation and experimental results obtained using suitable prototypes to illustrate the viability of the proposed concept. The promising nature of the performance projects a new dimension in the use of single phase MLIs for renewable energy related applications.

Keywords: Cascaded multilevel inverter, Carrier PWM, Matrix structure, Reduced count topology

1. Introduction

The crunching energy imbalance emphasizes the continuing need to explore the relevance of solar and wind energy for augmenting the traditional resources of generation. The nefarious effects of green house gases along with a strong requirement for alternate sources further enforce a line of action to contemplate on the effective use of the available non- conventional recap of power.

The direction forges on the inexplicable role of converter interfaces in view of the emergence of the HVDC transmission systems for transferring the power to the load outfits. Though elaborate exercise persists in improving the operational modalities of the power electronic circuits, still efforts to enhance the efficiency of power transformation invite renewed attention.

Multilevel inverters (MLIs) expose a different embodiment of synthesizing the output voltage to suit specific application details. Their capabilities owe to cater the high power high voltage attributes without in way harming the voltage limit capability of power devices. The benefits corner to support superior power quality, lesser electro-magnetic interference, low power loss and high voltage blocking capability [1, 2].

A three level neutral point clamped inverter the first of its kind in MLI series, patented by Nabae in 1980s utilizes a series of capacitor banks to split the dc link voltages and inherits the possibility of voltage unbalance of dc-link capacitors [3]. Baker and Banister in 1975 patented a CMLI to synthesize a staircase voltage [1], which requires multi-winding transformer for each isolated H- bridges and suffers from the excess use of H- bridges for a given number of voltage levels. Maynard and Foch discovered flying capacitor MLI using floating capacitors to clamp the voltage levels that augur to pre charge the capacitors and exhibits voltage balancing problems between the capacitors [4].

A host of MLI topologies have been suggested from a combination of basic topologies [5-11] which constitute a family of cascaded 3/2 inverters and a series combination of two level inverter with five level NPC inverter named as 5/3 MLI. The growth has been registered through the use of multi-winding transformer to produce multilevel output, but accompany the drawbacks of design complexity [12, 13]. A mathematical approach has been presented in [14] to determine the minimum number of power switches or dc sources to produce a given voltage levels, the disadvantage being the need to avail power components of different voltage rating and connect inverter circuits in series.

Several asymmetrical topologies have been brought out along with a requirement for high frequency switching devices and ability to withstand overall voltage, which restricts their use for high voltage applications [15-20]. A topology based on series parallel connection of dc sources to produce higher number of levels has not been in surface due to the different rating of power components and its associated increase in the overall cost [15].

The review tales out that the major disadvantage of multilevel inversion echoes to the higher number of semiconductor devices required and explicates to trace a path for decreasing the use of power switches in each

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sequence of operation to accrue the designed level of output voltage.

The primary endeavor encompasses to evolve a single phase symmetrical CMLI topology in the form of a matrix with reverse connected voltage sources and facilitate it to synthesize different voltage levels. The proposed topology offers same number of dc sources and rectifiers for 'm' level with reduced switch count/gate drivers in comparison to cascaded MLI. It fosters to reduce the number of power devices in each current conduction path and attempt to minimize the related gate drive circuitry to enjoy efficient operation of the power circuitry. The strategy envisages the use of a general multicarrier phase disposition PWM (PDPWM) to drive the inverter and articulate on simulation and experimental evaluation procedures to extradite the new approach.

2. Proposed Topology

The main theme centers to spring up with a generalized structure for a single phase CMLI suitable to offer varying levels of output voltage. The key philosophy revolves around the arrangement of power switches in the form of an appropriate matrix model (k×j) and attaches voltage sources in the topology to replicate variable frequency variable amplitude voltage of any level.

The module seen in Fig. 1 imbibes voltage sources ($V_{1,1}$−$V_{1,n1}$), ($V_{2,1}$−$V_{2,n2}$), ($V_{k,1}$−$V_{k,nj}$) isolated from each other and connected in series to form each row of the architecture. The multiple isolated dc sources can easily be rigged through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries. The front line switches ($S_{1,1}$, $S_{1,n1+1}$) and ($S_{k+1,1}$, $S_{k+1,nj+1}$) comprise the top and bottom of the circuit and the intermediate switches ($S_{2,1}$, $S_{2,n2+1}$) and ($S_{k,1}$, $S_{k,nj+1}$) connect the voltage sources to the load. The Fig. 2 (a) shows the structure for nine levels with four isolated dc sources and only twelve switches to produce nine levels. The devices ($S_{3,1}$, $S_{2,1}$ and $S_{1,3}$) seen in Fig. 2 (b) conduct to produce ($V_{1,1}$ and $V_{1,2}$) in the output voltage. In light of the fact that the body diode in the device ($S_{1,2}$) is forward biased due to the presence of the voltage source ($V_{1,2}$), it erupts to create inter-looping problems. Therefore bidirectional devices are only appropriate in the intermediate column to protect the voltage sources from inter looping problems. The topology can be easily extended to higher voltage levels by duplicating the middle stage as represented using enclosed circle in the same figure.

The operating modes for each level seen through Figs. 3 and 7 transcend the realities in the formulation and serve to establish the niceties in the methodology. The switches $S_{3,1}$, $S_{2,1}$ and $S_{1,3}$ in Fig. 4 are switched on to produce level 2 in the output voltage. The operational pattern as observed from the Figs. 3 to 7 explain the need for only three devices to switch in all the voltage levels and the minimal switching transition during each mode transfer which can help to decrease switching power dissipation.

The arrangement treads to eliminate many of power

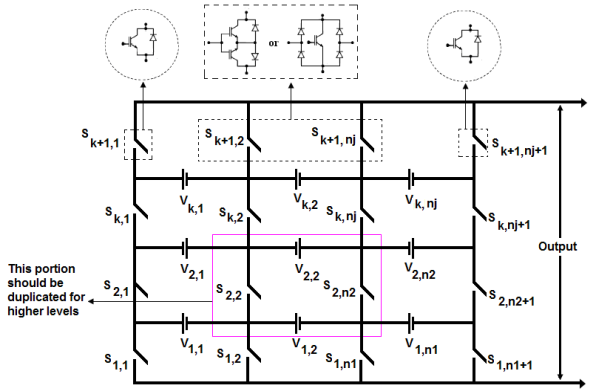


Fig. 1. Generalized topology

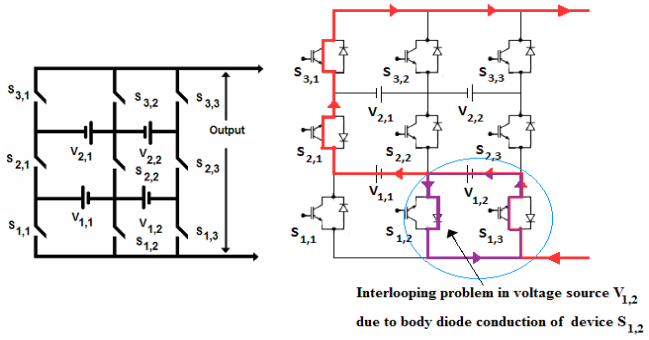


Fig. 2. Schematic of nine level inverter topology

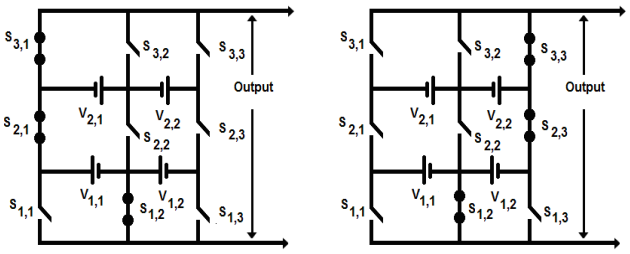


Fig. 3. Operating mode for level 1: (a) $+V_{1,1}$ (b) $-V_{1,1}$

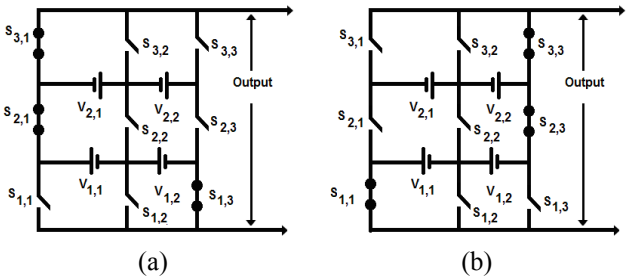
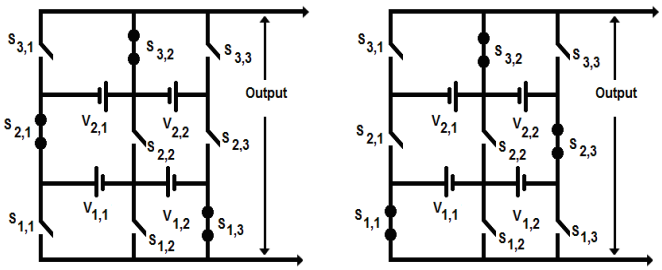
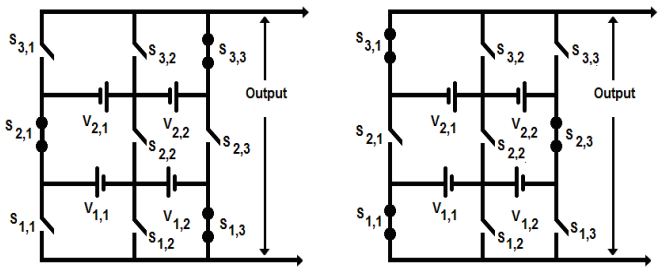


Fig. 4. Operating mode for level 2: (a) $+(V_{1,1}+V_{1,2})$ (b) $-(V_{1,1}+V_{1,2})$



(a) (b)

Fig. 5. Operating mode for level 3: (a) + ($V_{1,1}$+$V_{1,2}$+$V_{2,1}$) (b) −($V_{1,1}$+ $V_{1,2}$+ $V_{2,1}$)



(a) (b)

Fig. 6. Operating mode for level 4: (a) +($V_{1,1}$+ $V_{1,2}$+ $V_{2,1}$ + $V_{2,2}$) (b) −($V_{1,1}$+ $V_{1,2}$+ $V_{2,1}$+ $V_{2,2}$)

Table 1. PWM signal to acquire positive cycle of output voltage

PWM signals	Output level	Signals to be mapped for the devices
PWM 1	+1	$S_{1,2}$, $S_{2,1}$, $S_{3,1}$
PWM 2	+2	$S_{1,3}$, $S_{2,1}$, $S_{3,1}$
PWM 3	+3	$S_{1,3}$, $S_{2,1}$, $S_{3,2}$
PWM 4	+4	$S_{1,3}$, $S_{2,1}$, $S_{3,3}$

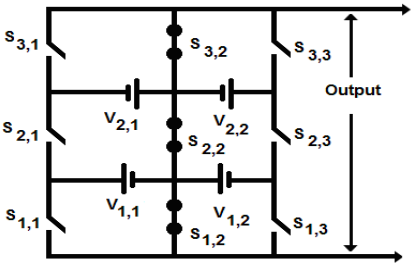


Fig. 7. Operating mode for level 0

Table 2. Power components required for proposed topology for ((2× (k×j))+1 level

Topology	Main switches	Main diodes	Gate drivers	Clamping diodes	Flying capacitors	dc-link capacitors	No. of devices in conduction path
Proposed single phase version	(2×j)×(k+1)	(2×j)×(k+1)	(k+1)×(j+1)	-	-	(k×j)	(k+1)
Proposed three phase version	(6×j)×(k+1)	(6×j)×(k+1)	3×(k+1)×(j+1)	-	-	3×(k×j)	3×(k+1)

Table 3. Power components comparison between proposed topology and conventional topologies for single phase 9 level inverter

Topologies	Main switches	Main diodes	Gate drivers	Clamping diodes	Flying capacitors	dc-link capacitors	Total
Cascaded	16	16	16	-	-	4	52
Diode clamped	16	16	16	56		4	108
Flying capacitor	16	16	16	-	28	4	80
Proposed	**12**	**12**	**9**	**-**	**-**	**4**	**37**

switches usually responsible to generate the output voltage levels in positive and negative polarities in conventional topologies. It forays the use of fewer power components in comparison to conventional topologies and requires half of the conventional carriers and two sinusoidal reference signals. It castigates the presence of redundant states and stretches it to elucidate the flexibility in the switching sequence. While a conventional nine level cascaded topology carries 16 switches and half of them traverse the current at any point in time, in the proposed structure only three switching devices portray each switching mode. Table 1 shows the PWM signals required to extract various levels of output voltage, while similar arrangements with negative reference can be used to produce PWM signals for negative cycle.

The entries in Table 2 govern the requirement of switches, dc sources, gate drive drivers and number of switches in current conduction path to achieve different levels using this new topology for single / threephase versions. The three phase topology can be derived using three single phase proposed topology connected in star network. The values in Table 3 compare the number of power components required to produce 9 level between proposed and conventional topologies to authenticate the merits of the new structure.

3. Modulation Strategy

The single phase topology requires (m-1) triangular carriers of the same amplitude and frequency and disposed horizontally in phase with each other, where, 'm' is the number of output voltage levels. The switching signals that buffer the power devices are obtained by direct comparison between triangular carriers (V_{cr1}, V_{cr2}, V_{cr3} and V_{cr4}) and the modulating reference sine (Msinωt) as indicated in Fig.

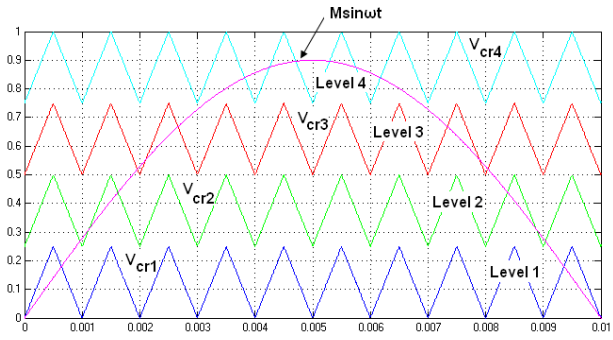


Fig. 8. Pulse width modulation phase disposition technique (PD-PWM)

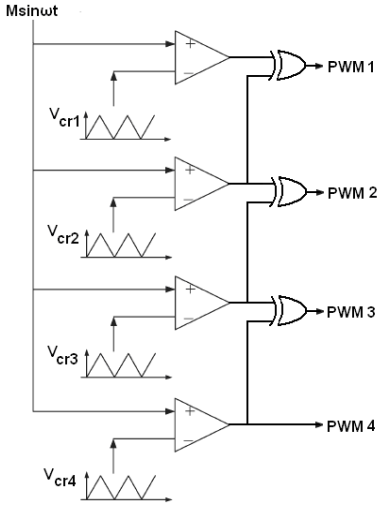


Fig. 9. Simplified Modulation scheme for single phase nine level inverter

9. The logical functions tailor the high frequency signals in order to appropriately turn on the switches used in the power circuit as shown in Fig. 2. The phase voltage amplitude can be varied by controlling the amplitude of the reference sine wave.

4. Simulation Results

The simulation parameters are chosen as $V_{1,1} = V_{1,2} = V_{2,1} = V_{2,2} = 75V$ each and a switching frequency of 2 kHz. The load components are treated to be R=150Ω and L=100 mH. The Fig. 10 shows the output voltage waveforms for five, seven and nine levels and their respective harmonic spectra obtained using the same shell input voltage. The inductive load current for single phase nine level inverter displayed in Fig. 11 traces the ripple free and distortion less nature of the output current owing to the efficacy of the structure and the modulation scheme used. The bar chart in Fig. 12 relates to the reduction in the number of switches in the conduction path for varying levels of the output voltage and throws the significance of the topology to erudite a seamless operation of CMLI for (k, j)=(2, 2).

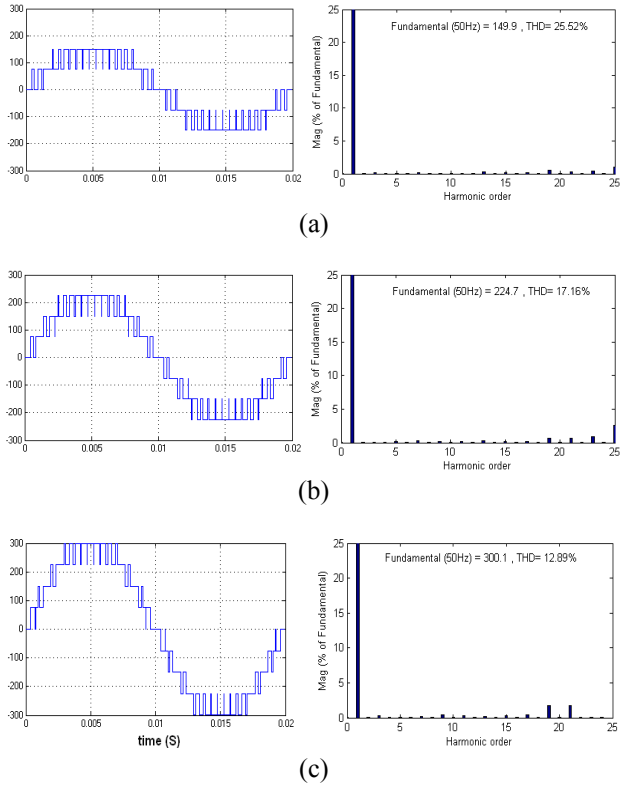


Fig. 10. Output voltage and Harmonic spectrum: (a) 5 level; (b) 7 level; (c) 9 level inverter

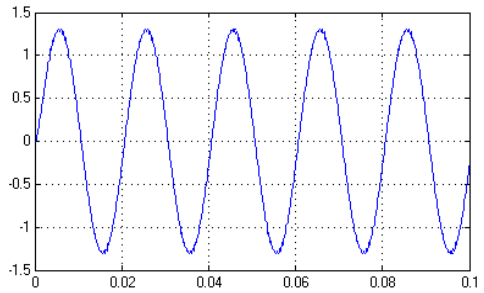


Fig. 11. Inductive load current for single phase 9 level inverter

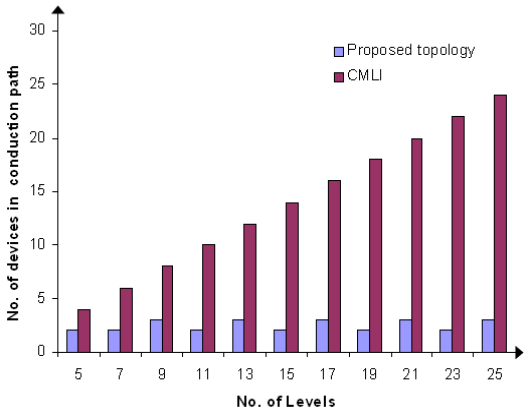


Fig. 12. Number of switches in the conduction path for varying levels

5. Experimental Results

The prototype depicted in Fig. 13 is fabricated for the same IGBTs (BUP306D) and similar load specifications to examine its applicability and validate the simulated performance. The Multicarrier phase disposition PWM (PDPWM) pulses generated through the Xilinx system generator is pictured in Fig. 14. The load voltage together with the harmonic spectrum and the load current waveforms for the nine level output corresponding to a modulation index of 1 and an output voltage of 220 V are shown in Figs. 15 and 16 respectively. The experimental results equivocally arbitrate the methodology, justify the simulated response and highlight the practical feasibility of the proposed MLI topology for use in the field.

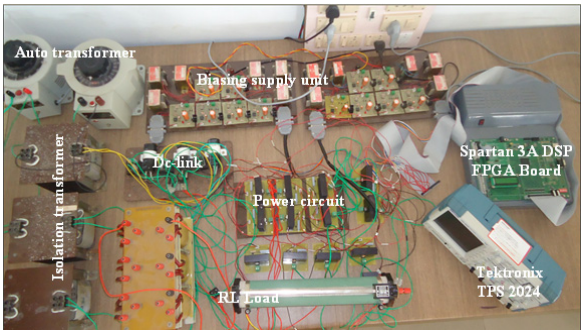


Fig. 13. Prototype of proposed single phase nine level inverter

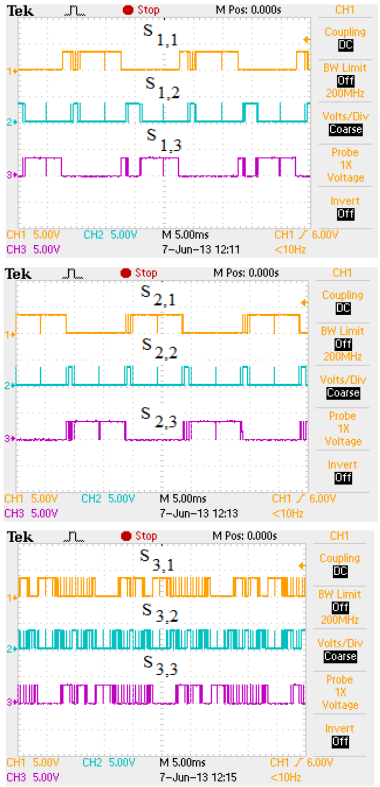


Fig. 14. Gating signals for the proposed nine level inverter

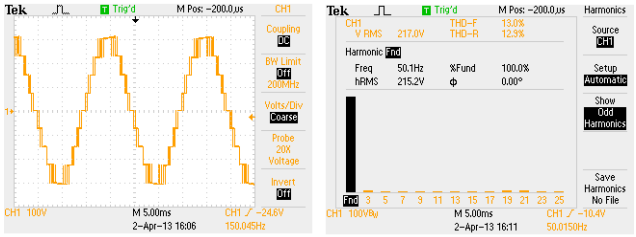


Fig. 15. Output voltage and Harmonic spectrum for nine level inverter

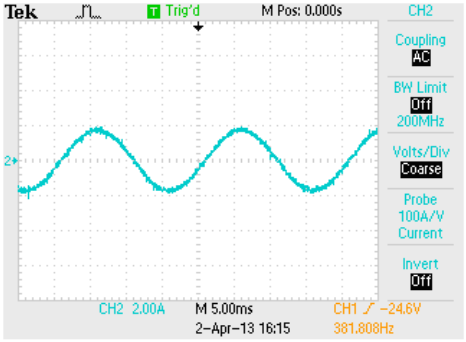


Fig. 16. Inductive load current waveform for nine level inverter

6. Conclusion

A new prodigy to emulate a matrix structure for a CMLI using isolated voltage sources or capacitors has been developed. The topology has been conceived using relatively smaller number of voltage sources and semiconductor devices compared to the existing MLI topologies. The proposed configuration has been dwelled to pull out and desired number of voltage levels from the same number of voltage sources and churn out a higher quality output voltage spectrum. The number of actual switches in operation during each conduction sequence has been drastically reduced to steam out the lowering of conduction losses and electromagnetic interference. The results castigate the reformation in the birth of newer structures and foresee an outburst of innovative applications for MLIs. The resurgence has been procrastinated to profess an increasing use of renewable sources and cater the needs of a green environment.

References

[1] R. H. Baker and L. H. Bannister, "Electric power converter," U.S. Patent, 3 867 643, Feb. 1975.

[2] R. H. Baker, "High-voltage converter circuit," U.S. Patent, 04 203 151, May 1980.

[3] A. Nabae, I. Takahashi and H. Akagi, "A new neutral-point clamped PWM inverter," in Proceeding of IAS, pp. 761-766, 1980.

[4] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage source inverters," in Proceeding of PESC, Vol. 1, pp. 397-403, 1992.
[5] M. R. Baiju, K. Gopakumar, K. K. Mohapatra, V. T. Somasekhar and L. Umannand, "A high resolution multilevel voltage space phasor generation for an open-end winding induction motor drive," European Power Electronics and Drive Journal, Vol. 13, No. 4, pp. 29-37, Sep./Oct./Nov. 2003.
[6] H. Stemmler and P. Guggenbach, "Configurations of high-power voltage source inverters drives," in Proceeding of European Conference on Power Electronics and Applications, Vol. 5, pp. 7-14, 1993.
[7] K. A. Corzine, M. W. Wielebski, F. Z. Peng and J. Wang, "Control of cascaded multi-level inverters," IEEE Trans. Power Electron., Vol. 19, No. 3, pp. 732-738, May 2004.
[8] C. Rech and J. R. Pinheiro, "Hybrid multilevel converters: Unified analysis and design considerations," IEEE Trans. Ind. Electron., Vol. 54, No. 2, pp. 1092-1104, Apr. 2007.
[9] J. Rodriguez, J. Lai and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., Vol. 49, No. 4, pp. 724-738, Aug. 2002.
[10] M. Manjrekar, P. K. Steimer and T. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," IEEE Trans. Ind. Appl., Vol. 36, No. 3, pp. 834-841, May/Jun. 2000.
[11] Z. Du, L. M. Tolbert, J. N. Chiasson and B. Ozpineci, "A cascade multilevel inverter using a single dc power source," in Proceeding of APEC, pp. 426-430, 2006.
[12] R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, and P. N. Enjeti, "Multilevel inverter by cascading industrial VSI," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 832-838, Aug. 2002.
[13] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, "A comparative analysis between the symmetric and the hybrid asymmetric nine-level series connected H-bridge cells inverter," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1-10.
[14] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. T. Haque, and M. Sabahi, "Reduction of DC voltage sources and switches in asymmetrical multilevel converters using a novel topology," *J. Elect. Power Syst.Res.*, vol. 77, no. 8, pp. 1073-1085, Jun. 2007.
[15] Ramkumar S, Kamaraj V, Thamizharasan S, Jeevananthan S," A new series parallel switched multilevel dc-link inverter topology", Int J Electr Power and Energy Syst, Vol. 36, Pg: 93-99, 2012.
[16] E. Beser, B. Arifoglu, S. Camur, and E. K. Beser, "Design and application of a single phase multilevel inverter suitable for using as a voltage harmonic source," *J. Power Electron.*, vol. 10, no. 2, pp. 138-145, Mar. 2010.
[17] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, "A new simplified multilevel inverter topology for dc-ac conversion," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1311-1319, Sep. 2006.
[18] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2435-2443, Jun. 2011.
[19] J. Selvaraj and N. A. Rahim, "Multilevel inverter for grid-connected PV system employing digital PI controller," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 149-158, Jan. 2009.
[20] Sung Geun Song, Feel Soon Kang and Sung-Jun Park, "Cascaded multilevel inverter employing three phase transformers and single dc input" *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2005-2014, June. 2009.

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