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Novel Low-Volume Solder-on-Pad Process for Fine Pitch Cu Pillar Bump Interconnection

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Abstract: Novel low-volume solder-on-pad (SoP) process is proposed for a fine pitch Cu pillar bump interconnection. A novel solder bumping material (SBM) has been developed for the 60 μm pitch SoP using screen printing process. SBM, which is composed of ternary Sn-3.0Ag-0.5Cu (SAC305) solder powder and a polymer resin, is a paste material to perform a fine-pitch SoP in place of the electroplating process. By optimizing the volumetric ratio of the resin, deoxidizing agent, and SAC305 solder powder; the oxide layers on the solder powder and Cu pads are successfully removed during the bumping process without additional treatment or equipment. The Si chip and substrate with daisy-chain pattern are fabricated to develop the fine pitch SoP process and evaluate the fine-pitch interconnection. The fabricated Si substrate has 6724 under bump metallization (UBM) with a 45 μm diameter and 60 μm pitch. The Si chip with Cu pillar bump is flip chip bonded with the SoP formed substrate using an underfill material with fluxing features. Using the fluxing underfill material is advantageous since it eliminates the flux cleaning process and capillary flow process of underfill. The optimized interconnection process has been validated by the electrical characterization of the daisy-chain pattern. This work is the first report on a successful operation of a fine-pitch SoP and micro bump interconnection using a screen printing process.

Keywords: solder-on-pad, fine pitch bumping, micro bump interconnection

1. Introduction

For high performance electronic products, more dense integration and short interconnection is required. To obtain the high-density I/Os and low signal loss, 3D die interconnection is a key technology. More dense integration and increasing number of IOs implies scaling down the micro bump dimension and pitch. Tight control for the performing process of micro bump and stacking accuracy are required. Several methods for interconnection micro bumps with a fine pitch have attempted, such as Cu(Ni)Sn Cu pillar with solder cap, Cu-Cu direct bonding and Transient liquid phase (TLP) CuSn bump.[1-6] Direct Cu-Cu bonding is needed relatively high bonding temperature and pressure in spite of high throughput.[3] Transient liquid phase (TLP) CuSn bonding is a promising process for low temperature thermo-compression bonding process that transforms solder into high melting point intermetallic (IMC) bonds.[4]

In view of obtaining high reliable micro bump, Cu pillar with solder cap using electro plating or electroless plating method is commonly used. The electroplating process for micro bump, it is very hard to obtain SAC305 solder cap. Therefore, cost-effective SAC305 SoP process using the screen printing is very attractive. Solder cap process is performed on the Cu pillar bump. The presented SoP is formed on the under bump metallization (UBM) layer in substrate.

Also, flux and underfill materials are the most critical components for a reliable flip-chip bonding process using micro bumps. For flux-applying process, however, cleaning of flux residue is another issue after flip-chip bonding process. The flux residue is unfavorable for following underfill dispensing process, and can further make a long-term reliability issue. Therefore, the development of flip-chip bonding process without the usage of flux for the joining of micro bumps is required.

In this paper, the developed fine pitch SoP process and interconnection process for fine pitch micro bump is newly presented. This fine pitch SAC305 SoP process is developed using a maskless screen printing.

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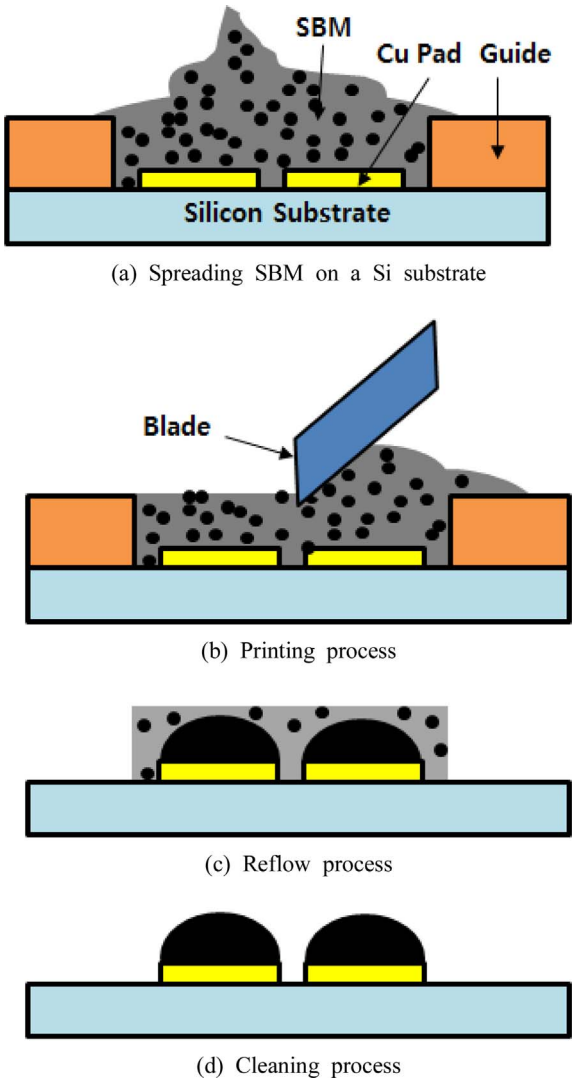
2. Fine Pitch SoP Process

Since the micro bump interconnection needs fine pitch and low-volume solder bump, a novel maskless solder bump maker (SBM) is developed.[7-13] The SBM, which is composed of solder powder and polymer resin, is the material that pastes or binds the solder bump on a given substrate. Particularly, the polymer resin for the SBM has the function of removing oxide layers existing on the surface of the solder powder and Cu pad during the bumping process. In this work, Sn-3.0Ag-0.5Cu (SAC305) powdered solder is blended with the resin. The specification of the distribution of the solder diameters for type 7 and type 8 are according to the standard:[14] 2 μm to 11 μm and 2 μm to 8 μm with weight percentages of 90% for type 7 and type 8, respectively.

The type 8 solder powder is newly adopted. From the previous results, the type 7 solder powder is usually used because the minimum bump pitch is over than 130 μm.[10-12] Using numerical estimation, the number of solder particles placed on the Cu pad area is calculated. When type 7 solder powder is used, 48 solder particles can be placed on a Cu pad with diameter of 45 μm. Similarly, for type 8, 81 solder particles can be placed on the same pad area.

The volumetric mixing ratio between the polymer resin and the SAC305 solder powder is 86:14. The mixing ratio is analyzed to establish a proper interaction between the solder powder and the Cu pads, and optimized fully to fill the Cu pads. Figure 1 shows the whole bumping process for the fine pitch SoP process. SBM material is printed on the Si substrate, and printed area and thickness is controlled by a guide. This guide is not a patterned mask, as opposed to a photoresist mask or a metal mask which defines the open areas or separates the micro bumps. The reflow process is performed at 270°C for 40 sec. in an IR oven. After reflow process, the residue and solder particles are cleaned off in ultrasonic baths of MIF, acetone, and methanol for several minutes. While previous works required processes such as a second resin printing, cleaning, and coining, this proposed SoP process does not require such processes.[10,11]

The test vehicles are fabricated to develop the fine pitch SoP process using SBM material and screen printing process. For its demonstration, Si chip and substrate are fabricated with a daisy-chain pattern. The 7 mm × 7 mm Si chip is fabricated with 6724 Cu pillars, which have a pitch of 60 μm. The used Cu pillars have the diameter of 45 μm and the height of 30 μm, as shown in Fig. 2(a). Moreover Si substrate having the same number of Cu pads is also fabricated to form the 60 μm pitch SoP, as shown in Fig. 2(b). The used Cu pads have a 5 μm TiW/Cu under bump met-



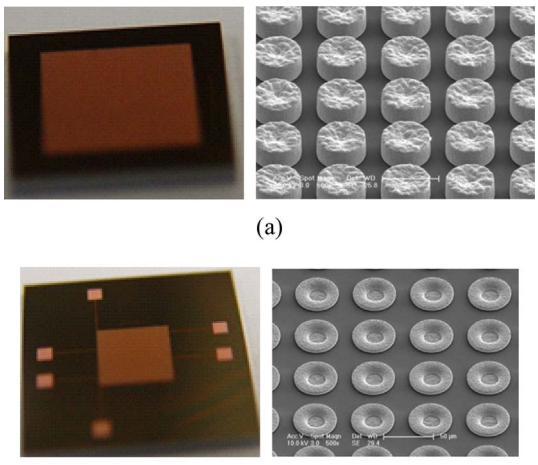
(a) Spreading SBM on a Si substrate

(b) Printing process

(c) Reflow process

(d) Cleaning process

Fig. 1. Process flow of fine pitch SoP using screen printing.



(a)

(b)

Fig. 2. Photograph and SEM images of daisy-chain test vehicle: (a) fabricated Si chip with Cu pillars, and (b) fabricated Si substrate with UBM.

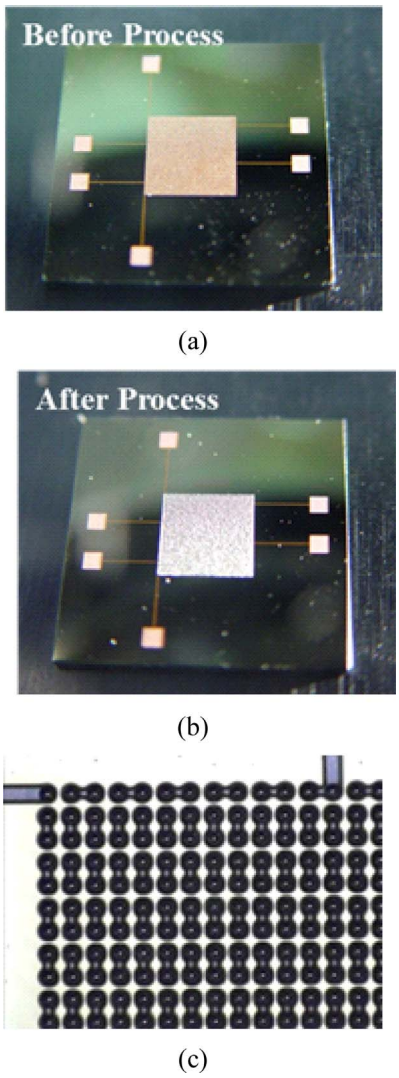


Fig. 3. Optical images of fabricated Si substrates: (a) before, (b) after SoP forming process and (c) magnification of (b).

allization (UBM) layer, which has a diameter of 45 μm.

The optical images of the fabricated Si substrate are shown in Fig. 3. The size of the used Si substrate is 15 mm × 15 mm. The fabricated Si substrate after SoP process is covered with SAC305 solder bumps as shown in Fig. 3(b). No solder bridges which are easily formed by maskless printing process are found in the Fig. 3(c). From the scanning electron microscope (SEM) image of the formed fine pitch SoP array, the 60 μm pitch SoPs are well formed on the UBM layers with uniform shapes. Also, all 6724 Cu pads are fully filled without any missing bumps, as shown in Fig. 4.

3. Fine Pitch Interconnection Process

The test vehicles are flip-chip bonded, and the bonding process flow is very simple. To begin with, a developed

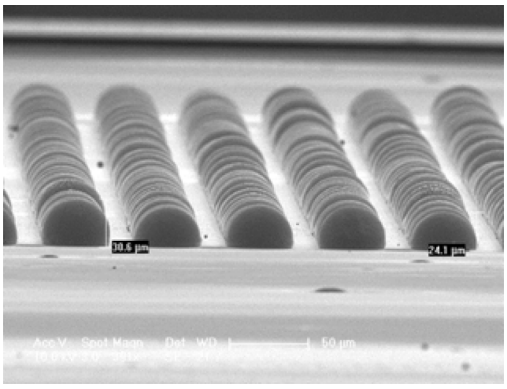


Fig. 4. SEM image of fully formed SAC SoPs on the 6724 Cu pads.

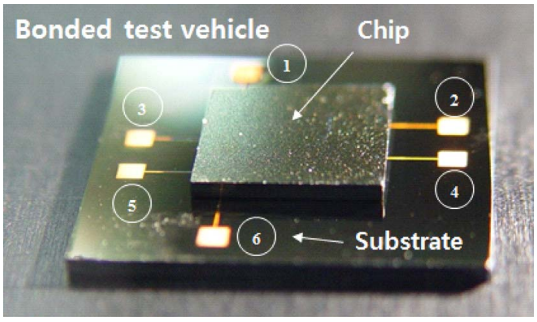
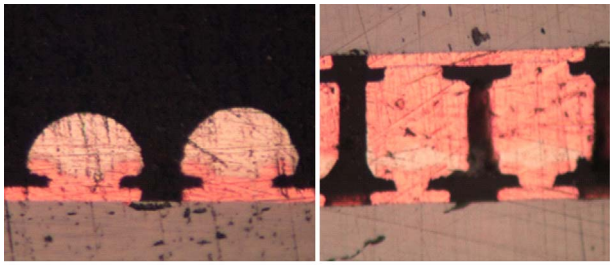


Fig. 5. Photograph of flip-chip bonded test vehicle.

fluxing underfill, which does not need a clean step, is applied to the Si substrate. The fluxing underfill material has the fluxing and the capillary underfill features.[15-17] In this material, deoxidizing agents together with a hardener are added to the underfill to form an epoxy-based thermoset. Then the Si chip with the Cu pillar bumps is aligned to the Si substrate with SoPs, and the solder joints are all formed simultaneously using the thermo-compressing bonding. During the flip chip bonding, additional flux cleaning and capillary action are not required. The optimized bumping and interconnection processes have been validated by an electrical characterization of the daisy-chain patterned test vehicles. Figure 5 shows the photograph of the flip-chip bonded test vehicle. Different bonding conditions (bonding temperature, time, and pressure) are examined to achieve the best joining result. The fabricated Si chip and substrate are well bonded with the developed fluxing underfill material. First, fluxing underfill is dispensed onto the Si substrate and preheated at 120°C for 10 seconds. Next, the pressure of 200 gf is applied onto the joint while the temperature is set to 250°C for 20 seconds.

The fine pitch interconnection between Cu pillars and SoP is checked using two quick analysis methods. One is the cross-section inspection of the bonded chip and substrate, as shown in Figs. 6(a) and 6(b). Figures 6(a) and



(a) (b)

Fig. 6. Cross-sectional images of the Si substrate: (a) before and (b) after flip chip bonding process.

6(b) show the cross-sectional views of the SoP and Cu pillar interconnections before and after the bonding process. From the cross-section inspection, the bump shape and height information of SoP obtained through an SEM virtual inspection are verified. Cu pillars and SoP are properly interconnected without an alignment issue. Electrical defects commonly occur in fine pitch bonding when the adjacent bumps make an electrical short effect or when an insufficient volume of solder creates an electrical opening effect. However, no such electrical defects are found in these fine pitch Cu pillar bump interconnections. The other method used to check the fine pitch interconnection is to compare the calculated and measured resistance values of the test vehicles with the daisy chain patterns, as shown in Figs. The measured DC resistance values are compared with the calculated resistances of the test vehicles with the daisy-chain patterns, as shown in Fig. 5 and 7. The bonded test vehicles are designed to connect all of the bumps and have six DC probing pads. In detail, total 6724 bump interconnection is checked by probing top pad and bottom pad, marked as number 1 and 6 respectively. The right and left pads are designed to inspect the internal bump open and short effects. If the test vehicles are well bonded, the DC resistance values will show an increasing tendency as the section goes from 1-2 to 1-6.

The simple DC resistance values can be calculated with Eq. (1)

$$R_{TOTAL} = \rho \times \frac{L}{A} \tag{1}$$

Here R_{TOTAL} is total sum of the resistance values, ρ is resistivity of metal and solder, L is length and A is cross-sectional area. The resistance values of redistribution layer (RDL) of Si chip, the interconnection bumps between the chip and substrate, and the RDL of Si substrate are included in R_{TOTAL}. Values L and A respectively represent the length and area of all the interconnection paths. The calculated and measured DC resistances values of the test

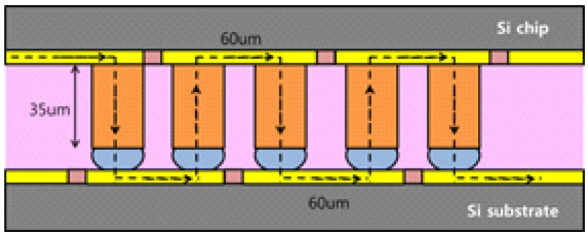


Fig. 7. Schematic of DC resistance calculation of daisy-chain patterned test vehicles.

Table 1. Comparison of DC resistance values between calculated results and measured data

Section	Measured Resistance (Ω)	Total measured resistance (Ω)	Total calculated resistance (Ω)
1-2	6		
1-3	17.3		
1-4	24.6	36.8	32.3
1-5	31.1		
1-6	36.8		

vehicle, reflecting 6,724 bump interconnections, are summarized in Table 1. From the comparison results, it is obviously proved that the interconnection of Cu pillars and SoPs is successful. This measured DC resistance values have some variations of contact resistance.

4. Conclusion

A fine pitch solder-on-pad process using a screen printing process was newly presented and successfully developed by optimizing the volumetric mixing ratio between resin and Sn-3.0Ag-0.5Cu solder powder. The test vehicles with daisy-chain pattern were fabricated to evaluate the presented SoP technology and the simple interconnection process using a fluxing underfill material. From SEM images and the DC resistance measurement data, presented bumping technology and fine pitch micro bump interconnection were verified. Therefore, because of the simplicity and cost-effectiveness of the process, the developed SoP technology can be used instead of solder cap process with electroplating.

Acknowledgements

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