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체내 이식 기기용 표준 CMOS 고전압 신경 자극 집적 회로

(A High-Voltage Compliant Neural Stimulation IC for Implant Devices Using Standard CMOS Process)

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요 약

본 논문에서는 신경 관련 인공 전자기기를 위한 신경 자극 집적회로를 0.18-μm 표준 CMOS 반도체 공정을 이용하여 설계하였다. 제안 된 신경 자극 회로는 12.8-V 전원을 사용하면서 10-kΩ의 부하에 최대 1 mA의 전류까지 전달이 가능하다. 표준 CMOS 공정 기술로 구현을 위해서 저전압 트랜지스터만을 이용하여 설계를 하였고, 고전압에서의 안정적인 동작을 위하여 트랜지스터 스태킹 기술을 적용하였다. 또한, 신경 자극 동작 후 전하 잔여량이 남아 있지 않도록 active charge balancing회로를 포함하였다. 제안 된 단일 채널 자극 집적회로의 경우 디지털-아날로그 변환기, 전류 출력 드라이버, 레벨 시프터, 디지털 제어 부분, 그리고 active charge balancing 회로까지 모두 포함하여 전체 칩 레이아웃 면적은 0.13 mm^2 을 차지하며, 다중 채널 방식의 신경 자극 기능의 체내 이식용 인공 전자기기 시스템에 적용을 하는데 적합하다.

Abstract

This paper presents the design of an implantable stimulation IC intended for neural prosthetic devices using 0.18-μm standard CMOS technology. The proposed single-channel biphasic current stimulator prototype is designed to deliver up to 1 mA of current to the tissue-equivalent 10-kΩ load using 12.8-V supply voltage. To utilize only low-voltage standard CMOS transistors in the design, transistor stacking with dynamic gate biasing technique is used for reliable operation at high-voltage. In addition, active charge balancing circuit is used to maintain zero net charge at the stimulation site over the complete stimulation cycle. The area of the total stimulator IC consisting of DAC, current stimulation output driver, level-shifters, digital logic, and active charge balancer is 0.13 mm^2 and is suitable to be applied for multi-channel neural prosthetic devices.

Keywords : neural stimulation, active charge balancing, transistor stacking, dynamic biasing, high-voltage

Ⅰ. Introduction

CMOS-based neural stimulation systems are widely being developed to be utilized in various implantable biomedical applications[1] such as in neural prosthetic devices to restore limb movement, in retinal implants to help restore vision in patients with sight impairment[2~4], and also for deep brain stimulation (DBS) purpose for patients with epilepsy.

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The basic idea of a neural stimulator is to excite the degenerated or damaged neuron in critical parts inside the brain or body by delivering and recovering controlled amount of electric charge to initiate action potential as a response and thereby recover its biological functionalities[1]. Among some of the major issues in realizing a stimulator IC such as safety, charge balance, type of stimulation waveform, low power consumption, number of channels, and small area, the high impedance level of the electrode/tissue interface require most of the existing stimulation ICs [1~4] to operate at high-voltage (HV) supplies in order to provide sufficient level of output current pulses to the stimulation site. To meet the requirement for HV compliance, special HV CMOS processes[2~4] are utilized for reliable operation despite sacrificing die area, cost, and turnaround time.

In this paper, a single-channel biphasic stimulator IC prototype using standard 0.18-μm CMOS process is proposed which may be applied for various implantable applications. Transistor stacking technique with dynamic gate biasing[5] is applied to the output driver circuit to facilitate HV operation without any reliability issues. To enable accurate charge delivery to and recovery from the stimulation site, active charge balancing circuit is included in the proposed stimulation IC. In addition, considering its application for multi-channel microsystems for implant devices, the design is done with careful attention to achieve small area for high integration as well as low-power consumption.

Section Ⅱ discusses the design considerations and overall system architecture while Section Ⅲ presents the key circuit design details. Section Ⅳ shows the simulation results of the proposed stimulation IC followed by the conclusions in Section Ⅴ.

Ⅱ. System Architecture

1. Design considerations

There are several factors that need to be taken into account when designing an implantable stimulation device. The primary stimulation parameters are amplitude, pulse-width, and stimulation rate. The magnitude of the stimulation current should exceed a threshold that leads to the occurrence of action potentials. Different applications require different current amplitudes for excitation. In this work, the proposed stimulator can provide output current in the range of 32 μA up to 1 mA which is sufficient to cover various neural stimulation applications. Figure 1 shows the timing diagram for current stimulation and charge balancing. The stimulation pulse width in the design is set to 100 μs while the rate is set as 400 μs. After stimulation phase, active charge balancing phase takes place within the 50 μs timing window. In addition to the design parameters, the device should consume low power and small area considering multi-channel implementation.

Figure 2 shows the simplified electrode and tissue interface model used in the design. The parameter values much depend on the electrode size and material[3]. In this work, an electrode model with R_E=10 MΩ, C_E=100 nF, and tissue resistance of 10 kΩ

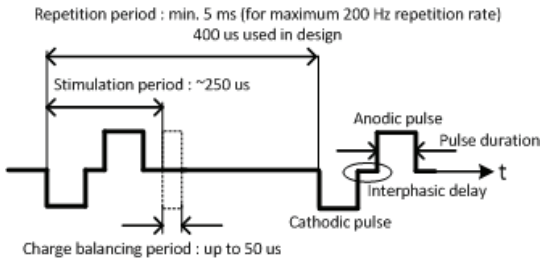


그림 1. 전류 자극 및 charge balancing 타이밍도
Fig. 1. Timing diagram of current stimulation and charge balancing.

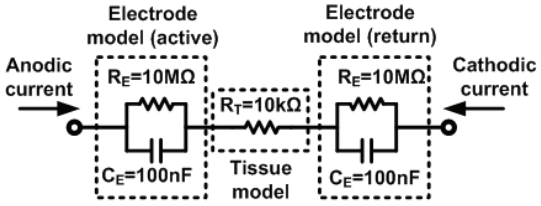


그림 2. Electrode-tissue 등가 모델
Fig. 2. Equivalent model of electrode-tissue interface.

values are assumed[3].

In order to deliver 1 mA of current to a 10-kΩ load, at least 10 V voltage compliance is needed. Common approaches to achieve this while maintaining reliability is by using special HV processes. However, HV transistor has several disadvantages such as high process cost, large drain resistance which lead to large transistor area and poor transistor matching[6]. In order to avoid these issues, only 1.8-V and 3.3-V standard CMOS transistors are used in the overall design of the proposed stimulator IC.

In the process of neural stimulation, it is important that no residual charge is left in the stimulation site to prevent any tissue damage. Considering the fact that mismatch in the biphasic pulse can occur during the stimulation process, the output driver is designed to have high linearity to deliver a balanced biphasic pulse. In addition, an active charge balancing circuit is used to minimize any charge error after each simulation cycle.

2. Overall Architecture

Figure 3 shows the architecture of proposed neural stimulator. The building blocks are comprised of digital control logic, level shifters, digital-to-analog converter (DAC), output driver and charge balancing circuit. The digital control logic is used to control stimulation parameters that includes output current amplitude, polarity, duration, and feedback from electrode after stimulation for charge balancing.

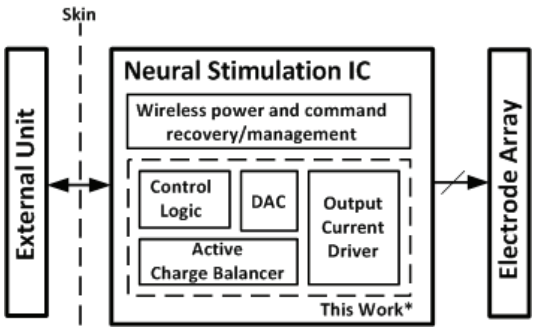


그림 3. 신경 자극 집적 회로의 전체 구조 블록도
Fig. 3. Block diagram of overall neural stimulation IC.

The DAC operates with signals swinging between 0 and 3.2 V, and the output driver requires both 0-3.2 V and 9.6-12.8 V swinging signals for operation. Thus, one level-shifter is needed to convert 1.8-Vpp signal to 3.2-Vpp, and then a second level-shifter is utilized to produce 9.6 to 12.8 V swinging signal from the 3.2-Vpp pulse.

The charge balancing circuit is implemented using 1.8-V transistors, and is protected from high voltage swing in the electrode by the stacked transistors in the output driver reconfigured to act as a HV isolation switch.

Ⅲ. Circuit Design

1. DAC

The current stimulation amplitude is controlled by a 5-bit current steering DAC[6] shown in Fig 4. A cascode current-steering is chosen over other DAC architectures to ensure linearity and to simplify the control circuit. The designed DAC can produce currents from 4 to 128 μA with 4 μA step to minimize current consumption. This current is amplified by eight times at the output driver stage. In the simulation result, the average DNL and INL are 0.000581 LSB and 0.0076 LSB, respectively.

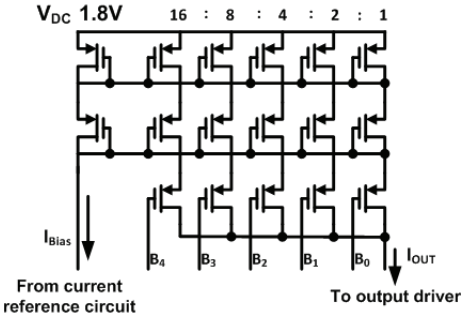


그림 4. Current-steering DAC의 회로도
Fig. 4. Schematic of current-steering DAC.

2. Output Current Driver

The output driver is designed to deliver a

maximum current of 1 mA to the electrode-tissue load. Thus a voltage difference of over 10 V is needed between the two load terminals. The driver usually consists of a current source and switches to control the current path for biphasic stimulation and a level-shifter to control the switches. In the proposed output driver, 3.3-V CMOS transistors in stacked configuration is used for the switches to replace HV transistors while satisfying high voltage compliance.

Figure 5 illustrates the diagram of two common types of output drivers used in neural stimulators. Fig. 5(a) shows the monopolar type while Fig. 5(b) shows the bipolar topology. The proposed output driver is based on the bipolar type due to its advantage of reduced power consumption with lower required supply voltage. In order to produce biphasic current, two switches diagonally opposite to each other in the bipolar driver are turned on at the same time. SW_2 and SW_3 are turned ON for cathodic phase, while SW_1 and SW_4 are turned OFF. In anodic phase, SW_1 and SW_4 are turned ON while SW_2 and SW_3 are turned OFF. When not stimulating, both electrodes are connected to the ground.

The schematic of the output driver, shown in Fig. 6, is used to deliver cathodic and anodic current to the electrode-tissue load. The current source at the top of the switch and current sink at the bottom are both used to control the stimulation operation. Instead of using only one current source (sink) to control the stimulation current, using both current source and current sink to push-pull the stimulation current for cathodic and anodic phase ensure good control of amount of charge delivered to and retrieved from the tissue. The switch is implemented using four stacks of 3.3-V transistors. The stacked switch is biased with dynamic gate biasing circuit[5] to ensure the voltage difference between terminals in each transistor is maintained below 3.3 V during operation.

In comparison to the work in [5], the usage of parallel capacitors to reduce the overshoot during transients in the dynamic biasing circuit are removed through careful simulations, saving much area in the overall current driver. Transistors M_{N5} and M_{N6} are added in the NMOS stack to facilitate both active charge balancing and electrode shorting operations after stimulation. The stacked switches provide the voltage compliance needed by the current source to push and pull stimulation current to and from the tissue. In addition, the stacks provide both high voltage protection for transistors M_{N5} and M_{N6} during the stimulation phase and a turn-ON path during the balancing phase. A high output resistance for the

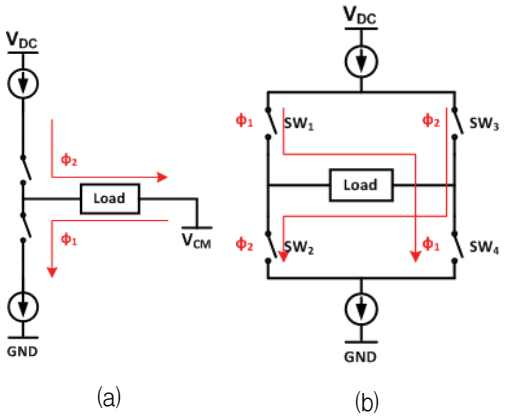


그림 5. (a) Monopolar 자극 방식 (b) Bipolar 자극 방식
Fig. 5. (a) Monopolar stimulation type
(b) Bipolar stimulation type.

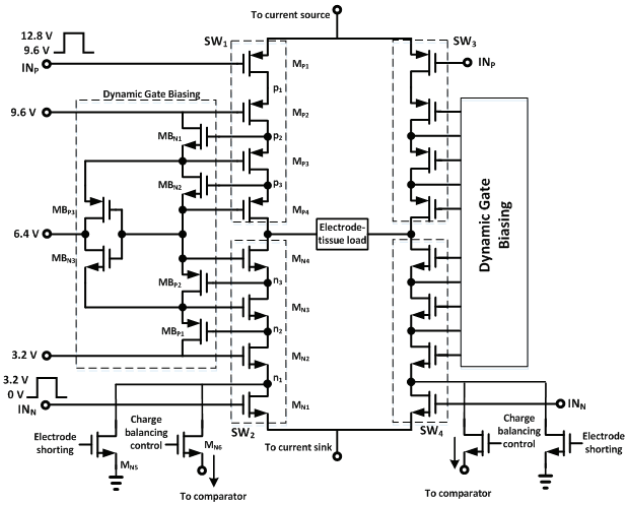


그림 6. 출력 드라이버의 회로도
Fig. 6. Simplified schematic of output driver.

current source is achieved by using large size transistors, with the width of the transistors also set to be large to minimize the voltage headroom to ensure enough voltage compliance for the load.

To explain the operation of the output driver, referring to Fig. 5(b) and Fig. 6, consider when SW1 is turned OFF and SW_2 is ON. When the NMOS input terminal INN changes from logic "low" to logic "high", transistor M_{N1} is turned ON, which leads to the node n1 to be discharged and turns ON M_{N2} as its gate terminal is biased constantly at 3.2 V (V_{DD1}). As node n2 becomes discharged, M_{BP1} turns ON, and the gate terminal of M_{N3} is shorted to V_{DD1}, which results in turning ON M_{N3}. The same reasoning can be applied to node n3, output node, transistor M_{BP2} and M_{N4}.

When gate terminal of M_{N4} is shorted to V_{DD1}, it has three effects. First it turns ON transistor M_{N4}. Secondly, it will turn ON M_{P4}, and then turn OFF M_{BN3} and turn ON M_{BP3}. As transistor M_{BP3} is turned ON, the gate terminal of M_{P3} is biased at 6.4 V (V_{DD2}). At this time the PMOS input terminal IN_P is at logic "low", which turns OFF M_{P1} and M_{P2}. As the gate of M_{P3} is biased at V_{DD2}, M_{P3} is also turned OFF, which means all the transistors comprising SW_2; M_{P1}-M_{P4} are all turned OFF.

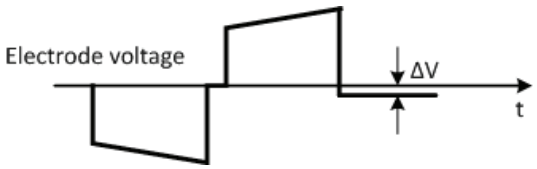


그림 7. 잔여 전하에 의한 전극에서의 전압 차 발생
Fig. 7. Diagram showing residual charge leading to increase in difference of electrode voltage.

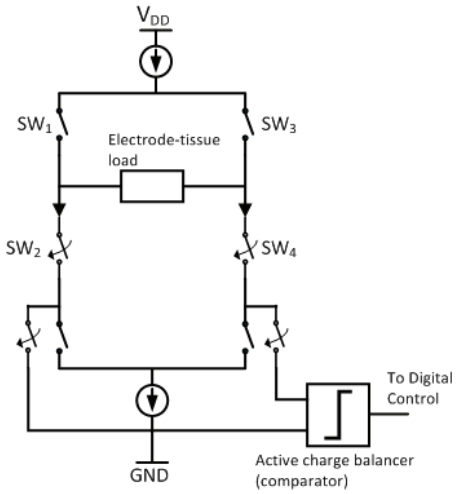


그림 8. Active charge balancer의 기본 동작 원리
Fig. 8. Basic operation of active charge balancer.

Careful consideration is needed when deciding the transistor size of the driver switch. The main path of the stacked switch is designed to be sufficiently large in order to carry as large current as 1 mA. Each size of the transistor is optimized to ensure correct operation within the allowable voltage range when the transistor switch is ON, OFF, and most importantly during transitions.

3. Charge Balancing Circuit

The mismatch within the output driver circuit results in the variation of current amplitude in each phase during stimulation. Although the mismatch is not significant for one stimulation cycle, the residual charge can accumulate after each stimulation cycle. The residual charge leads to the increase in voltage difference between the two electrodes as shown in Fig 7. The voltage difference should not exceed 100 mV[9], because it may cause damage in the tissue.

The basic operation of charge balancing circuit[2] is shown in Fig 8. After each stimulation cycle, the charge balancing phase begins. A charge balance trigger signal connects the electrode to a comparator through the turned-ON NMOS stack (SW_2 and SW_4) in the switch driver. The work in [2] uses a high voltage comparator in which high voltage transistors act as differential input stage to sense the electrode voltage and convert it into current, and then convert to low voltage before feeding it to the low voltage comparators. In this work, the voltage of the electrode is sensed and is converted to low voltage through the bottom stacked NMOS switch path. This way, both electrodes are shorted directly to low voltage comparator for comparison.

For one clock cycle, the comparator compares the

voltage difference between the two electrodes. The electrode voltage difference varies depending on the amount of mismatch between the biphasic pulses. If the voltage difference exceeds the safe limit which is set to ±50 mV[9], the result goes to the digital controller, delayed by one clock cycle, to then adjust the switch to enable secondary current flow in the direction to balance the residual charge. The charge balancing scheme is designed to utilize the same current source used in stimulation. The reasons are to save area and to minimize the time needed for charge balancing. The comparator consists of several low-voltage op-amps and the total current consumption is less than 2 μA. To save power, it is only turned ON during the charge balancing phase.

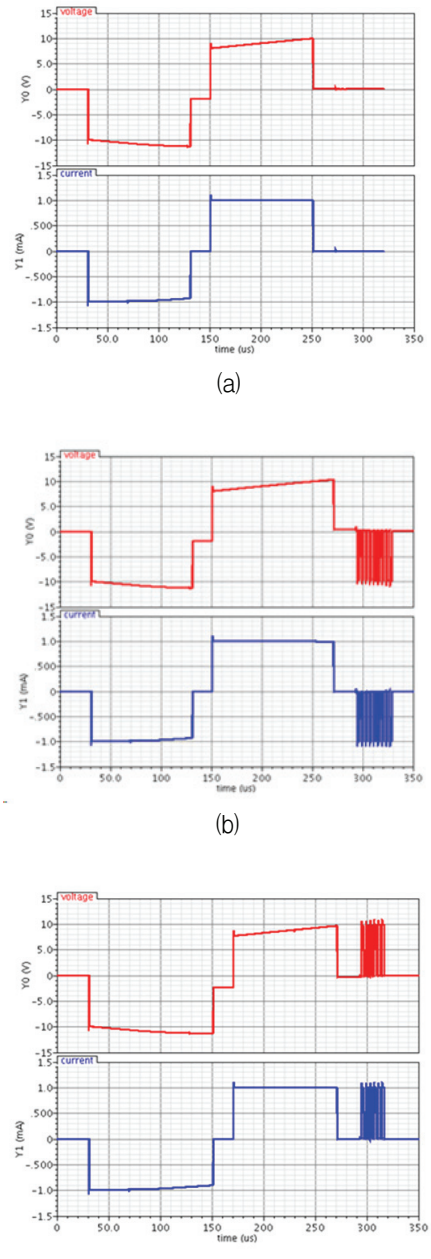
To ensure no charge remains, electrode shorting can also be performed after active charge balancing.

Ⅳ. Simulation Results

The stimulation period is set to be 400 μs, but it can be made adjustable. The cathodic and anodic pulse widths are set to 100 μs each, with interphasic delay of 20 μs. The charge balance trigger is set to be 20 μs after the stimulation phase with 10 μs duration.

Figure 9(a) shows the generated 1 mA stimulation current and the voltage between two electrodes. It can achieve good matching, with effective voltage difference between the two electrodes to be much less than 100 mV after stimulation.

To show the charge balancer in operation, the stimulator is forced to operate in an unbalanced situation. Figure 9(b) shows the voltage and current when anodic phase pulse width is set to be 20 μs wider than the cathodic phase, while Fig 9(c) illustrates the situation when the cathodic phase pulse width is set to be 20 μs wider than the anodic phase. The mismatch in duration and in current amplitude affect some charge to reside in the electrode. This is shown by the voltage across the electrodes for both



(a)

(b)

(c)

그림 9. (a) 자극 펄스의 출력 전압 및 전류 시뮬레이션 결과 (b) Cathodic 펄스에 mismatch가 추가 된 시뮬레이션 결과 (c) Anodic 펄스에 mismatch가 추가 된 시뮬레이션 결과

Fig. 9. (a) Simulated output voltage and current waveform of stimulation pulse (b) Simulated waveform with wider cathodic phase (c) Simulated waveform with wider anodic phase.

cases to exceed the safe window of ±50 mV. The charge balancing circuit then delivers current in such a way to make the voltage difference between two

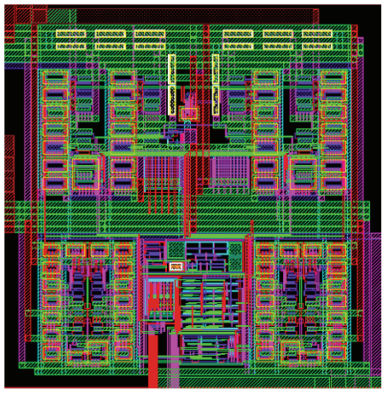


그림 10. 신경 자극 IC의 레이아웃
Fig. 10. Layout of neural stimulation IC.

표 1. Summary of proposed stimulation IC performance and comparison with previous similar works.
Table 1. Summary of proposed stimulation IC performance and comparison with previous similar works.

Parameter	[2]	[3]	[10]	This work
Supply voltage	22.5 V	15	18 V	12.8 V
Tissue load model	10 kΩ	10 kΩ	10 kΩ	10 kΩ
DAC bit	5 bit	5 bit	8 bit	5 bit
Stimulation current	32-992μA	32μA-1mA	4 μA-1mA	32-992μA
Current mismatch between cathode/anode	5% (avg.)	0.3% (avg.)	4.7% (max. current)	0.21% (avg.) 2.3% (max. current)
Charge balancing	Active	Shorting	Active + shorting	Active + shorting
Area	22 mm² (232 ch.)	0.1 mm²	2.27 mm²	0.13 mm²
Technology	0.35μm HVCMOS	0.35μm HVCMOS	0.6μm HVCMOS	0.18μm CMOS

electrodes to be within the safety range.

Figure 10 shows the layout of the designed overall neural stimulation IC. The total area including all the building blocks is 0.13 mm².

Table 1 shows the performance comparison with some previous works. This work uses 12.8 V of supply voltage which is the lowest value in comparison to previous neural stimulation drivers capable of generating a maximum stimulation current of around 1 mA to a 10 kΩ tissue-equivalent load model. This allows to reduce the power consumption during stimulation. In addition, all the previous works utilized HV CMOS processes for implementation while standard CMOS process is used for this work.

V. Conclusions

A biphasic neural stimulator with a current output range of 32 μA to 1 mA with active charge balancing circuit is designed using 0.18-μm standard CMOS process. A transistor-stacked architecture is used in the core output driver circuit to enable high-voltage compliance and the area of the designed stimulator IC is 0.13 mm².

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