http://dx.doi.org/10.5573/JSTS.2015.15.1.016 JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.15, NO.1, FEBRUARY, 2015

Forming Gas Post Metallization Annealing of Recessed AlGaN/GaN-on-Si MOSHFET

Jung-Yeon Lee, Bong-Ryeol Park, Jae-Gil Lee, Jongtae Lim, and Ho-Young Cha

Abstract—**In this study, the effects of forming gas post metallization annealing (PMA) on recessed AlGaN/GaN-on-Si MOSHFET were investigated. The device employed an ICPCVD SiO_2 film as a gate oxide layer on which a Ni/Au gate was evaporated. The PMA process was carried out at 350°C in forming gas ambient. It was found that the device instability was improved with significant reduction in interface trap density by forming gas PMA.**

Index Terms—**AlGaN/GaN heterostructure, forming gas annealing, interface trap density, MOSHFET, post metallization annealing**

I. INTRODUCTION

AlGaN/GaN heterostructures are a promising candidate for use in high-power and high-efficiency switching applications owing to their superior material properties, such as high breakdown field and high electron mobility [1-4]. In particular, AlGaN/GaN wafers grown on silicon substrates have gained additional attention due to their cost competitiveness with current Si technology. Prototype AlGaN/GaN FETs and power ICs have already demonstrated very low on-resistance and superior conversion efficiency in comparison with the state-of-the-art Si counterparts [5-7].

Insulated gate configuration has been widely employed in AlGaN/GaN power FETs because the insulated gate can suppress the off-state leakage current and adjust the threshold voltage. However, the bulk and trap charges generated during deposition and following process steps have strong influence on device characteristics, which becomes more critical when the device employs recessed-gate configuration with *ex-situ* gate insulator deposition. Since surface and interface states are strongly process-dependent, the gate insulator process must be carefully optimized.

It was reported that the insulator itself and interface conditions between insulator and semiconductor surface could be improved by appropriate post-annealing processes [8-12]. In this study, we investigated the effects of forming gas post metallization annealing (PMA) on recessed AlGaN/GaN-on-Si MOSHFET with ICPCVD SiO_2 gate oxide.

II. EXPERIMENTS AND DISCUSSIONS

Fig. 1 shows the cross-sectional schematic of recessed AlGaN/GaN-on-Si MOSHFET. The epitaxial layer structure consisted of a 4 nm undopped GaN capping layer, a 20 nm undoped AlGaN barrier, a 5 μm undoped GaN buffer on an N-type Si (111) substrate. The recessed gate region formed the metal gate/SiO_2/GaN MOS configuration whereas the parasitic channel region had the AlGaN/GaN heterostructure to keep a low channel resistance. The thickness of SiO_2 gate oxide was 35 nm. The 1 μm overhang from the gate edge formed a field plate under which a 150 nm SiN_x layer was inserted. The source-to-gate distance, gate length, and gate-to-drain distance were 3, 2, and 15 μm, respectively.

Devices were fabricated using the following process

Manuscript received Aug. 23, 2014; accepted Oct. 24, 2014
A part of this work was presented in Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices, Kanazawa in Japan, July 2014

School of Electrical and Electronic Engineering, Hongik University, 94 Wausan-ro, Mapo-gu, Seoul 121-791, Korea
E-mail : hcha@hongik.ac.kr

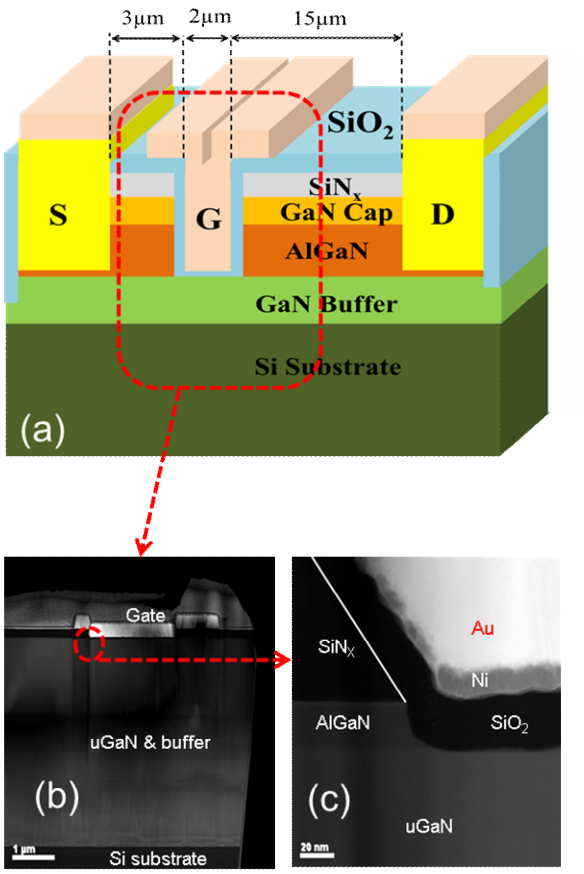


Fig. 1. (a) Cross-sectional schematic of recessed AlGaN/GaN MOSHFET, (b, c) TEM images of the recessed MOS gate region.

steps. After cleaning the wafer, a 150 nm SiN_x film, as a prepassivation layer, was deposited at 250°C using ICPCVD. Mesa isolation and gate recess were carried out using Cl_2/BCl_3 based ICP-RIE. As shown in Fig. 1(c), a sloped gate recess profile was obtained to suppress the localized high electric field. Ohmic contacts were formed by Si/Ti/Al/Mo/Au metallization followed by RTA annealing at 830°C. A 35 nm SiO_2 film was deposited at 250°C using ICPCVD [13]. A Ni/Au layer was evaporated for the gate and pad regions. Lastly, PMA was carried out by RTA at 350°C for 3 min in forming gas ambient (H_2(5%) + N_2(95%)) with the chamber pressure of 5 Torr.

1. Current-Voltage Characteristics

Current-voltage (I-V) transfer measurements were repeated using a dual sweep mode, i.e. positive and negative directions. As shown in Fig. 2, the initial characteristics before PMA process exhibited significant hysteresis with memory effects, suggesting negatively charged trapping effects. In contrast, no hysteresis was observed with a slightly enhanced on/off ratio after forming gas PMA. It should be noted that negative shift in threshold voltage was observed after forming gas PMA. In order to take a closer look at threshold voltage shift and uniformity issues, about 30 devices were measured at various locations in the sample. The threshold voltage variations before and after PMA are compared in Fig. 3. The initial threshold voltage was widely distributed from 1 to 4 V before PMA. On the other hand, the variation was significantly reduced to the range between -0.2 and 0.7 V after PMA. Since the threshold voltage is a strong function of oxide and interface charges, the threshold voltage and its uniformity must be associated with the change in oxide/interface charges during forming gas PMA. It is speculated that large variation of threshold voltage before PMA implies non-uniform distribution of oxide bulk charges caused by oxygen vacancies, and the hydrogenated dangling bonds and reduced oxygen vacancies after forming gas PMA are responsible for the improved uniformity and stability. Since the hydrogenated dangling bonds in SiO_2 act as positive charges, they would make negative shift in threshold voltage [14].

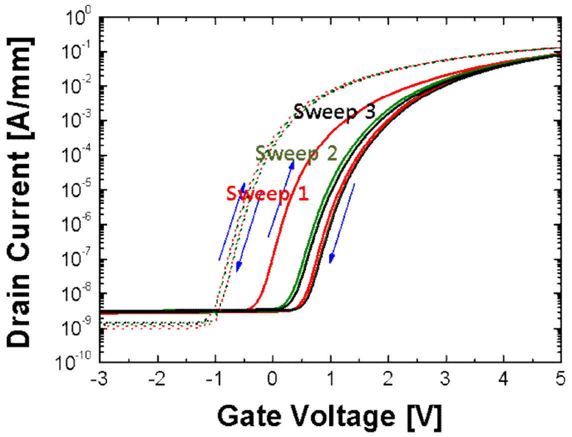


Fig. 2. Hysteresis of I-V transfer characteristics before (solid lines) and after (dot lines) forming gas PMA. The first, second, and third sweeps are shown in red, green, and black, respectively.

In terms of breakdown voltage characteristics, no significant change was observed after the forming gas PMA. Typical off-state breakdown voltages both before and after PMA were at least 1000 V.

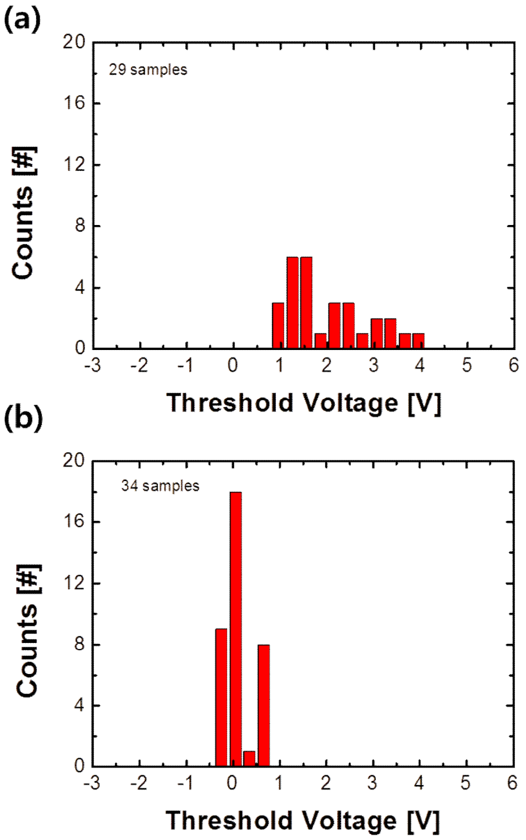


Fig. 3. Threshold voltage variation (a) before, (b) after forming gas PMA.

2. Capacitance-Voltage Characteristics and Interface Trap Density Extraction

In order to investigate the interface quality, the capacitance-voltage (C-V) characteristics were measured before and after PMA. C-V measurements were carried out using a circular recessed C-V pattern with a diameter of 50 µm. As compared in Fig. 4(a), the C-V hysteresis at 1 MHz was significantly reduced from 800 to 150 mV after forming gas PMA.

In order to quantitatively analyze the interface conditions, two different extraction methods, i.e. Terman [15] and Conductance [16] methods, were employed to estimate the interface trap density before and after PMA.

In Terman method, the interface trap density (D_{it}) is extracted by the following equation [17, 18]

$$D_{it} = \frac{C_{ox}}{q}\left[\frac{\left(\frac{\partial C}{\partial V}\right)_{ideal}}{\left(\frac{\partial C}{\partial V}\right)_{exp}} - 1\right] \qquad (1)$$

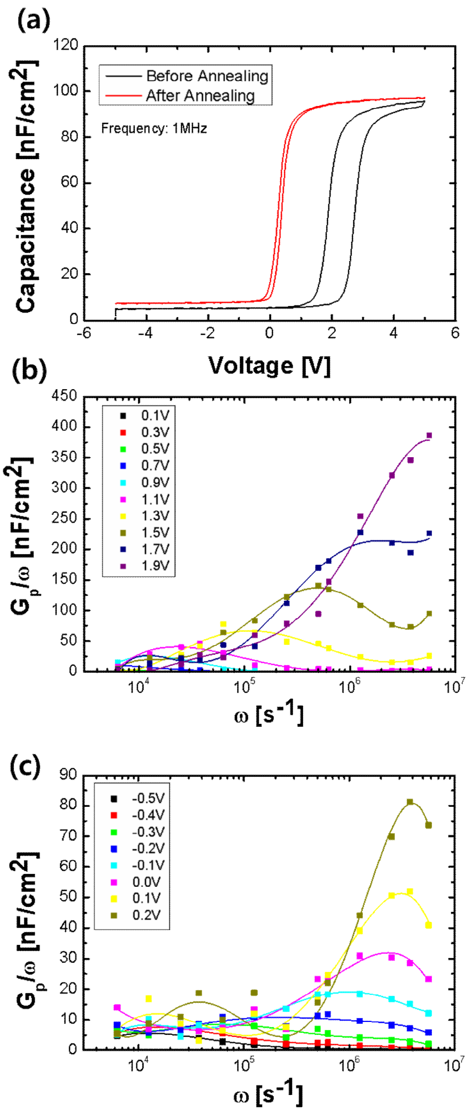


Fig. 4. (a) C-V hysteresis characteristics at 1 MHz and G_p/ω versus ω, (b) before, (c) after forming gas PMA.

where C_{ox} is the oxide capacitance and q is the electronic charge. The ideal capacitance characteristics were obtained by Schroder's method [19].

Unlike Terman method, Conductance method utilizes frequency dependent C-V characteristics to estimate D_{it}. The C-V characteristics were measured from 1 kHz to 1 MHz from which normalized conductance values were calculated as plotted in Figs. 4(b) and (c). The relationship between the normalized conductance (G_p/ω) and D_{it} is given by [19]

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{{G_m}^2 + \omega^2\left(C_{ox} - C_m\right)^2} \qquad (2a)$$

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\ln\left[1+\left(\omega\tau_{it}\right)^2\right] \qquad (2b)$$

where G_p is the parallel conductance, ω is $2\pi f$ (f = measurement frequency), G_m is the measured conductance, C_m is the measured capacitance, C_{ox} is the oxide capacitance, and τ_{it} is the trap time constant. An appropriate expression giving D_{it} in terms of the measured maximum conductance is $D_{it} \approx 2.5(G_p/q\omega)$ when $\omega \approx 2/\tau_{it}$ [19, 20]. The relationship between τ_{it} and the trap state energy (E_c-E_t) is given by [21]

$$\tau_{it} = \left[\left(\sigma_{it}N_C\upsilon_T\right)^{-1}\exp\left(\frac{E_c-E_t}{kT}\right)\right] \qquad (3)$$

where σ_{it} is the capture cross section of trap states, N_c is the density of states in the conduction band, and υ_T is thermal velocity. The values used for σ_{it}, N_c, and υ_T in this work are 3.4×10^{-15} cm^2, $4.3\times10^{14}\times T^{3/2}$ cm^{-3}, and 2.6×10^7 cm/s , respectively [21, 22].

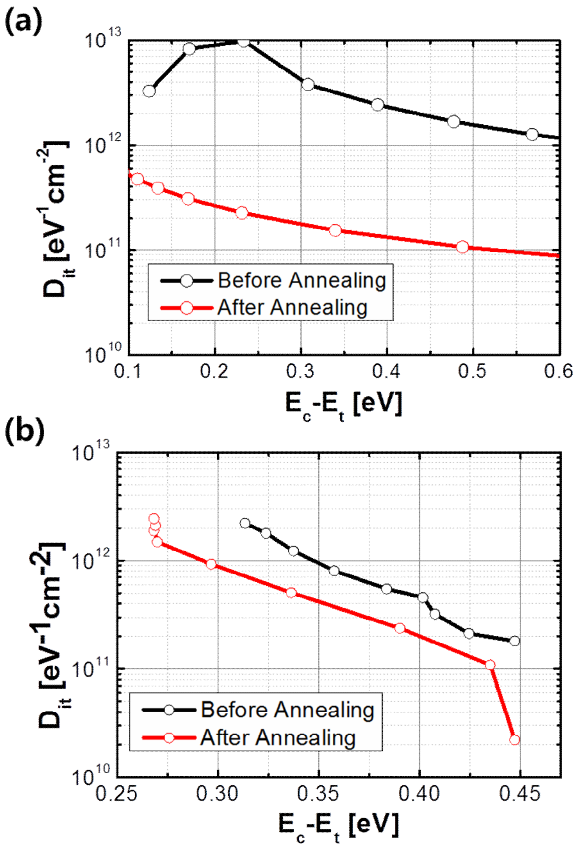


Fig. 5. D_{it} characteristics before and after forming gas PMA extracted by (a) Terman, (b) Conductance methods.

The D_{it} values extracted using Terman and Conductance methods are plotted in Fig. 5. Although two different methods did not give the same D_{it} values, both methods clearly exhibited noticeable reduction in D_{it} values after forming gas PMA. In comparison with other reports for GaN MIS configuration [23-25], very low D_{it} values were achieved in this work. It is suggested that the reduced interface trap states after forming gas PMA are responsible for the reduced hysteresis phenomenon.

III. CONCLUSION

We investigated the effects of forming gas PMA on recessed AlGaN/GaN-on-Si MOSHFETs that employed a SiO_2 gate oxide. It was found that the forming gas PMA not only eliminated the hysteresis phenomenon but also improved the threshold voltage uniformity. It is suggested that the hydrogenated dangling bonds and reduced oxygen vacancy in conjunction with the improved interface conditions are responsible for the improved device characteristics.

ACKNOWLEDGMENTS

This work was supported by No. 2012042153 and Nano Material Technology Development Program (NRF-2012M3A7B4035274) through National Research Foundation of Korea (NRF), the IT R&D program of MOTIE/KEIT (10048931, The development of epi-growth analysis for next semiconductor fundamental technology), and Korea Electric Power Corporation Research Institute through Korea Electrical Engineering & Science Research Insituitute (grant number : R13DA14).

REFERENCES

[1] J. G. Lee et al, “State-off-the-Art AlGaN/GaN-on-Si Heterojunction Field Effect Transistors with Dual Field Plates,” *Applied Physics Express*, Vol. 5, No. 6, p. 066502, May., 2012.

[2] O. Ambacher et al, “Two-dimensional Electron Gases Induced By Spontaneous And Piezoelectric Polarization In N- and Ga-face AlGaN/GaN Heterostructures,” *Journal of Applied Physics*, Vol. 85, No. 6, pp. 3222-3233, Mar., 1999.

[3] Z. Tang et al, “High-Voltage (600-V) Low-Leakage

Low-Current-Collapse AlGaN/GaN HEMTs With AlN/SiN_x Passivation," *IEEE Electron Device Letters,* Vol. 34, No. 3, pp. 366-368, March., 2013.

[4] W. Saito et al, "Recessed-gate Structure Approach Toward Normally Off High-Voltage AlGaN/GaN HEMT for Power Electronics Applications," *Electron Devices, IEEE Transaction on,* Vol. 53, No. 2, pp.356-362, Feb., 2006.

[5] W. Saito et al, "Design and Demonstration of High Breakdown Voltage GaN High Electron Mobility Transistor (HEMT) Using Field Plate Structure for Power Electronics Applications," *Japanese Journal of Applied Physics*, Vol. 43, No. 4B, pp. 2239–2242, Apr., 2004.

[6] E. Abdoulin et al, "High frequency 12V – 1V DC-DC converters – Advantages of Using EPC's Galium Nitride (GaN) Power Transistors vs. Silicon-based Power MOSFETs," *Application Note*, Efficient Power Conversion Corporation, www.epc-co.com, 2009.

[7] X. Hu et al, "Enhancement mode AlGaN/GaN HFET with Selectively Grown pn Junction Gate," *Electronics Letters,* Vol. 36, No. 8, pp. 753-754, Apr., 2000.

[8] S. Chandra et al, "Effect of Annealing on Structural and Electrical Properties of Ge Metal-Oxide-Semiconductor Capacitors with Pt Gate Electrode and HfO_2 Gate Dielectric," *Materials Tranasctions,* Vol. 52, No. 1, pp.118-123, Dec., 2010.

[9] H. Kambayashi et al, "High-quality SiO_2/GaN Interface for Enhanced Operation Field-Effect Transistor," *Physica Status Solidi A*, Vol. 204, No. 6, pp.2032-2036, Jun., 2007.

[10] R. D. Long et al, "Interface Trap Evaluation of Pd/Al_2O_3/GaN Metal Oxide Semiconductor Capacitors and The Influence of Near-Interface Hydrogen," *Applied Physics Letters*, Vol. 103, No. 20, p.201607, Nov., 2013.

[11] Y. Lin et al, "AlGaN/GaN HEMTs With Low Leakage Current and High On/Off Ratio," *IEEE Electron Device Letters*, Vol. 31, No. 2, pp.102-104, Feb., 2010.

[12] T. Hung et al, "Interface Charge Engineering for Enhancement-Mode GaN MISHEMTs," *IEEE Electron Device Letters*, Vol. 35, No. 3, pp.312-314, Mar., 2014.

[13] B. R. Park et al, "High-Quality ICPCVD SiO_2 for Normally Off AlGaN/GaN-on-Si Recessed MOSHFETs," *IEEE Electron Device Letters,* Vol. 34, No. 3, pp. 354-356, Mar., 2013.

[14] P. W. Peacock et al, "Behavior of Hydrogen In High Dielectric Constant Oxide Gate Insulators," *Applied Physics Letters,* Vol. 83, No. 10, pp. 2025-2027, Sep., 2003.

[15] L. M. Terman et al, "An Investigation of Surface States at a Silicon/Silicon Oxide Interface Employing Metal-Oxide-Silicon Diodes," *Solid-State Electronics,* Vol. 5, No. 5, pp.285-299, Oct., 1962.

[16] E. H. Nicollian et al, "The Si-SiO_2 Interface – Electrical Properties as Determined by the Metal-Insulator Silicon Conductance Technique," *The Bell System Technical Journal*, Vol. 46, No. 6, pp.1055-1133, Aug., 1967.

[17] H. -P. Chen et al, "Re-examination of The Extraction of MOS Interface-State Density by C-V Stretchout and Conductance Methods," *Semiconductor Science and Technology,* Vol. 28, No. 8, p. 085008, Jun,. 2013.

[18] A. J. Grede et al, "Components of Channel Capacitance in Metal-Insulator-Semiconductor Capacitors," *Journal of Applied Physics,* Vol. 114, No. 11, p. 114510, Sep., 2013.

[19] D. K. Schroder, *Semiconductor Material and Device Characterization*, A John Wiley & Sons, Inc., Publication, 2006.

[20] R. E. -H et al, "Comparison of Methods to Quantify Interface Trap Densities at Dielectric/III-V Semiconductor Interfaces," *Journal of Applied Physics*, Vol. 108, No. 12, p. 124101, Dec,. 2010.

[21] D. Gregusova et al, "Trap States in AlGaN/GaN Metal-Oxide-Semiconductor Structures with Al_2O_3 Prepared by Atomic Layer Deposition," *Journal of Applied Physics*, Vol. 107, No. 10, p. 106104, May., 2010.

[22] http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaN/bandstr.html

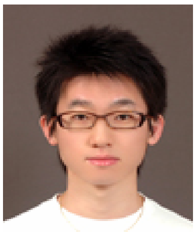
[23] H. Kambayashi et al, "High Performance Normally-Off GaN MOSFETs on Si Substrates," *224th ECS Meeting,* 27-1, p. 1911, Oct., 2013.

[24] H. -S. Yun et al, "Fabrication and Properties GaN MIS Capacitors with a Remote-Plasma Atomic-Layer-Deposited Al_2O_3 Gate Dielectric," *Journal of the Korean Physical Society*, Vol. 54, No. 2, pp. 707 -711, Feb., 2009.

[25] Y. Yao et al, "Normally-off GaN Recessed-gate MOSFET Fabricated by Selective Area Growth Technique," *Applied Physics Express,* Vol. 7, No. 1, p. 016502, Dec., 2013.

Jung-Yeon Lee received the B.S. degree in the school of electronic and electrical engineering from Hongik University, Seoul, Korea, in 2013. She is currently pursuing the M.S. degree at Hongik University. Her research interests include the modeling and the characterization of gallium nitride devices.

Bong-Ryeol Park received the M.S and Ph.D. degrees in electronic and electrical engineering from Hongik University, Seoul, Korea in 2009 and 2014. His research focuses on the simulation, the fabrication and the analysis of gallium nitride devices for high power applications.



Jae-Gil Lee received the B.S. and M.S degrees in electronic and electrical engineering from Hongik University, Seoul, Korea, in 2010 and 2012, respectively. He is currently pursuing the Ph.D. degree at Hongik University. His research focuses on the simulation, the fabrication and the analysis of gallium nitride devices for high power applications.

Jongtae Lim received the B.S. and M.S. degrees in Electronics Engineering from Seoul National University, Seoul, Korea in 1989 and 1991, respectively, and received the Ph.D. degree from the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, in 2001. In September 2004, he joined Korea Aerospace University, Goyang, Korea. Since March 2008, he has been with Hongik University, Seoul, Korea, where he is now Associate Professor of the School of Electronic & Electrical Engineering. His research interest are in digital communication systems, signal processing & semiconductor simulation.

Ho-Young Cha received the B.S. and M.S degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1996 and 1999, respectively, and the Ph.D. in electrical and computer engineering from Cornell University, Ithaca, NY, USA, in 2004. He was a postdoctoral research associated at Cornell University until 2005 and a research scientist at GE Global Research Center, Niskayuna, NY, USA, from 2005 to 2007. In 2007, he joined Hongik University, Seoul, Korea, where he is Associate Professor in the School of Electronic and Electrical Engineering. His research interests include wide bandgap semiconductor devices and sensors.