TRANSACTIONS ON ELECTRICAL AND ELECTRONIC MATERIALS
Vol. 16, No. 6, pp. 312-316, December 25, 2015

Regular Paper

pISSN: 1229-7607 eISSN: 2092-7592
DOI: http://dx.doi.org/10.4313/TEEM.2015.16.6.312
OAK Central: http://central.oak.go.kr

Use of Hard Mask for Finer (<10 μm) Through Silicon Vias (TSVs) Etching

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Received September 3, 2015; Revised October 4, 2015; Accepted October 13, 2015

Through silicon via (TSV) technology holds the promise of chip-to-chip or chip-to-package interconnections for higher performance with reduced signal delay and power consumption. It includes high aspect ratio silicon etching, insulation liner deposition, and seamless metal filling. The desired etch profile should be straightforward, but high aspect ratio silicon etching is still a challenge. In this paper, we investigate the use of etch hard mask for finer TSVs etching to have clear definition of etched via pattern. Conventionally employed photoresist methods were initially evaluated as reference processes, and oxide and metal hard mask were investigated. We admit that pure metal mask is rarely employed in industry, but the etch result of metal mask support why hard mask are more realistic for finer TSV etching than conventional photoresist and oxide mask.

Keywords: Through silicon via, Plasma etch

1. INTRODUCTION

As increasing demands for multi-function mobile consumer electronic devices, the complexity of the interconnection density of semiconductor chips continuously increase. Conventional chip to packaging integration (CPI) uses wire-bonding for interconnection of bonding pad to package leads. As chip scaling moves towards the atomic level, chip-to-chip interconnections using through silicon via (TSV) technology become an attractive potential solution for enabling higher performance form factors with low manufacturing cost [1]. Vertical electrical interconnects that pass through the silicon die can reduce the lengths of chip-to-chip interconnections and enable more compact CPI interconnection structures [2,3]. In TSV fabrication, high aspect-ratio structures with controlled sidewall profiles in silicon are important for microelectronic devices in the nanometer and micrometer scale [4].

TSV interconnection technology consists of deep silicon etching for via formation, insulating liner layer deposition, and via filling with conductive metals. Vertical and deep silicon via etching is attainable by plasma etching, but is still a challenging and complex fabrication process. Deep silicon via etching requires highly energetic ion bombardment to deliver enough kinetic energy to break chemical bonds of the silicon atoms on the wafer and immediate chemical reactions of highly reactive radicals to form a volatile etch by-products. Ion charging in a deep via region may cause a localization of silicon etching. Reactive radicals can increase the etch rate of silicon via, but it also increases lateral etch rate of TSVs. Increased ion bombardment can cause the erosion of via etch mask, and poor quality etch masks can result rough sidewall profiles [5]. Recent investigation employed hydrocarbon and hydro-fluorocarbon (HFC) gas chemistry to improve TSV etching profiles by forming a sidewall passivation and prevent etch mask erosion [6].

In this research, we investigated the effect of different types of etch mask in TSV etch and the effect of the sidewall profiles in TSVs. We first examined the sidewall profiles of TSV with a conventional photoresist (PR) mask, and investigated the effects of two types of hard masks on the sidewall profile of TSVs. The investigated TSV etch materials are photoresist, silicon dioxide, and aluminum. With narrower pattern sizes of masks, the etch depth and the etch rate tend to decrease.

Known as aspect-ratio-dependent-etching (ARDE), this result

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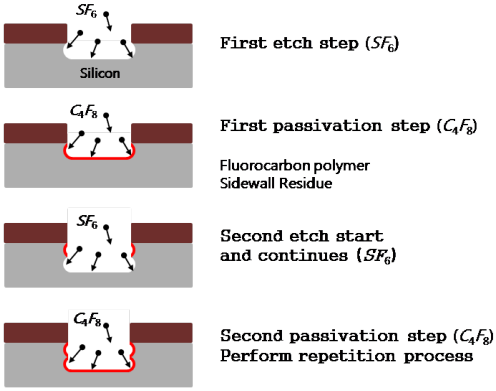

Fig. 1. Principle of deep reactive ion etching (DRIE- Bosch) process [7].

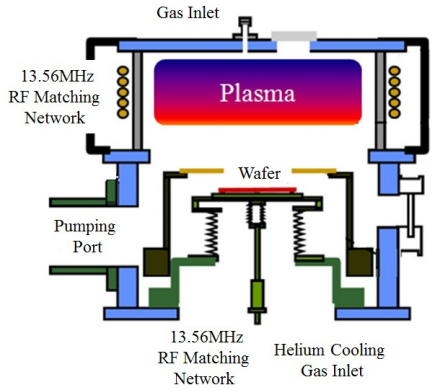

Fig. 3. A typical schematic of STS ICP etcher.

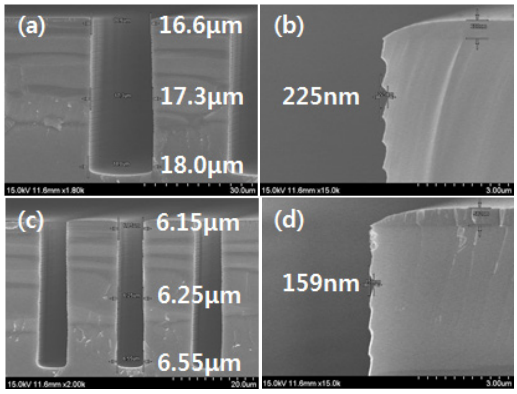

Fig. 2. Observed scallop pattern collapse measured at 6 μm diameter TSVs: (b) is a close up image of (a) and (d) is of (c).

is suspected to be primarily dependent on ion shadowing. When a soft mask had been used, scallop collapse of sidewall occurred below 6 μm as shown in Fig. 2.

Interaction between photoresist erosion and ion angular dispersion within sheath causes this abnormality. In contrast, no abnormalities occurred when hard masks were used. Etch rate and selectivity of the hard mask were superior compared to the soft mask. We recommend use of hard masks for finer TSVs and to reduce the amount of undercut and collapsed scallops.

2. EXPERIMENTS

Traditional plasma etching may suffer from a difficulty in high-aspect-ratio via etching, but the deep reactive ion etching (DRIE) with the Bosch process alleviated the concerns in TSV etching [8]. The Bosch process is performed by alternating passivation and etching steps, and is known as gas chopping etching or time multiplexed deep etching.

Figure 1 shows a schematic of typical Bosch process for deep silicon etching using SF_6 and C_4F_8 gases. In this experiment, we employed a STS-ICP DRIE system with SF_6, C_4F_8, and Ar gas mixture. SF_6 and C_4F_8 are known reactant gases for silicon etching, and *Ar* is used to increase physical etching to enhance the vertical sidewall profile in TSVs. The employed DRIE system consists of two 13.56 MHz RF power generators in the source and bias as shown in Fig. 3. The source power was fixed at 825 W, and the bias power was alternated 1 W to 13 W to increase the deposition rate of polymer and to increase the etch rate of silicon in etch step, respectively. Increased bias power decreases the physical distance of plasma sheath, and causes the formation of plasma near the wafer to increase the kinetic energy of ionic bombardment on the wafer surface, resulting in higher ion bombarded etch rate. A minimum amount of bias power of 1 W was applied during the polymer deposition cycle to create smoother cycle transitions between depositions and etch cycles instead of turning on and off the bias power.

Table 1. TSV etch recipe (source power was fixed at 825 W).

Step	Bias Power (W)	Pressure (mTorr)	Gas Flow (sccm) C_4F_8	SF_6	Ar	Time (sec)
Polymer deposition	1	22	100	0.5	25 30	5
Polymer etch	13	23	0.5	50	25 30	3
Silicon etch	13	23	0.5	100	25 30	5

Samples for TSV fabrication were prepared on 4 inch <100> *n*-type silicon wafers covered with three types of etch mask materials of photoresist, silicon dioxide, and aluminum. The average thickness of spin coated photoresist etch mask was 630 Å, PECVD deposited silicon dioxide (SiO_2) etch mask was 250±50 Å, and sputtered aluminum was 140±20 Å. Each type of samples contains various features and patterns from 100 μm to as small as 2 μm in diameters. Although TSVs smaller than 10 μm are unrealistically small in currently, further investigation is necessary to correlate TSV etch profiles with conventional silicon etching process.

Table 1 shows the process recipe including gas mixture used in this experiment.

3. RESULTS

Results of the etch profile using three different etch masks: photoresist, oxide, and metal. Factors considered for the evaluation of different types of etch mask are undercut, scallop, and etch rate.

3.1 Photoresist mask (Soft mask)

Table 2. TSV etch profile using AZ 1512 photoresist etch mask.

Factor	Pattern Size [μm] 100	50	20	10	8
Etch rate [μm/loop]	1.11	1.04	0.93	0.79	0.73
Undercut [nm]	211	212	185	172	66
Scallop [nm]	304	331	291	265	225
Undercut/Pattern size	2.11	4.24	9.25	17.2	8.25

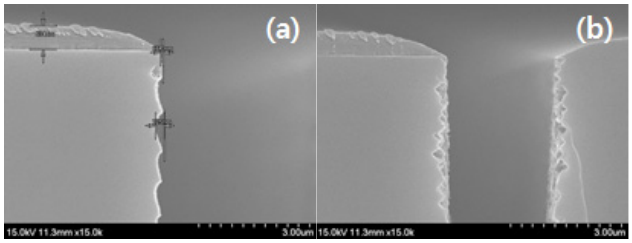

Fig. 4. The collapsed scallop in sidewall profile under the photoresist mask in small via patterns: (a) 8 μm via pattern and (b) 3 μm via pattern.

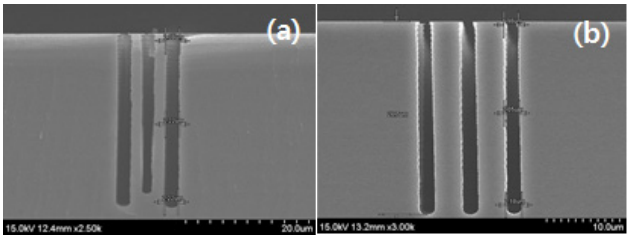

Fig. 5. Cross-sectional image of 2 μm sized TSVs with silicon dioxide etch mask: (a) Locally non-uniformly etched vertical profile with 30 sccm of *Ar* and (b) improved geometrical etch profile with 25 sccm of *Ar*, after process optimization.

Table 3. Etch result of using SiO_2 mask.

Factor	Pattern Size [μm]							
	20	10	8	6	5	4	3	2
Etch rate [μm/loop]	0.95	0.85	0.82	0.77	0.73	0.70	0.64	0.57
Undercut [nm]	581	568	621	568	555	568	542	528
Scallop [nm]	238	251	211	278	238	211	225	145
Undercut/Pattern size	29	57	78	95	111	142	180	264
Scallop/Pattern size	11.9	25.1	26.4	46.3	47.6	52.7	75.0	72.5

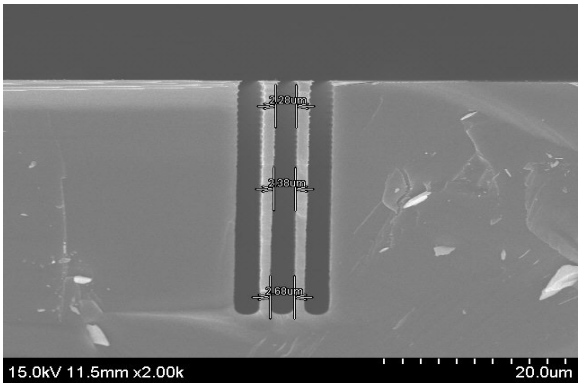

Fig. 6. Etch results of 2 μm pattern size under aluminum mask. Via was successfully etched well by 2 μm pattern size.

AZ 1512 photoresist was used for etch mask material, overall via etch results are presented in Table 2. Etch rates are monotonically decreased with the decrease in the size of diameters of TSVs, and is explained as the aspect ratio dependent etching (ARDE) in plasma etching. No significant amount of undercut was observed in larger vias, but undercut was drastically decreased in 8 μm sized vias. When the ratio of the amount of undercut and the pattern size was considered, smaller sized vias had much larger ratios of undercut to pattern size. This called our attention and led to further investigation of the etch profile in TSV for smaller pattern sizes with different mask materials.

Successful TSV profile was achieved in via sizes larger than 10 μm, but collapsed scallop patterns were observed below 10 μm size TSVs. Figure 4(a) shows via etching result in 8 μm sized via, and collapsed scallops began at the top of sidewall. As shown in Fig. 4(b), increased amount of collapsed scallops were observed in smaller sized vias. The scallop collapse has not been found in experiments using hard masks that will be described later.

3.2 Oxide mask (Hard mask 1)

Photoresists are useful etch mask materials for TSVs in larger diameter diameters, but may not suitable for smaller sized vias for collapsed scallops. To further investigate alternatives to photoresists for smaller sized TSV patterning, we investigated hard mask materials. The first candidate is silicon dioxide (SiO_2), and the geometrical characteristics of etched TSV profiles are presented in Table 3. Diameters larger than 20 μm of TSVs are beyond the scope of this experiment. Previously larger sized TSV etching in ARDE was also observed as via diameters were decreasing regardless the types of etch mask materials.

In terms of silicon etch rate employing silicon dioxide hard mask, it was successfully demonstrated a potential of TSV etch mask down to 3 μm diameter TSVs. We observed non-uniformly etched TSV profiles in a 2 μm diameter TSV, which is known as the loading effect [9] and is presented in Fig. 5(a). Etch rate uniformity deteriorates when pressure or average loading increase [10], and Argon does not chemically reacted with the poly and removes the passivation layer by sputtering the polymer with high energetic ions [11].

In order to avoid the loading effect due to high energy ions in our experiment, we reduced *Ar* flow from 30 sccm to 25 sccm, and a satisfactory etch profile was achieved as shown in Fig. 5 (b). The uniformity of the depth of the vias became uniform and via was etched well by 2 μm pattern size under silicon dioxide mask. Argon gas flow affected via depth uniformity. Although the etched profile appears successful from the presented SEM images in Fig. 5, TSVs with silicon dioxide mask still suffer from a large amount of undercut in smaller via geometries. For this reason, we investigated another type of hard metal to find a suitable etch hard mask material for finer TSVs in the next section.

3.3 Metal mask (Hard mask 2)

Among metal candidates used in semiconductor fabrication, aluminum is often selected for their ease of fabrication and compatibility with conventional fabrication process steps. Aluminum has been widely used for metal interconnections before copper metal interconnection is required for reducing interconnection delay. It is still used for back-end-of-line (BEOL) interconnection and bonding pad in many semiconductor products. Although metal etch masks are not used in conventional semiconductor fabrication processes, we are interested in this durable and reliable etch mask for the successful fabrication of finer features of TSVs. Table 4 shows via etch results with metal hard mask. As the pattern sizes become smaller, ARDE was also observed as shown in the previous experiments with different mask candidates.

Comparing the etch rates presented in Table 3 and 4, both types of hard masks showed similar etch rates in various sizes of TSVs. Unlike with hard oxide mask, metal masks showed improved undercut and scallop collapse, and the etched profiles are summarized in Table 4. Figure 6 shows TSV etch profiles in 2 μm diameter TSVs.

Table 4. Etch result of using Al mask.

Factor	Pattern Size [μm]							
	20	10	8	6	5	4	3	2
Etch rate [μm/loop]	0.93	0.84	0.80	0.75	0.73	0.68	0.62	0.58
Undercut [nm]	297	291	277	278	265	291	251	291
Scallop [nm]	242	278	251	251	198	198	185	211
Undercut/Pattern size	14.9	29.1	34.6	46.3	53	72.8	83.7	145
Scallop/Pattern size	20.3	10.1	9.51	5.41	4.16	3.75	2.47	2.91

4. DISCUSSION

4.1 Aspect-ratio-dependent-etching (ARDE)

With narrower pattern sizes, the etch depth is observed to decrease as shown in Fig. 7. Silicon etch rate is retarded especially with narrower pattern sizes is known as aspect-ratio-dependent-etching (ARDE) [12] or reactive ion etching (RIE) lag [13,14]. Although there are many factors of RIE lag, ARDE can be explained by three main reasons: ion shadowing, neutral shadowing, differential charging. Ion shadowing means the loss of ion flux at the bottom of the etched structure [12], neutral shadowing is caused by the depleted reactive neutral species in plasma [14,15], and differential charging which describes a tendency in which the top of pattern and top of sidewall is negatively charged and the bottom surface is positively charged if aspect ratio is higher [16]. In this experiment, we postulate that ion shadowing is the main reason for the observed ARDE. DRIE uses high-energy ion bombardment from plasma to attack the wafer surface and reactant gas species to chemically react with the surface material [17]. The loss of etchant species F ions is the main reason for deceleration of etching in narrower trenches [18,19]. As a result, ARDE occurred in all the cases of etch mask materials of photoresist, silicon dioxide, and aluminum mask. We also provide references for previous ARDE studies [7,20].

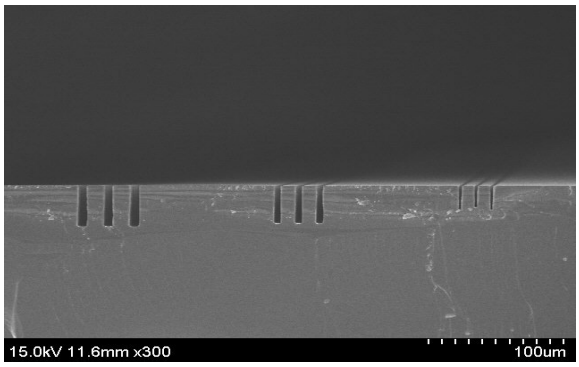

Fig. 7. Observed aspect-ratio-dependent-etching (ARDE) profile with photoresist mask.

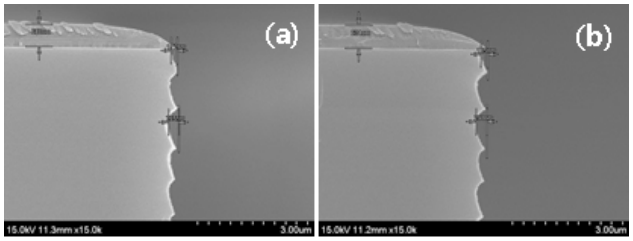

Fig. 8. Sidewall profile under the photoresist mask. The collapse scallop was not occurred under the photoresist mask at wider than 10 μm pattern size: (a) 10 μm pattern size and (b) 20 μm pattern size.

4.2 Photoresist erosion & ion angular dispersion

Soft masks in pattern sizes below 10 μm lead to collapsed scallops. In comparison, hard masks can yield a pattern up to 2 μm and can provide the better etch results than the soft masks. In this section, we describe the reasons of this phenomenon. Initially, collapsed scallops were thought to result from difference of substance between soft masks and hard masks. The photoresist soft mask is made up carbon-hydrogen bond, and the collapsed scallop were assumed to occur by reaction to carbon-hydrogen from the bond breaking polymer material by plasma [21,22]. If bond breaking of polymer material was cause of the collapsed scallop, sidewalls of whole pattern range under the photoresist mask must collapse similarly. For example, via pattern over 10 μm were successful as Fig. 8 but not below 10 μm. We noted two features in the collapse of scallop that started from top of sidewall and the thin form of photoresist mask on top edge of sidewall as in Fig. 8. The photoresist erosion is due to the formation of faceting angels on the top edge of patterns by high density ion plasma etch [23].

The start of the collapsed scallop from the top and photoresist erosion appeared to be related. In thinner photoresist masks both energy transmittance of mask and normalized focus range are increased [24,25]. This is why sidewall under thin photoresist mask has more damage rather than original thickness. Secondly, the cause of the defects of sidewall is the angular dispersion of ions by collisions with the sheath [26]. As the pattern narrows when the sidewalls get closer together, the number of ion collisions with sidewall increases at the top of the sidewall. The top sidewall receives more damage and the sidewall surface defects were created. The angular dispersion of ions is depicted in Fig. 9. This defect affects subsequent steps.

Since the sidewall surface defects were created during the previous etch steps, poor fluorocarbon polymer coverage on sidewall is created during passivation step. Poly-tetra-fluoro-ethylene (PTFE) is used to prevent lateral etching during severe etching [27]. If the sidewall surface becomes rough during the etch step, to deposit a polymer on sidewall as next step will fail, and it will get worse over and over again [28]. So in this research, collapsed scallop appears from the use of photoresist mask of narrow pattern. To solve this problem, mask thickness has to be increased. But thicker photoresist masks are prone to cracking as well as a large amount of photoresist have to be used [29]. On the other hand, silicon oxide mask and aluminum mask as hard mask endured plasma damage including ion bombardment. So

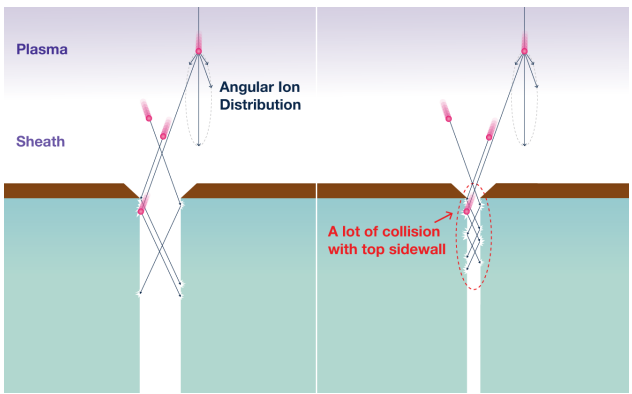

Fig. 9. The damage increased in top edge of sidewall of narrower pattern. As sidewalls get closer together, ion collision with sidewall increase from top edge of sidewall.

there were not collapsed scallop on sidewall and there became good profile until 2 μm pattern in using hard masks. Also in this research, we confirmed that selectivity of hard mask is higher than soft mask.

5. CONCLUSIONS

In this experiment, we investigated etch mask materials for the fabrication of finer sized through silicon vias (TSVs). Conventionally employed photoresist used as silicon etch masks may not be suitable for finer features of TSV fabrication using the Bosch process, and we suggested the use of hard masks for finer TSVs to reduce the amount of undercut and collapsed scallops. Hard metal masks in aluminum provided superior sidewall profiles of TSVs as small as 2 μm in diameter. Hard mask of silicon dioxide was useful in fabricating TSVs smaller than 20 μm, down to a few micro-meter diameters, but concerns of undercut below the oxide mask remain. Regardless of etch hard mask materials, ARDE from ion shadowing was observed.

ACKNOWLEDGMENT

This work was supported by the 2015 Small and Midsize Business Administration Industry-Academic Research Fund [C0328675].

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