# A Resistance Deviation-To-Time Interval Converter Based On Dual-Slope Integration

Zhi-Heng Shang*, Won-Sup Chung*★, and Sang-Hee Son*★

## Abstract

A resistance deviation-to-time interval converter based on dual-slope integration using second generation current conveyors (CCIIs) is designed for connecting resistive bridge sensors with a digital system. It consists of a differential integrator using CCIIs, a voltage comparator, and a digital control logic for controlling four analog switches. Experimental results exhibit that a conversion sensitivity amounts to 15.56 µs/Ω over the resistance deviation range of 0-200 Ω and its linearity error is less than ±0.02%. Its temperature stability is less than 220 ppm/℃ in the temperature range of −25-85℃. Power dissipation of the converter is 60.2 mW.

Key words: Resistive bridge sensor, Direct digital readout, resistance-to-time converter, second generation current conveyorm, Dual-Slope

## I. Introduction

Due to their high sensitivity, resistive sensor bridges are widely employed in industrial and process control systems and medical instrumentation. In order to interface these sensors with digital systems, an accurate interface circuit converting a small change of

resistance into a digital readout is required.

Several circuits are available in the literature for realization of such converters [1]-[7]. These are usually based on a resistance bridge. In these converters, the resistance deviation of resistive bridge sensors is converted into its corresponding offset voltage via a resistive bridge, this offset in turn is converted into a frequency (or time) by various oscillator circuits. A main drawback of these converters is that their frequency (or time period) outputs are proportional to not only the resistance deviation of sensors but also the timing component values.

The timing components usually have poor temperature stability and parasitic capacitances. The interface circuit which is not affected by the timing components is one based on charge-balancing type A/D converters, such as sigma-delta and dual-slope converters. These circuits give their outputs a digital pulse rate or a pulse width proportional to the bridge

imbalance and synchronous with the clock frequency. The interface circuits based on a sigma-delta A/D converter have been reported [8], [9]. These circuits have the advantages of simple structure and high noise rejection. However, they have a major disadvantage: their conversion characteristics are sensitive to temperature and supply voltage variations since their outputs are not only a function of resistance deviation but also a function of nominal resistance of sensor and current ratio of supply currents. Another disadvantage of these circuits is that the conversion resolution is limited by the delay imbalance of analog switches [8].

In this paper a new interface circuit with simple configuration and high stability on variations of temperature and nominal resistance of sensor is presented [10]. The proposed circuit is based on dual-slope integration using second generation current conveyors (CCIIs).

## II. Circuit Description and Operation

Fig. 1(a) shows the circuit diagram of the proposed resistance deviation-to-time interval (RD-to-TI) converter based on dual-slope integration. Here, resistors connected to the terminal Y of the CCIIs are half-bridge resistive sensors and $R_r$ connected to the terminal X is the fixed resistor. The converter consists of a differential integrator implemented with two CCIIs and a capacitor $C$, a comparator, and digital control circuits. Symbols and circuit diagrams of the CCIIs are shown in Fig. 2 [11]. CCII+ consists of a unity-gain buffer formed by transistors $Q_1$-$Q_4$ and two Wilson-current mirrors formed by $Q_5$-$Q_{10}$. In CCII- four Wilson-current mirrors are required. The operation of the converter can be divided into three states: "Initialization", "Inverting integration", and "Non-inverting integration", whose sequence and the voltage
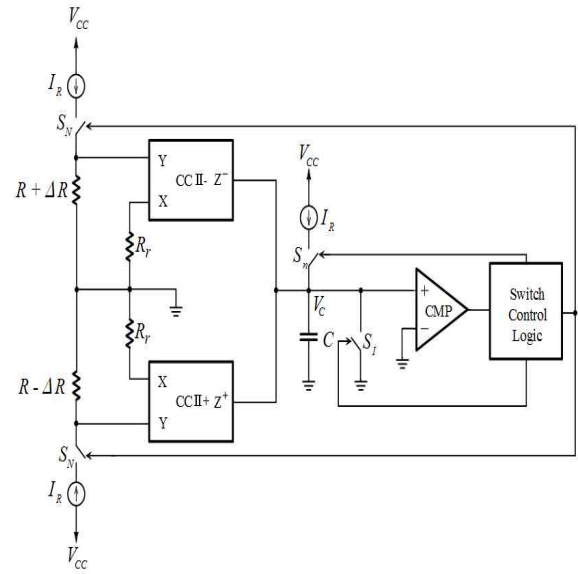


(a)
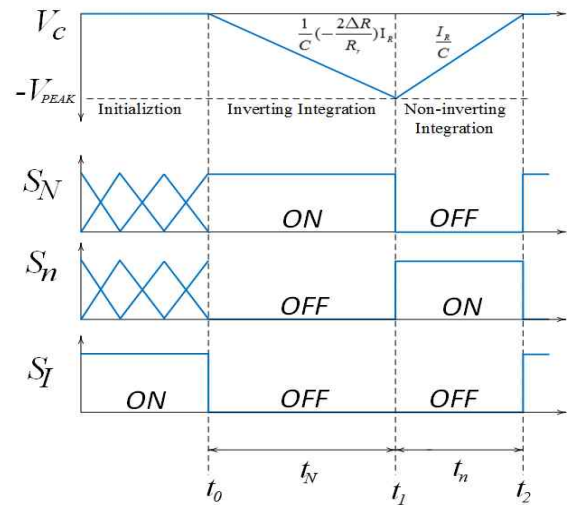


(b)

Fig. 1. (a) Circuit diagram of the resistance deviation-to-time interval converter based on dual-slope integrations using CCII, (b) timing diagrams of the state signals and the voltage waveform of the integrating capacitor.

waveform of the integrating capacitor at each state are shown in Fig. 1(b). The detailed operation in each state will be described in the following.
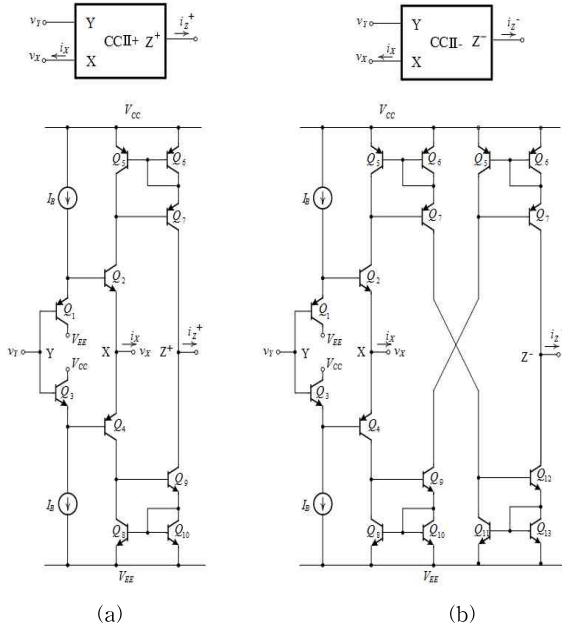
Fig. 2. Symbols and circuit diagrams of CCIIs used for the converter in Fig. 1: (a) CCII+; (b) CCII−.

## 2.1 Operation in "Initialization" state

In this state, while analog switch $S_I$ is kept "on", analog switches $S_N$ and $S_n$ do not matter. During this state, capacitor $C$ is discharged and its voltage $V_C$ is kept to zero.

## 2.2 Operation in "Inverting Integration" state

In this state, $S_N$ is kept "on", while $S_n$ and $S_I$ are kept "off", thereby the analog circuit forms the inverting integrator, which is composed of the half-bridge resistive sensors, the reference current $I_R$, the fixed resistor $R_r$, the positive current conveyor CCII+, the negative current conveyor CCII−, and the capacitor $C$. During this state, the current flowing through the capacitor $C$ is given by

$$I_C = -\frac{2\triangle R}{R_r}I_R \qquad (1)$$

where $\triangle R$ is the resistance deviation of the half-bridge sensors to be detected and converted into a time interval by the converter.

This current charges the capacitor, and thus capacitor voltage $V_C(t)$ may be expressed as follows:

$$V_C(t) = V_C(t_0) - \frac{2\triangle RI_R}{CR_r}\int_{t_0}^{t_1}dt \ (t_0 < t < t_1) \qquad (2)$$

where $V_C(t_0)$ is the initial voltage of the capacitor $C$. Equation (2) indicates that the capacitor voltage linearly ramps down with a slope of $-2\triangle RI_R/CR_r$. This inverting integration is carried out for a fixed period of time $t_N$ as shown in Fig. 1(b). Assuming that the initial voltage $V_C(t_0)$ of the capacitor $C$ is 0 V, the accumulated voltage of the capacitor at the end of the time period $t_N$ is given by

$$V_C(t_1) = -\frac{2\triangle RI_R}{CR_r}t_N \qquad (3)$$

After this integration the converter turns into the "Non-inverting integration" state.

## 2.3 Operation in "Non-inverting Integration" state

In this state, $S_n$ is kept "on", while $S_N$ and $S_I$ are kept "off", thereby the analog circuit forms the inverting integrator consisting of $I_R$ and capacitor $C$. During this state, the current flowing through capacitor $C$ is

$$I_C = I_R \qquad (4)$$

Therefore $V_C(t)$ may be expressed as follows:

$$V_C(t) = V_C(t_1) + \frac{I_R}{C}\int_{t_1}^{t_2}dt \ (t_1 < t < t_2) \qquad (5)$$

This shows that the capacitor voltage ramps up with a slope of $I_R/C$ until the ramp reaches back to zero as shown in Fig. 1(b). The zero crossing of the capacitor voltage will be detected by the comparator, which will then trigger digital control circuits to produce switch control signals for initializing the converter, and

the conversion cycle repeats. Let $t_n$ is the time duration of this non-inverting integration state, and combine (3) and (5). Then the relation between $t_n$ and $\triangle R$ may be expressed as follows:

$$t_n = \frac{2\triangle R}{R_r}t_N \qquad (6)$$

This equation indicates that the output time interval $t_n$ is directly proportional to the resistance deviation $\triangle R$. It is noticeable that the output time interval is independent of nominal resistance of sensor $R$ unlike the other works [2], [5]. This makes the converter have high stability on variations of temperature and nominal resistance of sensor. The digital values of $\triangle R$ can be known by counting the number of clock pulses gated into a counter for the time duration $t_n$.

## III. Non-Ideal Effects

For the proposed RD-to-TI converter, the CCII was implemented using bipolar transistor as shown in Fig. 2. Ideally, the input resistance at the X terminal of the CCII is zero and that at the Y terminal is infinite. The output resistance at the Z terminal of the CCII is infinite. However, the CCII actually has finite resistance for each terminal. The input resistance at the Y terminal is about 13 MΩ and that at the X terminal is about 150 Ω. The output resistance at the Z terminal is about 15 MΩ, which is sufficiently high to be negligible. Considering these finite resistances into the circuit analysis, the output of the converter can be expressed as follows:

$$t_n = \frac{2\triangle R}{R_r}t_N \frac{1}{(1+\frac{R_X}{R_r})(1+\frac{R+\triangle R}{R_Y})} \qquad (7)$$

where $R_X$ is the input resistance of the X terminal, and $R_Y$ is the input resistance of the Y terminal. Equation (7) can be rewritten using

Taylor series expansion as

$$t_n = \frac{2\triangle R}{R_r}t_N\left[1-(\frac{R_X}{R_r}+\frac{R+\triangle R}{R_Y})\right] \qquad (8)$$

This result indicates that the values in round brackets of right hand side are an error produced by the non-ideal input resistances of CCIIs.

## IV. Experimental Results

Based on the scheme in Fig. 1, a prototype circuit was built using discrete components. Transistors arrays 2N2222 and 2N2907 were used for implementing CCIIs. The bias currents $I_B$ of CCII+ and CCII− were set to 200 μA. The comparator was LM311. All of these devices were biased with ±5 V. The capacitor $C$ was 0.6 μF. A Wilson current mirror, which is formed by transistor arrays 2N2907 and resistor of 8.8 kΩ, was used to produce the reference current $I_R$ of 400 μA. The reference resistors $R_r$ were 1 kΩ. The clock frequency used in the control logic circuit was 3.3 MHz. $\triangle R$ was changed in 20 Ω steps from its fixed offset value of $R=1$ kΩ. Resistance was measured using Agilent digital multimeter type 34405A, and HP frequency counter 53131A was used to measure the time duration of the output pulse streams.

Fig. 3 (a) shows the entire circuit that includes control logic for experiment. Fig. 3 (b) shows the measured voltage waveforms of the circuit in fig. 3 (a).
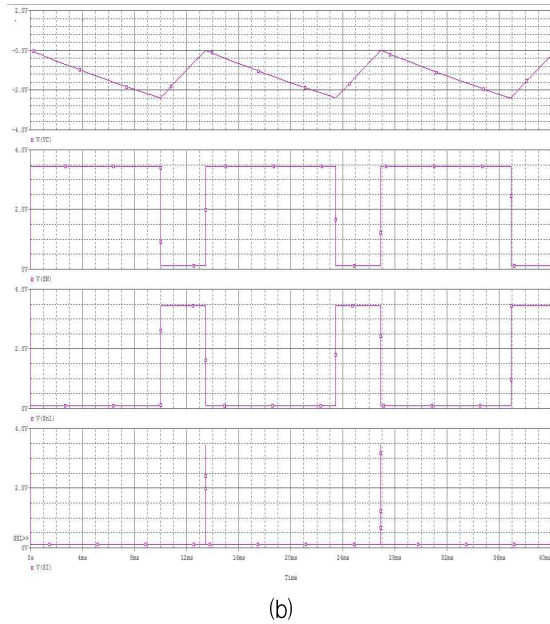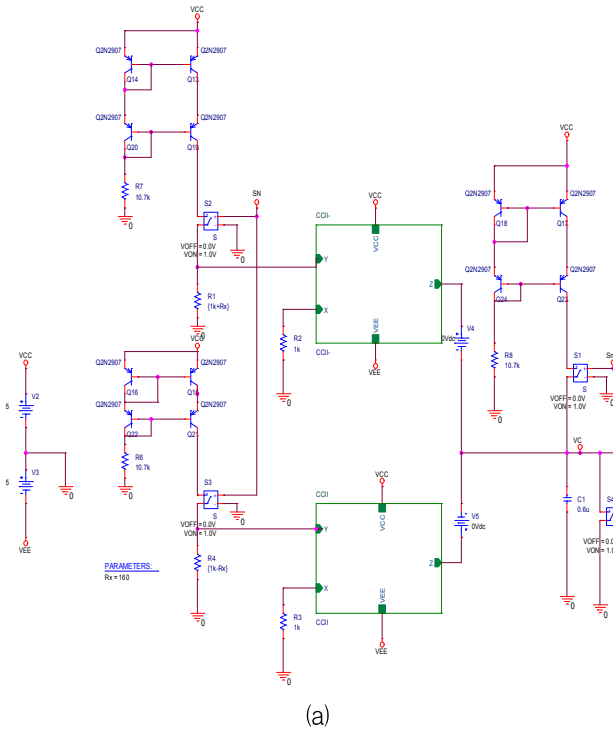
(a)



(b)

Fig. 3. (a) Entire circuit that includes control logic for experiment. (b) measured voltage waveforms of the circuit in Fig. 3. (a), Top trace: the voltage of the capacitor, Second trace: the voltage of analog switch,$S_N$Third trace: the voltage of analog switch $S_n$, Bottom trace: the voltage of analog switch.$S_I$

TABLE 1
performance characteristics of the converter

| Characteristics | Range/ Condition | Measured Values |
|---|---|---|
| Linearity error | @0–200 Ω | <±0.02% |
| Temperature stability | @−25–85℃ | <220 ppm/℃ |
| Power consumption | @$\triangle R = 160\Omega$ | 60.2mW |
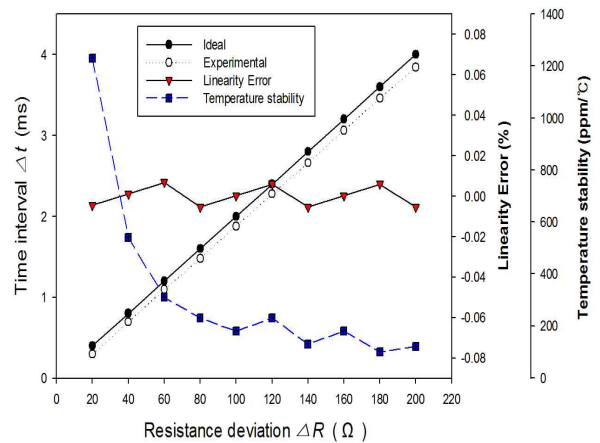


(a)
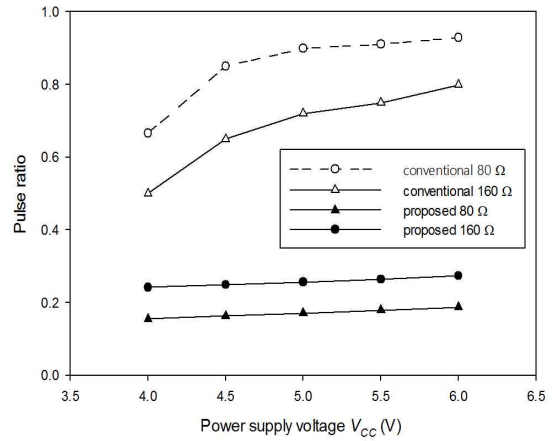


(b)

Fig. 4 (a) Measured time interval versus resistance deviation, its linearity error, and temperature stability measured in the temperature range of −25–85℃ when $t_N$ is 10 ms. (b) pulse ratio variation due to the power–supply voltage variation when $\triangle R = 80$ Ω and $\triangle R = 160$ Ω, respectively, where pulse ratio is $\left[t_n/\left(t_N + t_n\right)\right]$.

Fig. 4(a) shows experimental results when the inverting integration time $t_N$ was set to 10 ms.

It appears that the conversion sensitivity amounts to 15.56 μs/Ω with an offset error of 0.27 ms over the resistance deviation range of 0-200 Ω. The linearity error of conversion characteristic is less than ±0.02%, which is slightly lower than that of the previous converter [7].

The temperature stability of the proposed converter measured in the temperature range of −25-85℃ is less than 220 ppm/℃, while the temperature stability with the previous converter is about 250 ppm/℃. One can see that the temperature stability of the proposed converter is slightly lower than the previous converter. Fig. 4(b) shows the time interval variation due to the power-supply voltage variation when $\triangle R = 80$ Ω and $\triangle R = 160$ Ω, respectively. For comparison, the converter in [9] was also examined and the results are plotted in Fig. 4(b). Because of their different output types of the two converters, we represent Y-axis as pulse ratio $\left[ t_n / \left( t_N + t_n \right) \right]$ for comparison purposes. It appears that the proposed converter is about four times less affected by the supply voltage than the conventional converter. The results are summari zed in table 1 together with other performance characteristics.

## V. Conclusion

A novel RD-to-TI converter based on dual-slope integration using CCIIs has been described. The design principle and the circuit configuration are simple. Besides these, the converter features high stability on variations of temperature and supply voltage. These advantages make the converter especially suit for implementing a 'smart sensor', which gives a digital output directly connectable to a microprocessor.

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