A 900 MHz Zero-IF RF Transceiver for IEEE 802.15.4g SUN OFDM Systems

Changwan Kim, Seungsik Lee, and Sangsung Choi

This paper presents a 900 MHz zero-IF RF transceiver for IEEE 802.15.4g Smart Utility Networks OFDM systems. The proposed RF transceiver comprises an RF front end, a Tx baseband analog circuit, an Rx baseband analog circuit, and a ΔΣ fractional-N frequency synthesizer. In the RF front end, re-use of a matching network reduces the chip size of the RF transceiver. Since a T/Rx switch is implemented only at the input of the low-noise amplifier, the driver amplifier can deliver its output power to an antenna without any signal loss; thus, leading to a low dc power consumption. The proposed current-driven passive mixer in Rx and voltage-mode passive mixer in Tx can mitigate the IQ crosstalk problem, while maintaining 50% duty-cycle in local oscillator clocks. The overall Rx-baseband circuits can provide a voltage gain of 70 dB with a 1 dB gain control step. The proposed RF transceiver is implemented in a 0.18 μm CMOS technology and consumes 37 mA in Tx mode and 38 mA in Rx mode from a 1.8 V supply voltage. The fabricated chip shows a Tx average power of −2 dBm, a sensitivity level of −103 dBm at 100 Kbps with PER < 1%, an Rx input P_{1dB} of −11 dBm, and an Rx input IP3 of −2.3 dBm.

Keywords: CMOS, IEEE 802.15.4g, low-noise amplifier, passive mixer, PLL, RF transceiver, SUN, WPAN.

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I. Introduction

Remote metering of water, electricity, gas, and so on is currently performed by manual or semi-manual operation. To improve service efficiency and cost effectiveness, utility service providers require more intelligent metering systems. Radio frequency (RF)-based mesh networks are a good candidate to achieve a high efficiency with a low cost and therefore have huge market potential in the field of metering systems. Zigbee [1]–[4] is one of the solutions for RF-based mesh networking, but it has several drawbacks, including limited communication range, low data rates, instability of mesh routing, and shadow zone problems. To overcome these problems, the IEEE 802.15.4g Smart Utility Networks (SUN) standard [5] has been developed; the SUN system can communicate up to a range of 1 km and provides a maximum data rate of 1,600 Kbps. In addition, since it assures reliable mesh routing, it is expected to provide an adequate solution for RF-based mesh networking. Furthermore, it can be used for PC peripherals, personal healthcare, universal remote control (URC), and home control. Any IEEE 802.15.4g-compliant device shall at least implement one of the following physical layer (PHY) modes [5]: the MR-FSK PHY, the OFDM PHY, or the MR-O-QPSK PHY. In this paper, a high data-rate OFDM PHY-based RF transceiver is described.

This paper presents a 900 MHz zero-IF OFDM-based RF transceiver that is implemented in a 0.18 μm CMOS technology. To the best of our knowledge, this is the first report to describe a 900 MHz RF CMOS transceiver for the IEEE 802.15.4g SUN standard.

II. System Overview

The OFDM PHY in the IEEE 802.15.4g standard can

support data rates ranging from 50 Kbps to 800 Kbps. As shown in Table 1, the OFDM PHY includes four options (1 to 4), each being characterized by the number of active tones, a channel bandwidth, a sensitivity level, data rates, and so on [5]. Data rates in each option are also changeable with a different modulation scheme (that is, BPSK, QPSK, or 16-QAM). Since the total signal bandwidth for all cases ranges from 0.2 MHz to 1.2 MHz according to the number of active tones, multi-channel-selection low-pass filters should be adopted in the RF transceiver. However, since the subcarrier spacing is constant for all options and is equal to 10.416 kHz, the down-converted baseband signals in the receiver are located from 5.028 kHz to 600 kHz. An RF transceiver supporting a particular option (1, 2, 3, or 4) should be compatible with both binary phase-shift keying (BPSK) and quadrature phase-shift keying (QPSK) modulations, however, supporting 16-QAM is optional [5].

In the receiver, when the minimum input levels are measured at the antenna connector, the overall receiver noise figure (NF) is specified as 10 dB, but 6 dB of implementation margin is assumed in the standard. The minimum sensitivity level of −105 dBm for 50 Kbps with packet error rates (PER) of less than 10% and a maximum input signal level of −20 dBm are also specified. The linearity and sensitivity requirements are stricter than those of other wireless personal area network (WPAN) standards such as Zigbee [1]–[4]. The transmitter is recommended to provide a transmitted power of 10 dBm for wireless links of several hundred meters. However, due to the predetermined peak-to-average power ratio (PAPR) of about 10 dB, the average transmitting power level will be around 0 dBm. It would be challenging to achieve output power with a high efficiency using CMOS on-chip integration.

Table 1. Summary of OFDM PHY in IEEE 802.15.4g standard [5].

	Option 1	Option 2	Option 3	Option 4
BW (kHz)	1,200	800	400	200
FFT (tones)	128	64	32	16
Guard (tones)	23	11	5	1
Active (tones)	104	52	26	14
Pilot (tones)	8	4	2	2
Data (tones)	96	48	24	12
Subcarrier BW	10.416 kHz			
Sensitivity level PER < 10%	−103 dBm @100 Kbps	−105 dBm @50 Kbps	−105 dBm @50 Kbps	−105 dBm @50 Kbps
Data rates (Kbps)	100 – 800	50 – 800	50 – 600	50 – 300
Modulation	BPSK/QPSK : mandatory 16-QAM: optional			

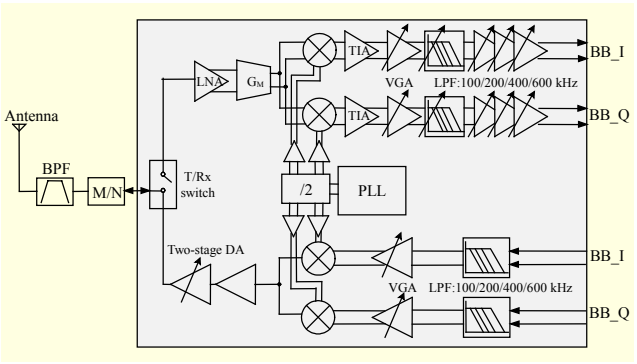

Fig. 1. Simplified block diagram of proposed zero-IF RF transceiver.

III. Transceiver Architecture

Figure 1 shows a block diagram of the proposed 900 MHz OFDM-based CMOS RF transceiver. To eliminate the need for image filtering, which increases the complexity and cost of the receiver, a zero-IF architecture is used in this work.

As shown in Fig. 1, the proposed RF transceiver is composed of a RF front end, a Rx baseband low-pass filter (LPF) and a variable gain amplifier (VGA), a Tx LPF and VGA, a T/Rx switch, and a voltage-controlled oscillator (VCO)-PLL block.

In the proposed RF front end, a T/Rx switch is integrated only at the input of the low-noise amplifier (LNA) so that the driver amplifier (DA) does not experience any signal loss caused by the T/Rx switch and provides a high output power to the antenna with a high dc efficiency. An external matching network (M/N) is used commonly as an input-matching circuit for the LNA in Rx mode and an output-power matching circuit for the DA in Tx mode, resulting in a small chip area due to fewer passive components. The RF transceiver integrates a ΔΣ fractional-N frequency synthesizer with a complementary differential (VCO) running at twice the local oscillator (LO) frequency of 1.4 GHz to 2 GHz. A divider-by-two circuit, following the VCO, generates quadrature 50% duty-cycle LO clocks for up- and down-conversion mixers. In the transmit path, quadrature analog-baseband signals are applied to a highly linear 5th-order active-RC LPF followed by a VGA. For the IQ modulation and frequency up-conversion, a single-ended quadrature voltage-mode passive mixer is utilized, which provides a high linearity with no LO leakage in the transmit path. To reduce dc power consumption, the two-stage DA has been designed with a single-ended topology, and it comprises class A and class AB amplifiers. In simulation, the transmitter achieves an output of 1 dB compression point of 10 dBm with a 1.8 V supply voltage. In the receiver chain, a noise-cancelling LNA topology [6] is used. The LNA's single-ended input is connected to the output of the DA to share the

matching network, and its differential output provides an active balun function for further differential signaling in the following receiver blocks. The RF signal amplified by the LNA is converted to RF current signal by a transconductance stage (G_M). Then, the RF current signal is down-converted to zero-IF by a current-driven quadrature passive mixer. To provide a large voltage swing of 1.4 V_{pp} to the analog-to-digital converter (ADC), the receiver analog-baseband circuit, comprised of a four-stage VGA and a 5th-order active-RC LPF, provides 70 dB of voltage gain with 1 dB gain control step.

IV. Circuit Design

Figure 2 shows the proposed RF front-end configuration, which consists of a single-ended 2nd-stage DA (M_1 and M_2), a noise-cancelling LNA (M_G and M_S), a T/Rx switch (sw0 and sw1), and an external M/N (L_1, L_S, and C_1). As shown in Fig. 2, the single-ended DA is implemented using n-MOS transistors to provide high output power, while the noise-cancelling LNA is implemented using p-MOS transistors to connect its single-ended input to the DA's output with dc-coupling through sw0. This configuration allows the DA and LNA to share a common RF pad and M/N. As shown in Fig. 2, in the transmit mode, the LNA is disabled when switch sw0 is off and switch sw1 is on. Thus, the M/N is used for the output power-matching circuit for the DA. The DA delivers its high output power to the antenna efficiently without any signal loss caused by the T/Rx switch. The simulated power-added efficiency (PAE) of the proposed DA is 36.5%. The input transistors M_G and M_S of the LNA are protected from the DA's large output power with both dc-isolation by sw0 and AC-isolation by sw1. In the T/Rx switch, the p-MOS switch sw0 has a high body voltage of V_{DD2} = 2.3 V through a high-value resistor R_B such that its drain and bulk are protected from breakdown. In the receive mode, the DA is disabled when sw0 is on and sw1 is off. The single-ended input of the LNA is directly dc-coupled to M/N, which is used for LNA's input-matching circuit and dc current path for M_G. Loss caused by sw0 at the LNA input is below 1.1 dB in the 900 MHz frequency range from simulation results.

The LNA in Fig. 2 adopts a noise-cancelling topology [6], which comprises a non-inverting signal path (M_G) and an inverting signal path (M_S) for noise cancelling and single-ended to differential signal conversion. The simulated NF of the proposed LNA with the T/Rx switch is 3.9 dB. Its single-ended input is connected to the single-ended output of the DA, and its differential output is connected to the following double-balanced passive mixer. In the LNA, since transconductances of the input transistors M_G and M_S are set to be equal to reduce dc power consumption, the impedance value of the two *RLC* loads is also identical. Under this condition, the thermal noise

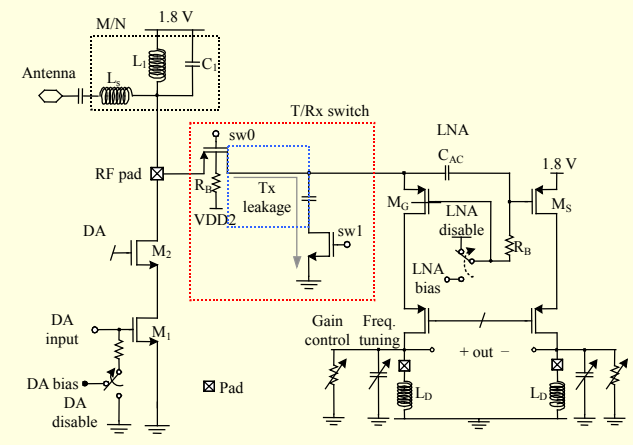

Fig. 2. Configuration of DA, LNA, and T/Rx switches.

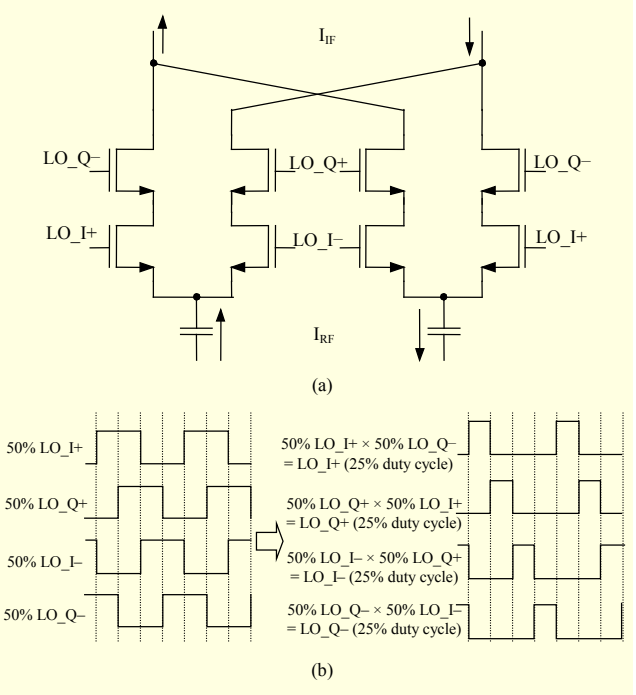

Fig. 3. (a) Proposed current-driven passive mixer (I-path) and (b) effective 25% duty-cycle clock generation using 50% duty-cycle clocks.

from M_G can be cancelled at the differential output and the fully differential output voltage signal can be achieved. The proposed LNA provides a high voltage gain of 30 dB and a low voltage gain of 10 dB to accommodate an RF input signal in a range from the minimum sensitivity level of −105 dBm to the maximum input level of −20 dBm. It draws 3.3 mA from a 1.8 V supply voltage.

In the proposed zero-IF receiver shown in Fig. 1, since the down-converted IF signal has occupied from 5.208 kHz, flicker noise may be troublesome for the receiver's sensitivity. To solve this problem, a quadrature current-driven passive

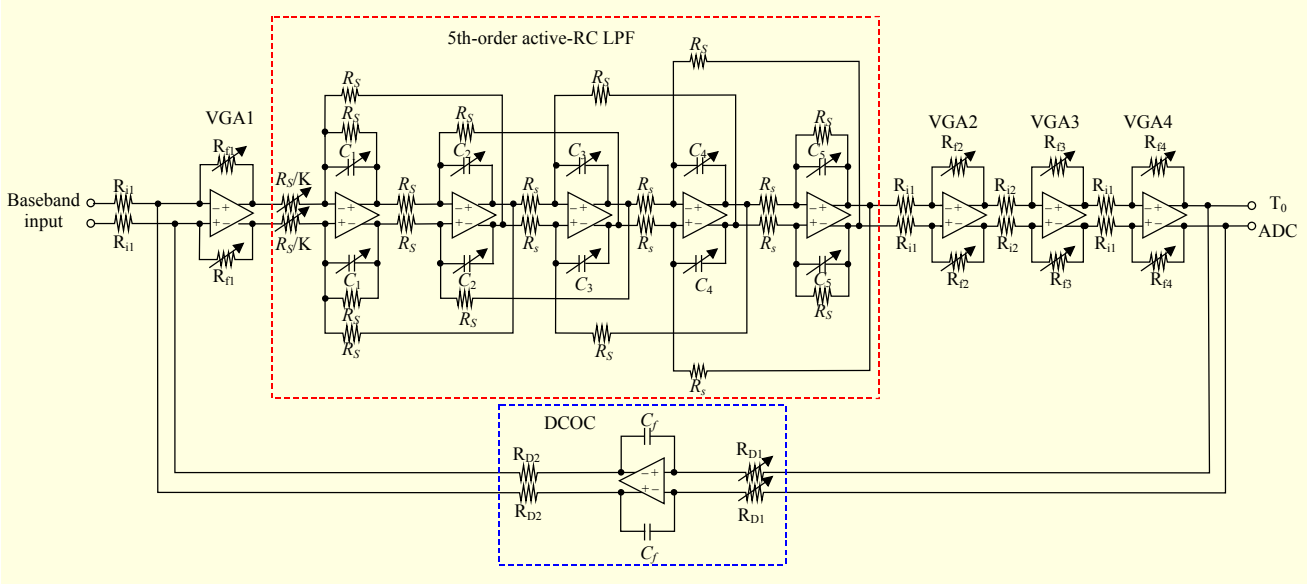

Fig. 4. Proposed baseband circuit (I-path).

mixer has been adopted in this work, as shown in Fig. 3, which provides little or no flicker noise while providing a high linearity in the receive path. However, passive mixers have no reverse isolation. As a result, in passive mixers with 50% duty cycle, an IQ crosstalk problem occurs since one mixer switch from the I-channel and the other mixer switch from the Q-channel are simultaneously on at any given moment [7]. To mitigate this IQ crosstalk problem, 25% duty-cycle passive mixers [7], [8] and an LO-2LO mixer [9] have been previously reported. However, these approaches [7]–[9] tend to require more complex LO-generation circuits and higher dc power consumption than those adopting 50% duty cycle. Therefore, a quadrature passive mixer topology, presented in [10], has been modified and then utilized in this work. Figure 3(a) shows the proposed current-driven passive mixer (only I-path), in which two switches are connected in series to form an AND function for two 50% duty-cycle LO clocks to achieve a 25% duty-cycle switching effectively. For example, in Fig. 3(b), multiplication of two 50% duty-cycle LO clocks, LO_I+ × LO_Q–, effectively generates a new 25% duty-cycle LO_I+ clock. In this way, the proposed passive mixer is effectively driven by 25% duty-cycle LO clocks, which can eliminate the IQ crosstalk in the receiver. The current conversion gain of the proposed current-driven passive mixer, shown in Fig. 3(a), can be briefly expressed as

$$\left|\frac{I_{IF}}{I_{RF}}\right| \approx \frac{\sqrt{2}}{\pi}, \qquad (1)$$

where I_{RF} and I_{IF} are a differential RF current signal and a differential IF current signal, respectively. This current conversion gain in (1) is equal to that of a 25% duty-cycle current-driven passive mixer [7]. Finally, the proposed current-driven passive mixer can solve the IQ crosstalk problem without degradation of other aspects of performance, requiring no additional circuits or additional dc power consumption.

Figure 4 shows the proposed analog baseband circuit (only I-path), comprising a channel-selection LPF, four resistive-feedback VGAs, and a dc offset cancellation (DCOC). The proposed analog baseband circuit provides a voltage gain of 70 dB in 1 dB step with a cutoff frequency from 100 kHz to 600 kHz depending on the channel bandwidth in use.

In general, since active RC LPF shows higher linearity than G_m-C LPF, a 5th-order active RC Chebyshev LPF [11], [12] has been adopted in Fig. 4. In Fig. 4, the 1 dB cutoff bandwidth of the channel-selection LPF is given by $1/(R_s \cdot C_{1-5})$ and controlled by the digitally-controlled capacitor C_{1-5} for high immunity of process, voltage, and temperature (PVT). In Fig. 4, VGA1 [13], which can provide a voltage gain of 24 dB, is followed by the channel-selection LPF to suppress flicker and thermal noises generated from the following circuits, while other VGAs are located after the channel-selection LPF for considering linearity. In Fig. 4, the channel-selection LPF and four VGAs use the same operational amplifier (OP)-amp, which is a two-stage configuration [13] with large input devices to suppress flicker noise at low frequency. The designed OP-amp shows a dc gain of 65 dB and a differential mode phase margin of 100° at a unit-gain bandwidth of 72 MHz, drawing 395 μA from a 1.8 V supply voltage. Measured output spectrum of the receiver has been shown in Fig. 5. dc-offset cancellation in a zero-IF receiver is inevitable since dc-offset may saturate the baseband output. As shown in Fig. 4, to solve the dc-offset problem, a DCOC loop has been built based

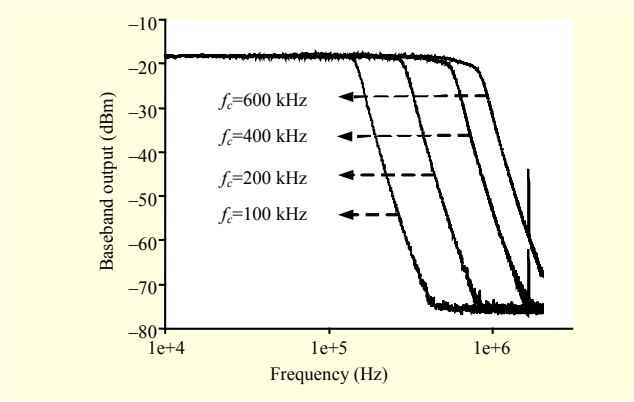

Fig. 5. Measured output spectrum of receiver.

on voltage-current negative feedback. In Fig. 4, the cutoff frequency of the DCOC is set at around 2 kHz since active subcarriers occupy from 5.208 kHz [5]. However, due to the low cutoff frequency in this work, the required capacitances C_f is 5 μF, which cannot be integrated on a chip. Thus, they are externally implemented at the cost of pads. To achieve a constant cutoff frequency in DCOC, the value of input resistor R_{D1} in DCOC digitally decreases as the voltage gain by an LPF and four VGAs in the forward path decreases. The post-layout simulation shows that the analog baseband output can be tolerated up to a 400 mV input DC offset. The OP-amp used in the DCOC consumes about four times the dc current in the 2nd-stage (compared to other OP-amps) to have a high zero frequency for loop stability and to provide enough feedback current through R_{D2}. The total dc current consumption for IQ-analog baseband circuits is 9.8 mA from a 1.8 V supply voltage.

In the proposed IQ direct-conversion transmitter, shown in Fig. 1, quadrature analog-baseband signals from digital-to-analog converters (DAC) are applied to a highly linear quadrature 5th-order active-RC LPF, and then subsequently to an IQ VGA with a 6 dB gain range. For IQ modulation and frequency up-conversion, a quadrature voltage-mode passive mixer has been utilized in this work since it provides higher linear characteristics, requires no dc power consumption, and has a smaller chip area compared to the Gilbert active mixer. Figure 6 shows the proposed up-conversion passive mixer, where two switches are also connected in series to form an AND function for two 50% duty-cycle LO clocks to achieve a 25% duty cycle; this being effectively the same as the down-conversion passive mixer in Fig. 3. Since this configuration mitigates the unwanted IQ crosstalk in the proposed IQ direct-conversion transmitter, the two RF sides of the mixers do not need to be buffered by two transconductors [14]; thus, leading to a smaller chip area and lower dc power consumption. Though the proposed passive mixer is designed with a single-ended topology to drive the following single-ended DA, it does not produce LO leakage to its single-ended output [14], [15]. In

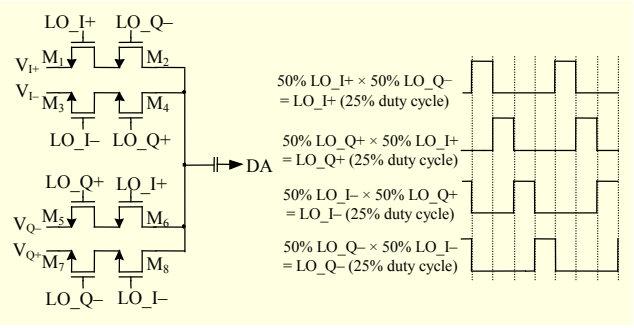

Fig. 6. Proposed up-conversion passive mixer.

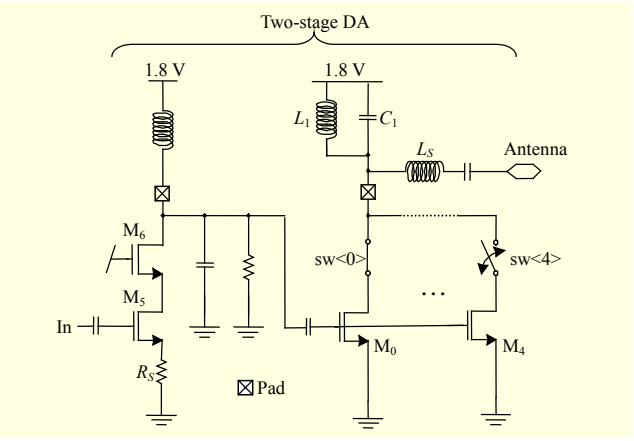

Fig. 7. Simplified two-stage driver amplifier.

the proposed up-conversion passive mixer, if the IF quradrature-input-voltage signals are $V_{I\pm} = \pm A\cos\omega_{IF}t$ and $V_{Q\pm} = \pm A\sin\omega_{IF}t$, the up-converted output voltage signal $V_{RF,out}$ can be expressed by

$$V_{RF,out}(t) \approx \frac{2\sqrt{2}}{\pi} A\cos(\omega_{RF}t + \varphi), \quad (2)$$

where A is the amplitude of IF voltage signals, and φ is a phase delay. From (2), the voltage conversion gain is –0.9 dB and is equal to that of the 25% duty-cycle single-ended passive mixer described in [15].

Figure 7 shows the proposed driver amplifier. Considering linearity and power efficiency, the proposed DA has been designed as a single-ended two-stage topology; it comprises class A and class AB amplifiers. As shown in Fig. 7, the first stage amplifier (M_5 and M_6) with an *RLC* resonate load is biased in class A mode and also source-degenerated by R_S to achieve high linearity. It provides a high voltage swing for the following class AB amplifier with a moderate gain and high linearity. The second-stage amplifier is a cascode common-source class AB amplifier, where the amplifier transistors are split into binary scaled units (M_0 to M_4) that can be turned on or off by thick-oxide cascode transistor switches of sw<0> to sw<4> such that dc power consumption is proportional to the

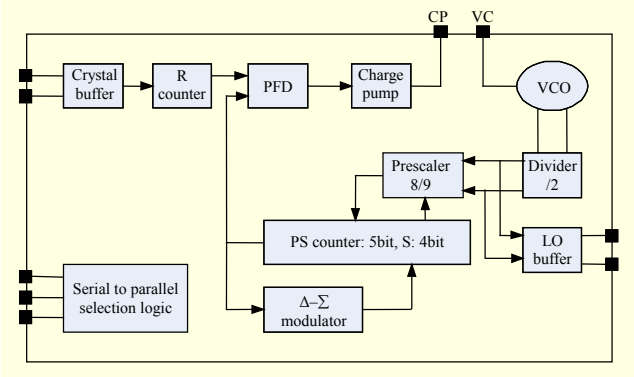

Fig. 8. Block diagram of PLL.

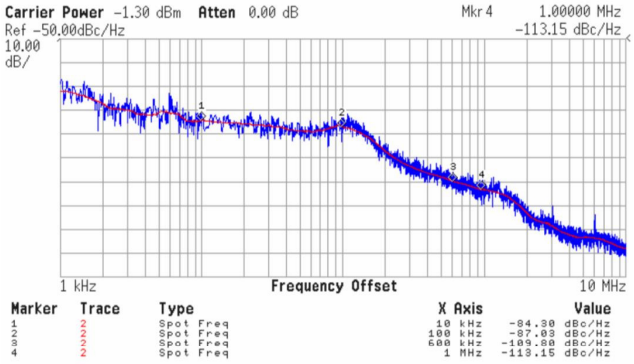

Fig. 9. Measured phase noise.

output power level. In Fig. 7, the variable output power range of the overall DA is from −10 dBm to 10 dBm and the corresponding dc power consumption is from 8.1 mW to 24.3 mW. To achieve a high-output compression point with a 1.8 V supply voltage, the output of the second stage is power matched instead of gain matching by using a series inductor *Ls* and resonant circuit (L_1 and L_2) at the cost of gain reduction of 1.5 dB. In Fig.7, all inductors used for DA are externally implemented for smaller chip size.

Figure 8 shows a block diagram of the proposed ΔΣ fractional-N frequency synthesizer. It uses a 24 MHz reference clock with a complementary differential VCO running at twice the LO frequency of 1.4 to 2 GHz. A divide-by-two circuit converts the differential VCO output signal to quadrature 920 MHz LO signals for the up- and down-conversion passive mixers shown in Figs. 3 and 6. The 3rd-order three-bit output ΣΔ modulator improves the closed-in phase noise and provides a resolution of 91.55 Hz. The measured output phase noise is shown in Fig. 9, which is −84 dBc/Hz at a 10 kHz offset and −113 dBc/Hz at a 1 MHz offset, respectively.

V. Measurement Results

The proposed 900 MHz zero-IF OFDM-based RF transceiver was implemented in a 0.18 μm CMOS technology. The die micrographic image is shown in Fig. 10, and the chip area, including pads, is 2.8 mm × 3.0 mm. The fabricated RF transceiver consumes 37 mA in Tx mode and 38 mA in Rx mode from a 1.8 V supply voltage. The fabricated chips have been MLF packaged and then mounted on an FR4 test board. As shown in Fig. 11, the test board consists of three printed circuit boards (PCBs); the upper PCB is for the RF chip, the middle PCB is for the ADC/DAC, and the bottom layer is for the Modem/MAC. Although not described in this paper, ADC and DAC were also implemented in a 0.18 μm CMOS technology. Modem and MAC are also designed with FPGA to support OFDM signals. By using this FR4 test board, the fabricated RF chips have been evaluated for option 1, since

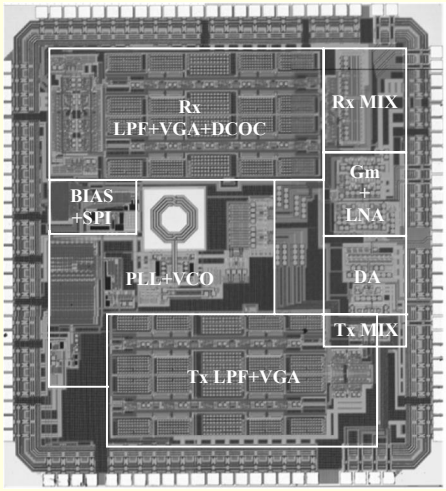

Fig. 10. Chip micrograph.

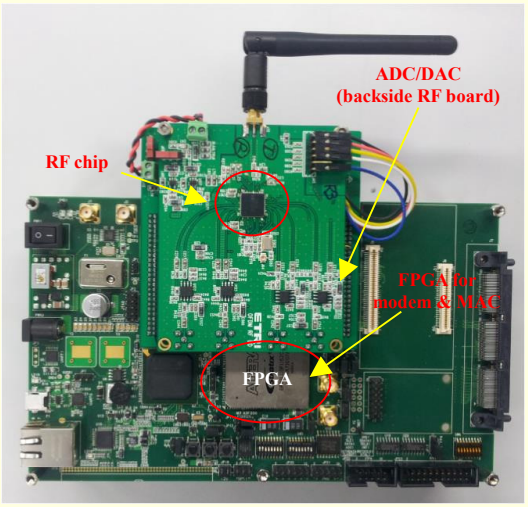

Fig. 11. Test board comprises RF chip, ADC/DAC, and Modem/MAC.

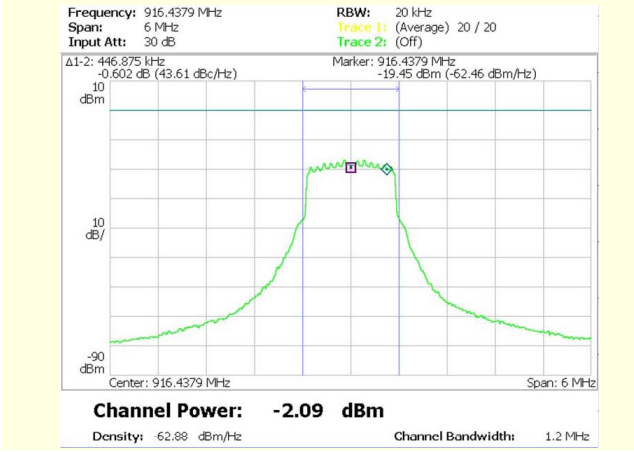

Fig. 12. Transmitted output signal spectrum.

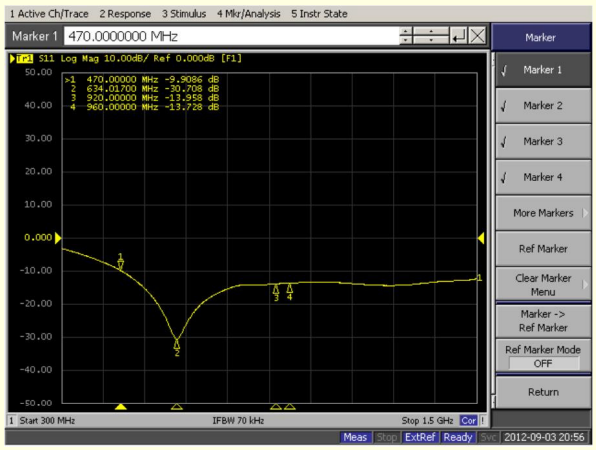

Fig. 13. Measured input return loss (S_{11}) for receiver.

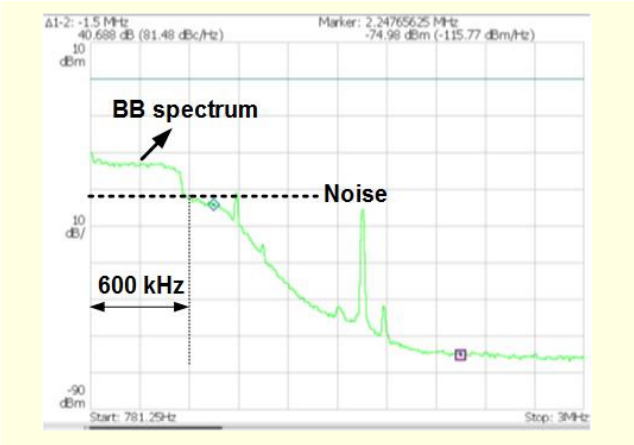

Fig. 14. Measured receiver output spectrum.

RF requirements described in option 1 are most challenging, as shown in Table 1.

Figure 12 plots the measured output spectrum of –2 dBm (including cable loss), which was QPSK-modulated with a data rate of 800 Kbps. In Fig. 12, the occupied channel bandwidth is 1.2 MHz, but it can also be changed to 800/400/200 kHz to support various data rates. Figure 13 shows the measured input return loss (S_{11}) of the receiver. Though the input resonant frequency has been shifted to 634 MHz due to unexpected parasitic capacitances, the input return loss is still better than –13 dB at the 900 MHz frequency

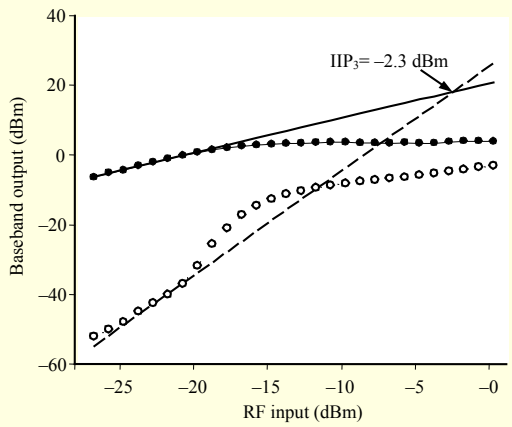

Fig. 15. Measured receiver IIP_3.

Table 2. Performance summary and comparisons.

	This work	[2]	[3]	[4]
RF freq. (Hz)	920 M	2.4 G	2.4 G	2.4 G
Rx architecture	Zero-IF	Low-IF	Zero-IF	Low-IF
NF (dB)	-	5.7	9.5	-
Sensitivity (dBm)	–103	–102	–96	–82
ICP1 (dBm)	–11	-	–27	-
IIP_3 (dBm)	–2.3	–16	–18	+6
IIP_2 (dBm)	> 25	-	> 25	-
Tx power (dBm)	–2	+3	+3	0
Tx OCP1 (dBm)	+10	-	+5	-
Rx mode (mA)	38	11	13.6	11.7
Tx mode (mA)	37	12.9	15.7	16.7
Supply voltage (V)	1.8	1.8/3.75	1.8/3.6	1.8
CMOS Tech. (μm)	0.18	0.18	0.18	0.18

Table 3. Measured sensitivity levels for option 1.

Data rates	Standard (PER < 10%)	Measured (PER < 1%)
100 Kbps	–103 dBm	–103 dBm
200 Kbps	–100 dBm	–102 dBm
400 Kbps	–97 dBm	–101 dBm
800 Kbps	–94 dBm	–98 dBm

band. Figure 14 shows the output spectrum of the receiver when the RF-modulated signal supporting option 1 has been applied to the input of the receiver. In Fig. 14, unwanted spurs in out-of-channel bands are caused by series-to-parallel interface clocks, not causing any degradation to the receiver performances. For linearity measurements, two RF single tones with a 100 kHz offset have been applied to the receiver in low-gain mode. As shown in Fig. 15, the measured input IIP_3 is –2.3 dBm. Table 2 summarizes the measured RF transceiver performance and compares the values with those of previously reported IEEE 802.15.4 transceivers [2]–[4].

The receiver sensitivity level has also been tested for option 1. The measured minimum sensitivity level at a data rate of 100 Kbps is –103 dBm with a PER < 1%, and the sensitivity level for a data rate of 800 Kbps is –98 dBm with a PER < 1%. Table 3 summarizes other measured sensitivity levels for various data rates. Finally, the measured sensitivity levels all satisfied the IEEE 802.15.4g OFDM PHY [5]. In addition, a public demonstration of the fabricated RF CMOS transceiver has been carried out, which shows the possibility of its use in commercial products [16].

VI. Conclusion

This paper has presented a 900 MHz zero-IF OFDM-based RF transceiver for IEEE 802.15.4g SUN systems, which is implemented in a 0.18 μm CMOS technology. The measured results demonstrate that the proposed RF transceiver favorably supports the IEEE 802.15.4g OFDM PHY requirements.

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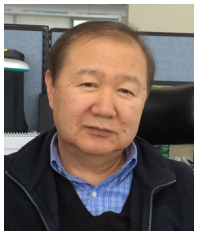

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