Device Performances Related to Gate Leakage Current in Al₂O₃/AlGaN/GaN MISHFETs

Do-Kywn Kim¹, V.Sindhuri¹, Dong-Seok Kim¹, Young-Woo Jo¹, Hee-Sung Kang¹, Young-In Jang¹, In Man Kang¹, Youngho Bae², Sung-Ho Hahm¹, and Jung-Hee Lee¹

Abstract-In this paper, we have characterized the electrical properties related to gate leakage current in AlGaN/GaN MISHFETs with varying the thickness (0 to 10 nm) of Al₂O₃ gate insulator which also serves as a surface protection layer during high-temperature RTP. The sheet resistance of the unprotected TLM pattern after RTP was rapidly increased to 1323 Ω/\Box from the value of 400 Ω/\Box of the as-grown sample due to thermal damage during high temperature RTP. On the other hand, the sheet resistances of the TLM pattern protected with thin Al₂O₃ layer (when its thickness is larger than 5 nm) were slightly decreased after high-temperature RTP since the deposited Al₂O₃ layer effectively neutralizes the acceptor-like states on the surface of AlGaN layer which in turn increases the 2DEG density. AlGaN/GaN MISHFET with 8 nmthick Al₂O₃ gate insulator exhibited extremely low gate leakage current of 10⁻⁹ A/mm, which led to superior device performances such as a very low subthreshold swing (SS) of 80 mV/dec and high Ion/Ioff ratio of $\sim 10^{10}$. The PF emission and FN tunneling models were used to characterize the gate leakage currents of the devices. The device with 5 nm-thick Al₂O₃ layer exhibited both PF emission and FN tunneling at relatively lower gate voltages compared to that with 8 nm-thick Al₂O₃ layer due to thinner

Semiconductors, Seoul in Korea, Feb. 2014.

¹ School of Electronics Engineering, College of IT Engineering, Kyungpook National University, Daegu, 702-701, Korea

² Department of Electronic Engineering, Uiduk University, Gyeongju, 780-713, Korea, 702-701, Korea

780-715, Kolea, 702-701, Kol

E-mail : jlee@ee.knu.ac.kr

 Al_2O_3 layer, as expected. The device with 10 nm-thick Al_2O_3 layer, however, showed very high gate leakage current of 5.5×10^{-4} A/mm due to poly-crystallization of the Al_2O_3 layer during the high-temperature RTP, which led to very poor performances.

Index Terms—Gallium nitride, HFET, thin Al₂O₃ layer, ALD, sheet resistance, gate leakage current

I. INTRODUCTION

AlGaN/GaN heterojunction field-effect transistors (HFETs) have been widely investigated as a very promising device for high-power/frequency applications due to the high two-dimensional electron gas (2DEG) density along with the high electron mobility [1-3]. For better device performance, a thin AlGaN barrier is usually required to suppress the short channel effect and to increase the transconductance of the device, which results in high cutoff frequency $(f_{\rm T})$ and maximum oscillation (f_{max}) frequency [4]. In general, however, the device with thin AlGaN barrier suffers from a large gate leakage current due to various surface damage during subsequent fabrication steps such as plasma or high temperature thermal process. The large gate leakage current of HFET can cause severe device degradation such as high subthreshold swing (SS), low Ion/Ioff ratio, and current dispersion [5, 6]. AlGaN/GaN metalinsulator-semiconductor HFETs (MISHFETs) with appropriate thin gate insulator such as Al₂O₃, SiO₂, or Si₃N₄ layer were therefore investigated to reduce the gate leakage current. The use of thin gate insulator is also required to achieve the high frequency operation ($f_{\rm T}$,

Manuscript received May. 12, 2014; accepted Jul. 30, 2014 A part of this work was presented in Korean Conference on

 f_{max}) for RF devices [7-9]. The Al₂O₃ layer, usually deposited by atomic layer deposition (ALD), has been widely used as a gate dielectric layer among other insulators because it offers high gate capacitance due to relatively high dielectric constant (9.1 eV), high breakdown field (10 MV·cm⁻¹), and large conduction band offset of 2.1 eV with AlGaN layer which ensures low gate leakage current [10-13].

In this work, we have optimized the thickness of the thin Al_2O_3 layer, which can serve as an effective surface protection layer during high-temperature RTP as well as an excellent gate dielectric layer in AlGaN/GaN MISHFETs. The utilization of the thin Al_2O_3 layer simplifies the fabrication of the AlGaN/GaN MISHFET because it does not require removal of the Al_2O_3 protection layer after RTP and re-deposition of the gate dielectric layer.

II. EXPERIMENT

Fig. 1 shows the cross-sectional schematic of the fabricated AlGaN/GaN MISHFET with Al₂O₃ gate dielectric. A 17 nm-thick AlGaN/GaN heterostructure with an electron mobility of 1900 cm²/Vs, sheet electron concentration of 8×10^{12} /cm², and the sheet resistance of 400 Ω/\Box was grown on sapphire (0001) substrate by metal organic chemical vapor deposition (MOCVD).

Firstly, the device isolation was carried out by transformer-coupled-plasma reactive ion etching (TCP-RIE) using a BCl₃/Cl₂ gas mixture. A thin amorphous Al₂O₃ layers, with different thickness of 5, 8, and 10 nm were then deposited with a deposition rate of 0.7 Å/cycle at 450°C using plasma-enhanced atomic layer deposition

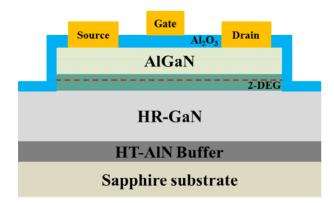


Fig. 1. Schematic structure of AlGaN/GaN MISHFET fabricated with thin Al_2O_3 layer.

(PEALD), which serves as both the surface protection layer during RTP and as gate insulator of the device. The Al₂O₃ layer was patterned to define the source/drain regions and then Si/Ti/Al/Ni/Au (1/25/160/40/100 nm) layers were deposited, followed by two-step RTP at low temperature of 500°C for 20 sec and subsequently at higher temperature of 800°C for 30 sec in N₂ ambient. Finally, Ni/Au (50/50 nm) gate metal was deposited. The gate length and width of the fabricated AlGaN/GaN MISHFETs were 3 and 100 μ m, respectively. After the fabrication of the devices, the electrical properties and device parameters were characterized according to the variation of the thickness of Al₂O₃ layer.

III. RESULTS AND DISCUSSION

The resistance parameters for ohmic contact were extracted by using transmission line method (TLM). The sheet resistance of the device with unprotected AlGaN surface was increased to 1323 Ω/\Box from the value of 400 Ω/\Box , obtained by hall measurement for the as-grown AlGaN/GaN heterostructure. This clearly indicates that the surface of the thin AlGaN layer becomes thermally damaged due to the high temperature exposure during RTP [14, 15], which would create many acceptor-like states on the AlGaN surface and thus decrease the electron density in the 2DEG channel underneath. On the contrary, the sheet resistances of the surface protected devices were not degraded, but rather decreased after high temperature RTP. This is because the thin Al₂O₃ layer not only protects the AlGaN surface during the RTP, but also effectively compensates the acceptor-like states on the surface of AlGaN layer which increases the electron density in the 2DEG channel.

Fig. 2 shows the semi-log transfer characteristics for AlGaN/GaN MISHFETs with different Al₂O₃ thicknesses. The curve with black squares represents the characteristics for the AlGaN/GaN HFET without Al₂O₃ gate insulator, which is reference device. It is noticed that the threshold voltage (V_T) of the device negatively shifts with increasing the thickness of Al₂O₃ layer. The extracted threshold voltages for the devices were also shown in the inset of Fig. 2. The device with 8 nm-thick Al₂O₃ layer clearly demonstrates excellent performances such as very low off-state leakage current (I_{off}) of 6.4 × 10^{-11} A/mm, very low subthreshold swing (SS) of 80

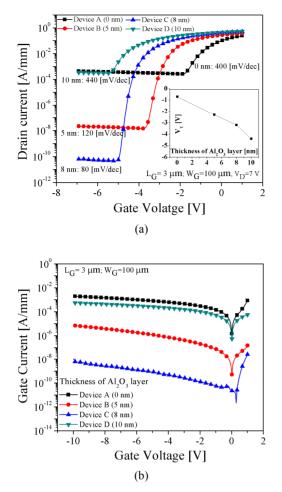


Fig. 2. (a) Log-scale I_D - V_G characteristics according to the thickness of Al_2O_3 layer. The inset shows the threshold voltages with varying the thickness of Al_2O_3 layer, (b) Gate leakage current as functions of gate bias.

mV/dec, and high I_{on}/I_{off} ratio of ~ 10¹⁰, which indicates that 8 nm-thick Al_2O_3 layer is very effective in decreasing both the gate leakage current and the surface leakage current between the gate and the drain which also results in suppressing the off-state surface leakage current. In contrast, the device with 10 nm-thick Al_2O_3 layer exhibits the highest on-state current due to large negative V_T of -4.4 V, but the other performances are very poor such as very low I_{on}/I_{off} ratio of ~ 10³, very high SS of 440 mV/dec, and high off-state leakage current of 3.4×10^{-4} A/mm owing to the high gate leakage current of the device.

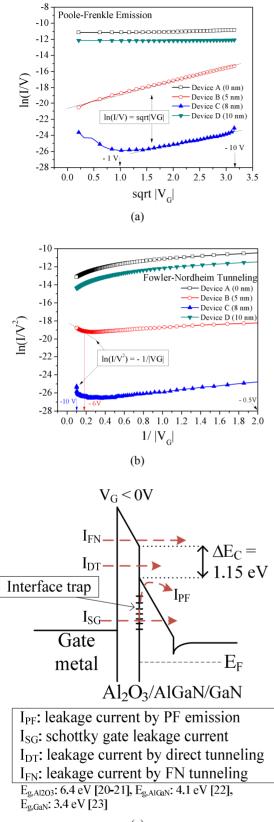
It was found the device performances observed in Fig. 2(a) were strongly related to the gate leakage currents. The device with lower gate leakage current exhibited better device performances as shown in Fig. 2(b). The

Table 1. The parameters extracted from devices

	Device A	Device B	Device C	Device D
Al ₂ O ₃ thickness [nm]	0	5	8	10
$V_{T}[V]$	- 0.7	- 2.3	- 3.2	- 4.4
I _{D,max} at V _D = 7V [mA/mm]	248.6	355.8	513.5	533.7
g _{m,max} [mS/mm]	155	127	129	110
SS [mV/dec]	400.0	120.0	80.0	440.0
I _{on} /I _{off} ratio	10 ³	107	10 ¹⁰	10 ³
I _{D,off} at V _G = - 7 V [A/mm]	4.30E-04	2.20E-08	6.40E-11	3.40E-04
I_G at V_G = - 10 V [A/mm]	1.90E-03	6.90E-06	6.10E-09	5.50E-04

reference HFET device without Al₂O₃ layer showed high gate leakage current of $\sim 2 \times 10^{-3}$ A/mm at V_G = - 10 V, due to typical schottky gate leakage current (I_{SG}) through thin AlGaN barrier and the surface leakage current (I_{SI}) by the surface defect charge [16-18]. The leakage current greatly decreased to $\sim 7 \times 10^{-6}$ A/mm at V_G = - 10 V as the thickness of the Al₂O₃ layer was increased to 5 nm and the current was further decreased to 6.1×10^{-9} A/mm at same gate voltage for the device with 8 nm-thick Al₂O₃ layer. However, the device with 10 nm-thick Al₂O₃ layer showed very high gate leakage current of 5.5×10^{-4} A/mm, similar to the value for the reference HFET device. It is generally known that the ALD Al₂O₃ layer poly-crystallized when the becomes annealing temperature reaches at ~ 850°C [19]. Furthermore, premature poly-crystallization of the layer can be observed even at lower annealing temperature as the thickness of the layer increases. Thus, the unexpected result for the device with 10 nm-thick Al₂O₃ layer is probably due to the poly-crystallization of the Al₂O₃ layer during the RTP which causes large current flow through the grain boundaries of the Al₂O₃ layer to make the layer very leaky. The extracted parameters of all the devices are summarized in Table 1.

Two models, Poole-Frankel (PF) emission, $\ln(I/V) = \sqrt{V}$ and Fowler-Nordheim (FN) tunneling, $\ln(I/V^2) = -(1/V)$, were employed to characterize the gate leakage current of the Al₂O₃ gate insulator with different thickness. Fig. 3(a) shows PF emission plots from the gate leakage currents of the devices with 5 and 8 nm-thick Al₂O₃ layer. PF emission of the device with relatively thin 5 nm-thick Al₂O₃ layer begins from very low gate voltage. This indicates that the electrons emitted from the gate easily tunnel through the thin Al₂O₃ layer to be captured into the interface trap between the Al₂O₃



⁽c)

Fig. 3. (a) Poole-Frankel emission plots, (b) Fowler-Nordheim plots with varying the thickness of Al_2O_3 layer, (c) The schematic model of the gate leakage current of the device.

layer and AlGaN layer, and then the trapped electrons escape from the trap toward the channel to form the gate leakage current (I_{PF}) as a simple band diagram modeled in Fig. 3(c). On the other hand, the device with relatively thick 8 nm-thick Al₂O₃ layer exhibited the PF emission at higher gate voltage larger than - 1 V, which is expected because the thicker gate oxide requires higher gate voltage to supply tunneling electrons to the interface traps. Fig. 3(b) shows FN tunneling plots extracted from the gate leakage currents (I_{FN}) of the devices. The plot may cover the voltage related to the direct tunneling (I_{DT}) , which occurs prior to the FN tunneling. The FN tunneling for the device with 5 nm-thick Al₂O₃ layer begins at the gate voltage of - 6 V. For the device with 8 nm-thick Al₂O₃ layer, the tunneling becomes significant when the gate voltage is larger than - 10 V and the current level is three orders lower in magnitude compared to the value observed in the device with 5 nmthick Al₂O₃ layer, which is also expected from the band diagram in Fig. 3(c), because the thicker oxide needs higher tunneling voltage. Finally, the device with 10 nmthick Al₂O₃ layer showed neither the FN tunneling nor the PF emission since the 10 nm-thick Al₂O₃ layer became poly-crystallized during the high-temperature RTP and the layer lost the insulating properties, which resulted in very similar poor leakage characteristics with the reference device without the Al₂O₃ layer.

IV. CONCLUSIONS

In this work, we have investigated the device performances related to gate leakage current in Al₂O₃/ AlGaN/GaN MISHFETs with varying Al₂O₃ gate insulator thickness. Thin Al₂O₃ layer serves as excellent gate dielectric and the effective surface protection layer during the fabrication of the AlGaN/GaN MISHFET. Models for the PF emission and the FN tunneling were employed to characterize the gate leakage current of the Al₂O₃ gate insulator with different thickness. The devices with 5 and 8-nm Al₂O₃ gate insulator exhibited both the PF emission and the FN tunneling. The device with 8 nm-thick Al₂O₃ gate insulator showed very low gate leakage current of 6.1×10^{-9} A/mm which led to excellent device performances such as SS of 80 mV/dec and I_{on}/I_{off} ratio of $\sim 10^{10}$. However, the device with 10 nm-thick Al₂O₃ layer showed neither the PF emission nor the FN

tunneling, but instead exhibited very large gate leakage current because the Al₂O₃ layer became poly-crystallized during the high-temperature RTP, which led to very poor device performances.

ACKNOWLEDGEMENTS

This work was supported by Kyungpook National University Research Fund 2012, the BK21 Plus funded by the Ministry of Education (21A20131600011), Korea Basic Science Institute (KBSI) and the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2008-0062617, 2011-0016222).

REFERENCES

- V. Kumar, W. Lu, R. Schwindt, A. Kuliev, G. Simin, J. Yang, M.A Khan, and I. Adesida, "AlGaN/GaN HEMTs on SiC With *f_T* of Over 120 GHz", *IEEE Electron Device Letters*, Vol.23, No. 8, pp.455-457, Aug.2002.
- [2] S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, J. W. Palmour, L. T. Kehias, and T. J. Jenkins, "High-Power Microwave GaN/AlGaN HEMT's on Semi-Insulating Silicon Carbide Substrates", *IEEE Electron Device Letters*, Vol.20, No. 4, pp.161-163, April.1999.
- [3] J-H Lee, C. Park, K-S Im, and J-H Lee, "AlGaN/GaN-Based Lateral-Type Schottky Barrier Diode With Very Low Reverse Recovery Charge at High Temperature", *IEEE Transactions On Electron Devices*, Vol.60, No.10, pp.3032-3036, Oct.2013.
- [4] J.W. Chung, W. E. Hoke, E. M. Chumbes, and T. Palacios, "AlGaN/GaN HEMT With 300-GHz f_{max}", *IEEE Electron Device Letters*, Vol. 31, No. 3, pp.195-197, 2010.
- [5] J. W. Chung, J. C. Roberts, E L. Piner, and T. Palacios, "Effect of Gate Leakage in the Subthreshold Characteristics of AlGaN/GaN HEMTs", *IEEE Electron Devices Letters*, Vol.29, No.11,pp.1196-1198, Nov.2008.
- [6] M. V. Hove, S. Boulay, S. R. Bahl, S. Stoffels, X. Kang, D. Wellekens, K. Geens, A. Delabie, and S. Decoutere, "CMOS Process-Compatible High-Power Low-Leakage AlGaN/GaN MISHEMT on

Silicon" *IEEE Electron Devices Letters*, Vol.33, No.5, pp.667-669, Nov.2008.

- [7] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, and V. Sahmuganathan "Improved Linearity for Low-Noise Applications in 0.25-μm GaN MISHEMTs Using ALD Al₂O₃ as Gate Dielectric" *IEEE Electron Devices Letters*, Vol.31, No.8, pp.803-805, Aug.2010.
- [8] Zhi Hong Liu, Geok Ing Ng, Subramaniam Arulkumaran, Ye Kyaw Thu Maung, Khoon Leng Teo, Siew Chuen Foo, Vicknesh Sahmuganathan, Tao Xu, and Chee How Lee "High Microwave-Noise Performance of AlGaN/GaN MISHEMTs on Silicon With Al₂O₃ Gate Insulator Grown by ALD" *IEEE Electron Devices Letters*, Vol.31, No.2, pp.96-98, Feb.2010.
- [9] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, and V. Sahmuganathan "Improved two-dimensional electron gas transport characteristics in AlGaN/GaN metal-insulatorsemiconductor high electron mobility transistor with atomic layer-deposited Al₂O₃ as gate insulator" Applied Physics Letters, Vol.95, 223501, (2009).
- [10] P. D. Ye, B. Yang, K. K. Ng, and J. Bude, G. D. Wilk, S. Halder and J. C. M. Hwang, "GaN metaloxide-semiconductor high-electron-mobilitytransistor with atomic layer deposited Al2O3 as gate dielectric" *Appl. Phys. Lett*, Vol.86, pp. 063501-1-063501-3, Jan. 2005.
- [11] D Gregušova, R Stoklas, K C icco, T Lalinsky and P Kordoš, "AlGaN/GaN metal-oxide-semiconductor heterostructure field-effect transistors with 4 nm thick Al2O3 gate oxide", Semiconductor Science and Technology, Vol.22, pp.947-951, Jun. 2007.
- [12] T. Hashizume, S. Ootomo, and H. Hasegawa, "Suppression of current collapse in insulated gate AlGaN/GaN heterostructure field-effect transistors using ultrathin Al₂O₃ dielectric", *Appl. Phys. Lett*, Vol.83, No.14, pp. 2952-1-2952-4, Oct. 2003.
- [13] H-S Kang, M.S.P Reddy, D-S Kim, K-W Kim, J-B Ha, Y S Lee, H-C Choi and J-H Lee, "Effect of oxygen species on the positive flat-band voltage shift in Al2O3/GaN metal-insulator-semiconductor capacitors with post-deposition annealing ", *Appl. Phys. Lett*, Vol.46, No.14, pp. 155101-1-155101-4, Feb.2013.

- [14] K.SHIOJIMA and N.SHIGEKAWA, "Thermal Stability of Electrical Properties in AlGaN/GaN Heterostructures", *JJAP Lett.*, Vol.43, No.1, pp.100-105, Jan.2004.
- [15] K.SHIOJIMA and N.SHIGEKAWA, "Thermal Stability of Sheet Resistance in AlGaN/GaN 2DEG Structure", *phys. stat. sol Lett*, Vol.0, No.1, pp.397-400, Oct.2002.
- [16] Y.H. Chen, K. Zhang, M.Y.Cao, S.L. Zhao, J.C. Zhang, X. H. Ma, and Y. Hao, "Study of surface leakage current of AlGaN/GaN high electron mobility transistors", *Appl. Phys. Lett*, Vol.104, pp.153509-1-153509-4, April.2014.
- [17] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Influence of Surface Defect Charge at AlGaN–GaN-HEMT Upon Schottky Gate Leakage Current and Breakdown Voltage", *IEEE Transactions On Electron Devices*, Vol.52, No.2, pp.159-164, Feb.2005.
- [18] H. Hasegawa and M. Akazawa, "Current Transport, Fermi Level Pinning, and Transient Behavior of Group-III Nitride Schottky Barriers", *Journal of the Korean Physical Society*, Vol. 55, No.3, pp. 1167-1179, Sept.2009.
- [19] S. Jakschik, U. Schroeder, T. Hechta, M. Gutsche, H. Seidl, Johann W. Barth, "Crystallization behavior of thin ALD-Al₂O₃ films", *Thin Solid Films Letters*, Vol.425, pp. 216-220, Dec. 2003.
- [20] J. Hu, A. Nainani, Y. Sun, K.C. Saraswat, and H.S. Philip Wong, "Impact of fixed charge on metalinsulator-semiconductor barrier height reduction", *Appl. Phys. Lett*, Vol.99, pp. 252104-1-252104-4, Dec.2011.
- [21] N.V. Nguyen, O. A. Kirillov, W. Jiang, W. Wang, J.S. Suehle, P. D. Ye, Y. Xuan, N. Goel, K.W. Choi, W. Tsai, and S. Sayan, "Band offsets of atomiclayer-deposited Al₂O₃ on GaAs and the effects of surface treatment", *Appl. Phys. Lett*, Vol.93, 082105-1-082105-3, Aug. 2008.
- [22] M-W Ha, S-C Lee, J-H Park, K-S Seo and M-K Han, "New Post-Annealing Method for Unpassivated AlGaN/GaN High Electron Mobility Transistors Employing XeCl Excimer Laser Pulses", *Journal of the Korean Physical Society*, Vol.47, S568-S571, Nov.2005.
- [23] S-J Kim, D-H Kim, J-M Kim, K-M Jung and T-G Kim, "Reduction of the Gate Leakage Current in

Binary-trench-insulated Gate AlGaN/GaN Highelectron-mobility Transistors", *Journal of the Korean Physical Society*, Vol.55, pp.356-361, Jul.2009.



Do-Kywn Kim was born in Busan, Korea, in 1982. He received the B.S degree in electronic engineering from Uiduk University, Gyeongju, Korea, in 2009. He worked as an engineer for Semiconductor Education and Research Center from 2008 to 2009.

He received M.S. degree from Kyungpook National University (KNU), Daegu, Korea, in 2012. During his master's course, he was as a visiting researcher to characterize GaN-based devices at IMEP-INPG, France from 2011 to 2012. He is currently a Ph.D. candidate in KNU, and his current research is focused on the characterization of GaN-based electronic devices for RF/Power applications. Furthermore, he has worked as a teaching assistant for semiconductor process education at Institute of Semiconductor Fusion Technology (ISFT) in KNU.



Sindhuri Vodapally is currently pursuing her Ph.D. degree with Kyungpook National University, Daegu, Korea. Her current research interest includes GaN based electronic devices for power applications.



Dong-Seok Kim received the B.S. and M.S. degrees in electronic engineering from Kyungpook National University (KNU), Daegu, in 2008 and 2010, respectively. He is currently working toward the Ph.D. degree in electrical engineering and

computer science from KNU, Daegu, Korea. His current research is focused on the growth of nitride-based materials and the fabrication and characterization of GaN-based electronics



Young-Woo Jo was born in Kyeungsangbuk-Do, Korea, in 1980. He received the B.S degree in electronic and electrical engineering from Yeungnam University, Kyeungsan, Korea, in 2008 and M.S. degree from Kyungpook National University

(KNU), Daegu, Korea, in 2010. He is currently a Ph. D. candidate in KNU. His current research interests include GaN-based electronic devices for RF/Power application and nano-electronic emerging devices.



Hee-Sung Kang received the Master's degree in electrical engineering and computer science from the Kyungpook National University (KNU), Republic of Korea, in 2008, where he is currently working toward the Ph.D. degree in

electronics engineering. His main research interests are in design and fabrication of GaN-based power devices. He has worked as a teaching assistant for semiconductor process education at Institute of Semiconductor Fusion Technology (ISFT) in KNU.



Young-In Jang has been working toward B.S. degree in electrical engineering from the School of Electronics Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2012. His interests include design, fabrication and characterization

of III-V compound transistors.



In Man Kang received the B.S. degree in electronic and electrical engineering from School of Electronics and Electrical Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2001, and the Ph.D. degree in electrical

engineering from School of Electrical Engineering and Computer Science (EECS), Seoul National University (SNU), Seoul, Korea, in 2007. He worked as a teaching assistant for semiconductor process education from 2001 to 2006 at Inter-university Semiconductor Research Center (ISRC) in SNU. From 2007 to 2010, he worked as a senior engineer at Design Technology Team of Samsung Electronics Company. In 2010, he joined KNU as a full-time lecturer of the School of Electronics Engineering (SEE). Now, he has worked as an assistant professor. His current research interests include CMOS RF modeling, silicon nanowire devices, tunneling transistor, low-power nano CMOS, and III-V compound semiconductors. He is a member of IEEE EDS.



Youngho Bae received B.E., M.E., and Ph.D. degrees in electronic engineering from Kyungpook National University in 1984, 1986, and 1993, respectively. From 1987 to 1996, he worked for the RIST, where he worked on advanced Si wafer

technology including SIMOX SOI, and semiconductor power devices. Since 1996, he has been a professor of the department of electronics, Uiduk University in Gyeongju, Korea. He was a visiting professor of IMEP, Grenoble institute of technology, France during 2009-2010, where he worked on electrical characterization of SOI devices and materials. His research interests include electrical characterization of high speed semiconductor device, including SOI MOSFET and GaN FET. He is also interested in radiation effect in semiconductor devices.



Sung-Ho Hahm received the B.S. degree in electronic engineering from Kyungpook National University (KNU), Daegu, in 1985 and received M.S. and Ph.D. degrees in Electronic Engineering from Korea Advanced Institute of Science and Technology

(KAIST) in 1987, and 1991, respectively. From 1992 to 1996, he served Korean Ministry of Trade and Industry as a deputy director for semiconductor industry. Since 1996, he has been a professor at School of Electronics Engineering, College of IT Engineering at KNU. From 2003 to 2004, he visited National University of Singapore as a Teaching Fellow. From 2008 to 2009, he was a chief at National Education Center for Semiconductor Technology (NECST). His current research interests include GaN based UV opto-electronic devices and schottky barrier GaN MOSFET.



Jung-Hee Lee received the B.S. and M.S. degrees in electronic engineering from Kyungpook National University (KNU), Daegu, in 1979 and 1983, respectively, the M.S. degree in electrical and computer engineering from Florida Institute of Technology,

Melbourne, in 1986, and the Ph.D. degree in electrical and computer engineering from North Carolina State University, Raleigh, in 1990. His doctoral research concerned carrier collection and laser properties in monolayer-thick quantum-well heterostructures. From 1990 to 1993, he was with the Compound Semiconductor Research Group, Electronics and Telecommunication Research Institute, Daejeon, Korea. Since 1993, he has been a Professor with the School of Electrical Engineering and Computer Science, KNU, Daegu. He is the author or coauthor of more than 200 publications on semiconductor materials and devices. His current research is focused on the growth of nitride-based epitaxy, the fabrication and characterization of gallium-nitridebased electronic and optoelectronic devices, atomic layer epitaxy for metal-oxide-semiconductor application, and characterizations and analyses for the 3-D devices such as fin-shaped FETs.