Pixel Circuit with Threshold Voltage Compensation using a-IGZO TFT for AMOLED

Jae Pyo Lee, Jun Young Hwang, and Byung Seong Bae

Abstract—A threshold voltage compensation pixel circuit was developed for active-matrix organic light emitting diodes (AMOLEDs) using amorphous indium-gallium-zinc-oxide thin-film transistors (a-IGZO-TFTs). Oxide TFTs are n-channel TFTs; therefore, we developed a circuit for the n-channel TFT characteristics. The proposed pixel circuit was verified and proved by circuit analysis and circuit simulations. The proposed circuit was able to compensate for the threshold voltage variations of the drive TFT in AMOLEDs. The error rate of the OLED current for a threshold voltage change of 3 V was as low as 1.5%.

Index Terms—Active matrix organic light-emitting diode (AMOLED), pixel circuit, threshold voltage

I. INTRODUCTION

Recently, active-matrix organic light-emitting diodes (AMOLEDs) displays, which have advantages in flexible displays, and transparent displays have attracted considerable attention as the next generation flat panel displays because they are thinner, lighter, faster, and more power efficient than active-matrix liquid crystal displays (AMLCDs) [1]. Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) and low-temperature polycrystalline-silicon (LTPS) TFTs are

Manuscript received May. 12, 2014; accepted Aug. 25, 2014 A part of this work was presented in Korean Conference on

Semiconductors, Seoul in Korea, Feb. 2014.

Department of Display Engineering, Hoseo University, Chungnam 336-795, Korea.

E-mail: bsbae3@hoseo.edu

used widely at the backplanes of displays because of their low fabrication cost in the case of the a-Si:H TFTs, and high mobility and stability in LTPS TFTs, respectively [2-4]. Although both backplane technologies are used widely, the threshold voltage of a-Si:H TFTs shifts seriously from their initial value as a result of the electrical stress caused by charge trapping and dangling bond creation. The threshold voltage of LTPS TFTs differs among pixels due to the random distribution of grain boundaries in the polysilicon material, resulting in a non-uniform gray-scale over the display area [5, 6]. Consequently, TFTs based on other semiconductor materials have been evaluated as an alternative approach to realizing reliable, high-resolution and low cost AMOLEDs [7]. First of all, amorphous indium-galliumzinc-oxide (a-IGZO) TFTs have attracted special attention as an alternative to a-Si:H and LTPS TFTs due to the adequate field-effect mobility, high current on-off ratio, low off-current, a low processing temperature, visible transparency, a sharp sub-threshold swing, and potentially better electrical stability, which makes the a-IGZO TFT much more suitable to use in AMOLED displays [8-13]. Although a-IGZO TFTs exhibit excellent device performance, the instability of threshold voltage under gate voltage and light illumination stress remains a major issue for AMOLED pixel circuits using a-IGZO TFTs [14, 15]. Therefore, to compensate for the threshold voltage shifts of the drive TFT, a 2 transistor pixel circuit requires additional control signal lines, capacitors and transistors. Several compensation circuits and driving techniques based on a-IGZO TFTs have already been proposed to achieve good uniformity in displays [16-19]. Many compensation circuits using pchannel TFTs have been developed and used in

AMOLED displays. In addition, p-channel compensation circuits without power (V_{DD}) line have been proposed [20-22].

This paper proposes a threshold voltage compensation pixel circuit consists of six TFTs and one capacitor to produce displays with uniform brightness. The circuit analysis and simulation results showed that the proposed pixel circuit can compensate effectively for both the positive and negative threshold voltage shifts of the drive TFT.

II. PROPOSED PIXEL CIRCUIT AND DRIVING METHOD

Fig. 1 shows a schematic diagram of the proposed pixel circuit with a threshold voltage compensation scheme.

The circuit consists of four control signal lines (SEL1, SEL2, EM, and SCAN[n]), a ground line (V_{SS}), five n-channel switching TFTs (T1, T2, T3, T5, and T6), a n-channel drive TFT (T4), and one storage capacitor (C1).

Fig. 2 presents the driving scheme of the proposed pixel circuit. The proposed pixel circuit has four periods



Fig. 1. Schematic diagram of the proposed pixel circuit.



Fig. 2. Timing diagram of the proposed pixel circuit.

for the threshold voltage compensation of the drive TFT. This study considered the operation of the pixel circuit for the two data levels of V_{DATA_H} and V_{DATA_L} , where V_{DATA_H} is the high voltage of data line and V_{DATA_L} is the low voltage of data line. V_{DATA_H} was applied during the Data Input period and was kept at 0 V. The OLED current was set by the V_{DATA_L} , which was varied according to the required OLED current. The detailed operating principles of the proposed circuit are described as follows and illustrated in Fig. 3.

1. Pre-charging Period

As shown in Fig. 3(a), the aim of the pre-charging period is to store the pre-charging voltage to node B while setting low data voltage (V_{DATA_L}) to node A through T1. In this period, SEL1 and EM are high voltages to settle node B as V_{DD} through T3 and T2 and to discharge node C to the ground voltage (V_{SS}) through T6. SCAN[n] is a high voltage to turn on T1. Therefore, all switching TFTs except for T5 turn on. Because T3 and T4 turn on during in this period, the current flows to the OLED and emits light. However, the period is as short as 5 µs compared to the frame time of 16.7 ms. Therefore, the power consumption by this pre-charge period is negligible.

2. V_{TH} Detecting Period

As shown in Fig. 3(b), SEL1 and SCAN[n] remain a high voltage to keep T1, T2 and T6 turned on. SEL2 maintains a low voltage to turn off T5. Therefore, the voltage at nodes A and C are kept at V_{DATA_L} and V_{SS} , respectively. As the EM voltage becomes low, the charge at node B is discharged through T2, T4 and T6. Therefore, the voltage at node B decreases from V_{DD} to V_{TH_T4} at which T4 turns off, where V_{TH_T4} is the threshold voltage of T4. At the end of this period, the threshold voltage of the drive TFT (T4) is extracted at node B and the voltage at node A and node C is V_{DATA_L} and V_{SS} , respectively.

$$V_A = V_{DATA L}, V_B = V_{TH T4}, V_C = V_{SS}$$
(1)



Fig. 3. Schematic diagram of the proposed pixel circuit at each stage of operation (a) Pre-charging, (b) V_{TH} detecting, (c) Data Input, (d) Emission. The dotted line indicates the closed circuit path and the solid line indicates opened circuit path.

3. Data Input Period

As shown in Fig. 3(c), SEL1 goes to a low voltage to turn off T2 and T6. SEL2 and EM remain a low voltage to turn off T5 and T3, and the SCAN[n] remains a high voltage to turn on T1. The DATA voltage becomes a high voltage (V_{DATA_H}). Successively, the voltage at node A increases from V_{DATA_L} to V_{DATA_H} through T1. In the meantime, the voltage at node B changes from V_{TH_T4} to $V_{TH_T4}+V_{DATA}$ by coupling through C1, where V_{DATA} is different between V_{DATA_H} and V_{DATA_L} . Therefore, after data input, the voltage at nodes A and B are V_{DATA_H} and $V_{TH_T4}+V_{DATA}$, respectively,

$$V_A = V_{DATA H}, V_B = V_{TH T4} + V_{DATA}, V_C = V_{SS}$$
(2)

4. Emission Period

As shown in Fig. 3(d), SEL1 remains a low voltage to turn off T2 and T6. SEL2 and EM become a high voltage to turn on T5 and T3, and SCAN[n] goes to a low voltage to turn off T1. The voltage at node A becomes V_{SS} through T5. Therefore, the voltage at node A maintains the voltage of the previous period because V_{SS} is equal to V_{DATA_H} ($V_{SS} = V_{DATA_H}$). The emission current flows through T3, T4 and the OLED. Node C is connected to the source of T4 and the anode of OLED. The source voltage of T4 becomes V_{OLED} and the gate voltage of T4 is $V_{TH_T4}+V_{DATA}$, where V_{OLED} is the voltage of the OLED. Therefore, the voltage at nodes A, B and C are shown in Eq. (3), and the drain current of T4 can be expressed as Eq. (4).

$$A = V_{SS}, B = V_{TH_{T4}} + V_{DATA}, C = V_{OLED}$$
(3)

$$I_{OLED} = \frac{1}{2} \cdot k \cdot (V_{GS_{T4}} - V_{TH_{T4}})^{2}$$

$$= \frac{1}{2} \cdot k \cdot (V_{TH_{T4}} + V_{DATA} - V_{OLED} - V_{TH_{T4}})^{2}$$
(4)

$$= \frac{1}{2} \cdot k \cdot (V_{DATA} - V_{OLED})^{2}$$

where k is $\mu \cdot C_{OX} W/L$, μ is the field effect mobility of drive TFT T4, C_{OX} is the capacitance per unit area of the gate insulator of drive TFT T4, W is the channel width of drive TFT T4, and L is the channel length of drive TFT T4. Therefore, the OLED current is independent of the threshold voltage of the drive TFT. Consequently, the proposed pixel circuit can effectively compensate for the threshold voltage variation.

III. RESULT AND DISCUSSION

A new novel pixel circuit that can compensate for the threshold voltage variation effectively is proposed. The circuit was verified by circuit analysis in the previous section. In addition to circuit analysis, the circuit simulation was performed to prove the function of the proposed pixel circuit. The mobility and threshold voltage of the IGZO TFT were 5 cm²/Vs and 7 V, respectively. The channel width and length of the switching TFT were 15 and 15 μ m, respectively, and the corresponding values for the drive TFT were 60 and 15 μ m, respectively. The model used in the Smart SPICE was a Rensselaer Polytechnic Institute (RPI) a-Si:H TFT model (level 35). Initially, the model parameters were extracted by fitting carefully to the a-IGZO TFT characteristics.

Fig. 4 shows the gate voltage of the drive TFT for a range of threshold voltages of the drive TFT when the input data voltage changes from -7 V to 0 V. Until the emission period, the gate voltage of the drive TFT changes according to the changes in the threshold voltages, such as 6, 7 and 8 V. As shown in Fig. 4, the sudden drop in the gate voltage of the drive TFT between the Data Input period and Emission period is due to parasitic capacitance between the gate and source nodes of the drive TFT. The change in gate voltage according to the change in threshold voltage shows the successful compensation of the threshold voltage shift of the drive



Fig. 4. Simulation results of the gate voltages of the drive TFT for threshold voltage variations of $V_{TH} = 7 \pm 1$ V.



Fig. 5. Simulation results of the OLED current for threshold voltage variation of $V_{TH} = 7 \pm 1$ V when the input data voltages was changed from -7 V to 0 V.



Fig. 6. Simulation results of the OLED current variations in the proposed circuit for different V_{DATA} and V_{TH} variations ($V_{TH} = 7 \pm 1$ V).

TFT. Fig. 5 shows the simulated OLED current of the proposed pixel circuit with a threshold voltage variation of $V_{TH} = 7 \pm 1$ V when the input data voltages changes from -7 V to 0 V. The deviation of the OLED current of the proposed pixel circuit with a threshold voltage

variation of ± 1 V was less than 4 nA.

Fig. 6 shows the OLED current of the proposed pixel circuit for the different threshold voltages of 7 ± 1 V when the data voltages are changed from 0 to -7 V. The OLED currents increased with decreasing data voltage. The OLED currents for several threshold voltages of the drive TFT were compared. The OLED current variation was small, even for a threshold voltage change from 6 to 8 V. Therefore, Fig. 6 shows the successful compensation for the threshold voltage variation of the drive TFT. The error rate of the OLED current in Fig. 6 is the deviation percentage of the currents at $V_{TH} = 7 \pm 1$ V from the OLED current at V_{TH} = 7 V. The OLED current error rate in the proposed pixel circuit was suppressed to less than 3% for $\triangle V_{TH} = \pm 1$ V of the drive TFT. This is an improved error rate compared to the previous circuit, which showed an error rate of 20 % [23]. The OLED current error rate was defined using the following equation:

Error rate =
$$\frac{I_{OLED}(\Delta V_{TH} = 0) - I_{OLED}(\Delta V_{TH})}{I_{OLED}(\Delta V_{TH} = 0)} \cdot 100\%$$
(4)

Fig. 7 compares the error rate of the OLED current between the conventional circuit (2T1C) and the proposed circuit (6T1C) for different threshold voltages ($\Delta V_{TH} = \pm 3$ V). For a data voltage corresponding to a 1 μ A current to the OLED, the error rate was compared with that of the conventional 2T1C pixel circuit. As



Fig. 7. Comparison of the error rate of the OLED current between the conventional circuit (2T1C) and the proposed circuit (6T1C) as a function of V_{TH} at $I_{OLED} = 1 \ \mu$ A.

shown in Fig. 7, the error rate of the proposed pixel circuit was less than that of the conventional 2T1C pixel circuit. The error rate of the conventional 2T1C pixel circuit was increased by 80% for $\triangle V_{TH} = \pm 3$ V of the drive TFT. On the other hand, the error rate of the proposed pixel circuit was reduced significantly compared to the conventional one. The OLED current error rate in the proposed pixel circuit was suppressed to below 1.5% for $\triangle V_{TH} = \pm 3$ V of the drive TFT at I_{OLED} = 1 μ A. Therefore, the display image quality of the proposed pixel circuit will be more uniform than that of the conventional 2T1C pixel circuit because of the successful compensation of the threshold voltage shift. In the case of a bottom emission structure, the estimated aperture ratio for the proposed circuit was 38.9 % with a sub-pixel size of 107 μ m × 280 μ m. The bottom emission structure emits light through a glass substrate. Therefore, the aperture ratio for light emission is limited by the area of the pixel circuit. On the other hand, the top emission structure emits light to the other side, which enables an increase in emission area regardless of the pixel circuit.

V. CONCLUSIONS

A novel pixel circuit with a-IGZO TFTs was proposed to achieve AMOLEDs with better uniformity. The circuit consists of six TFTs and one capacitor to compensate for the threshold voltage shift. The proposed pixel circuit was verified by circuit analysis and proved by circuit simulations with Smart SPICE. The proposed pixel circuit was found to compensate for the threshold voltage variation much more effectively. The simulation and analytical results showed that the proposed pixel circuit is immune to the threshold voltage variations of the drive TFT, and good brightness uniformity of AMOLED displays can be achieved.

ACKNOWLEDGMENTS

This study was supported by the Academic Research Fund of Hoseo University in 2014 (FRC-2014-0082).

REFERENCES

Y. G. Mo, M. K. Kim, C. K. Kang, J. H. Jeong, Y. S. Park, C. G. Choi, H. D. Kim, and S. S. Kim

"Amorphous Oxide TFT Backplane for Large Size AMOLED TVs," *J. Soc. Inf. Disp.*, Vol.19, No.1, pp.16-20, Jan., 2011.

- [2] S. H. Na, J. H. Shim, M. Y. Kwak, and J. W. Seo, "Fabrication of Charge-pump Active-matrix OLED Display Panel with 64 x 64 Pixels," *J. Info. Disp.*, Vol. 7, No. 1, pp. 35-40, Nov. 2010.
- [3] R. Hattori, "Accuracy of Current Delivery System in Current Source Data-Drivr IC for AM-OLED," *Journal of Semiconductor Technology and Science.*, Vol.4, No.4, pp.269-274, Dec., 2004.
- [4] C. L. Lin, W. Y. Chang and C. C. Hung, "Compensating Pixel Circuit Driving AMOLED Display With a-IGZO TFTs," *IEEE Electron Device Lett.*, Vol.34, No.9, pp.1166-1168, Sep., 2013.
- [5] C. Chen, K. Abe, T. C. Fung, H. Kumomi, and J. Kanicki "Amorphous In-Ga-Zn-O Thin Film Transistor Current-Scaling Pixel Electrode Circuit for Active-Matrix Organic Light-Emitting Displays," *Jpn. J. Appl. Phys.*, Vol.48, pp.03B025-1-03B025-7, Mar., 2009.
- [6] W. J. Wu, L. Zhou, M. Xu, L. R. Zhang, R. H. Yao, and J. B. Peng "An AC Driving Pixel Circuit Compensating for TFTs Threshold-Voltage Shift and OLED Degradation for AMOLED," *J. Disp. Technol.*, Vol.9, No.7, pp.572-576, Jul., 2013.
- [7] C. Chen, K. Abe, H. Kumomi, and J. Kanicki "a-InGaZnO Thin-Film Transistors for AMOLEDs: Electrical stability and Pixel-Circuit Simulation," *J. Soc. Inf. Disp.*, Vol.17, No.6, pp.525-534, Jun., 2009.
- [8] J. S. Lee, S. Chang, S. M. Koo, and S. Y. Lee "High-Performance a-IGZO TFT with ZrO₂ Gate Dielectric Fabricated at Room Temperature," *IEEE Electron Device Lett.*, Vol.31, No.3, pp.225-227, Mar., 2010.
- [9] Y. K. Kim, J. D. Kim, H. K. Lym, S. Y. Kim, H. S. Oh, and K. C. Park, "A Gate Driver Circuit for IGZO TFTs Driven by Two Clock Signals," *J. Info. Disp.*, Vol. 13, No. 4, pp. 179-183, Dec. 2012.
- [10] T. Kamiya, K. Nomura, and H. Hosono "Present status of Amorphous In-Ga-Zn-O Thin-Film Transistors," *Sci. Technol. Adv. Mater.*, Vol.11, No.4, pp.044305-044328, Aug., 2010.
- [11] H. H. Hsieh, H. H. Lu, H. C. Ting, C. S. Chuang, C. Y. Chen, and Y. Lin "Development of IGZO TFTs

and Their Applications to Next-Generation Flat-Panel Displays," *J. Info. Disp.*, Vol. 11, No. 4, pp. 160-164, Dec. 2010.

- [12] C. Yang, X. Chen, J. Zhang, and C. Li "Design of an Amorphous In-Ga-Zn-O TFT Current-Scaling Pixel Driving Circuit for AMOLED with Threshold-voltage Shift Compensating," *Proc. of the 2nd International Conference on Computer Science and Electronics Engineering*, pp.1785-1788, Jan., 2013.
- [13] T. C. Fung, C. S. Chuang, K. Nomura, H. P. Davide Shieh, H. Hosono, and J. Kanicki "Photofield-Effect in Amorphous In-Ga-Zn-O (a-IGZO) Thing-Film Transistors," *J. Info. Disp.*, Vol. 9, No. 4, pp. 21-29, Dec. 2008.
- [14] Y. G. Mo, M. K. Kim, C. K. Kang, J. H. Jeong, and Y. S. Park "Amorphous Oxide TFT Backplane for Large Size AMOLED TVs," J. Soc. Inf. Disp., Vol.19, No.1, pp.16-20, Jan., 2011.
- [15] P. T. Liu, Y. T. Chou, and L. F. Teng "Environment-Dependent Metastability of Passivation-Free Indium Zinc Oxide Thin Film Transistor After Gate Bias Stress," *Appl. Phys. Lett.*, Vol.95, pp.233504-1-233504-3, Dec., 2009.
- [16] I. S. Yang, and O. K. Kwon "Transparent Pixel Circuit with Threshold Voltage Compensation Using ZnO Thin-Film Transistors for Active-Matrix Organic Light Emitting Diode Displays," *Jpn. J. Appl. Phys.*, Vol.48, pp.03B024-1-03B024-5, Mar., 2009.
- [17] Y. C. Kim, J. Kanicki, and H. J. Kim "An a-InGaZnO TFT Pixel Circuit Compensating Threshold Voltage and Mobility Variations in AMOLEDs," J. Disp. Technol., Vol.10, No.5, pp.402-406, May., 2014.
- [18] T. Tanabe, S. Amano, H. Miyake, A. Suzuki, R. Komatsu, J. Koyama, S. Yamazaki, K. Okazaki, M. Katayama, H. Matsukizono, Y. Kanzaki, and T. Matsuo "New Threshold Voltage Compensation Pixel Circuits in 13.5-inch Quad Full High Definition OLED Display of Crystalline In-Ga-Zn-Oxide FETs," *SID Int. Symp. Dig. Tech. Pap.*, Vol.43, pp.88-91, Jun., 2012.
- [19] C. Chen, J. Kanicki, K. Abe, and H. Kumomi "AM-OLED Pixel Circuits Based on a-InGaZnO thin film transistors," *SID Int. Symp. Dig. Tech. Pap.*, Vol.40, pp.1128-1131, Jun., 2009.

- [20] W. J. Nam, J. H. Lee, C. Y. Kim, H. J. Lee, and M. K. Han "High-Aperture Pixel Design Employing V_{DD} Line Elimination for Active Matrix Organic Light Emitting Diode Display," *Jpn. J. Appl. Phys.*, Vol.45, No.4A, pp.2433-2436, Apr., 2006.
- [21] S. P. Hong, D. S. Moon, B. S. Bae "Characterization of AMOLED Pixel Circuit Without Power Line," *Analog Integr. Circuits Signal Process.*, Vol.70, No.1, pp.157-162, Jan., 2012.
- [22] J. P. Lee, H. S. Jeon, D. S. Moon, and B. S. Bae "Threshold Voltage and IR Drop Compensation of an AMOLED Pixel Circuit Without a V_{DD} Line," *IEEE Electron Device Lett.*, Vol.35, No.1, pp.72-74, Jun., 2014.
- [23] H. S. Jung, Y. C. Kim, Y. S. Kim, C. Chen, J. Kanicki, and H. J. Lee "a-IGZO TFT Based Pixel Circuits for AM-OLED Displays," *SID Int. Symp. Dig. Tech. Pap.*, Vol.43, pp.1097-1100, Jun., 2012.



Jae Pyo Lee received his B.S. degree in digital display engineering from Hoseo University, Asan, Korea, in 2013 and is currently working toward a M.S. degree in display engineering at Hoseo University, Asan, Korea, in 2013. His research interests include

analog circuit design, integrated circuit design for AMOLED applications.



Jun Young Hwang received his B.S. degree in digital display engineering from Hoseo University, Asan, Korea, in 2014 and is currently working toward a M.S. degree at the display engineering from Hoseo University,

Asan, Korea, in 2014. His research interests include lenticular lens LC, and oxide pixel circuit design for AMOLED applications.



Byung Seong Bae received his B. S. degree in atomic nuclear engineering from Seoul National University, Seoul, Korea, in 1984 and M. S. and Ph. D. degrees in applied physics from the Korea Advanced Institute of Science and Technology, Seoul,

Korea, in 1986, and 1991, respectively. Between 1991 and 1998, he worked at Samsung Electronics on the development of amorphous and poly-silicon TFT LCDs with an integrated driver. From 1999 to 2003, he set up the high-temperature poly-silicon TFT LCD factory and developed micro-display for projection displays at ILJIN Display. Since 2006, he has been a Professor, New IT Engineering College of Hoseo University, Asan, Korea.