Characterization of Dielectric Relaxation and Reliability of High-k MIM Capacitor Under Constant Voltage Stress

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Abstract—**In this paper, the dielectric relaxation and reliability of high capacitance density metal-insulator-metal (MIM) capacitors using Al_2O_3-HfO_2-Al_2O_3 and SiO_2-HfO_2-SiO_2 sandwiched structure under constant voltage stress (CVS) are characterized. These results indicate that although the multilayer MIM capacitor provides high capacitance density and low dissipation factor at room temperature, it induces greater dielectric relaxation level (in ppm). It is also shown that dielectric relaxation increases and leakage current decreases as functions of stress time under CVS, because of the charge trapping effect in the high-k dielectric.**

Index Terms—**MIM (Metal-Insulator-Metal), AHA (Al_2O_3-HfO_2-Al_2O_3), SHS (SiO_2-HfO_2-SiO_2), charge trapping effect, dielectric relaxation**

I. INTRODUCTION

Metal-Insulator-Metal (MIM) capacitors are widely used for in integrated circuit applications, such as analog-to-digital (A/D) converters, digital-to-analog (D/A) converters, and resonators, due to their low parasitic capacitance, and low series resistance [1, 2]. Recently, the MIM capacitors have generated great attention in silicon integrated circuit (IC) applications as passive components, because the total area of passive devices, capacitors in particular, usually consumes a large portion of the whole chip size. Therefore, MIM capacitors with a high capacitance density have been required in order to increase the circuit density and reduce the system cost [3]. Silicon dioxide (SiO_2 , ~3.9) and silicon nitride (Si_3N_4, ~7) are commonly used as insulator materials in conventional MIM capacitors. Although these conventional dielectric materials have good voltage linearity and low temperature coefficients, their capacitance density has been limited, owing to their low dielectric constant. Achieving high capacitance density by reducing the thickness of conventional dielectric materials, silicon dioxide (SiO_2) and silicon nitride (Si_3N_4), has led to high leakage current and reliability issues [4]. Therefore, the use of high-k dielectric materials, such as HfO_2 (~25), Al_2O_3 (~9), ZrO_2 (~20), Ta_2O_5 (~25), and TiO_2 (~80), is necessary to increase the capacitance density and reduce the leakage current. Due to outstanding properties, such as high capacitance density, good thermal stability, and high band gap, hafnium-oxide based MIM capacitors are widely used for next generation capacitors [5]. However, MIM capacitor with single high-k dielectric shows high leakage current. In the last few years, laminate or sandwiched structures of MIM capacitor by adding Al_2O_3 or SiO_2 layers have been studied to reduce the leakage current. However, it is known that MIM capacitors with high-k dielectric have many defects in the metal-insulator interface, which implies that the injected charges in the interface of high-k dielectric induce greater change of capacitor characteristics than those in the interface of conventional

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dielectric materials do [6]. These cause a large dependence of capacitance performance on applied voltage and temperature. Also, it is shown that performance of MIM capacitors degrades by electrical stress [7]. Dielectric relaxation (DR) is one of the related phenomena, due to the trapping and de-trapping mechanism in the high-k dielectric [8]. DR can degrade the performance, like analogue and digital converters (ADC) and voltage controlled oscillators (VCO) linearity [9]. However, there has been little study of electric stress associated with DR.

In this paper, reliability and dielectric relaxation of MIM capacitors, in particular, of advanced capacitors with Al_2O_3- HfO_2- Al2O3 (AHA) and SiO_2-HfO_2-SiO_2 (SHS) sandwiched structure are analyzed under constant voltage stress (CVS).

II. EXPERIMENT

Fig. 1 shows the process flow by which the MIM capacitors used in this experiment were fabricated, with sandwiched dielectric structure of Al_2O_3/HfO_2/Al_2O_3 and SiO_2/HfO_2/SiO_2. MIM capacitors were fabricated on 8-inch p-type silicon substrates. TiN layer was used as the bottom electrode. After that, the stacked dielectric layers with Al_2O_3 (2 nm), HfO_2 (11 nm), and Al_2O_3 (2 nm) and SiO_2 (3 nm), HfO_2 (4 nm), and SiO_2 (3 nm) were sequentially deposited using the atomic layer deposition (ALD) method at 300℃. Finally, TiN layer was deposited and patterned, to form the top electrode.

A conventional MIM capacitor with Si_3N_4 was also fabricated using PE-CVD method for comparison. An Al-Cu layer was used as the bottom electrode and a TiN layer was used as the top electrode.

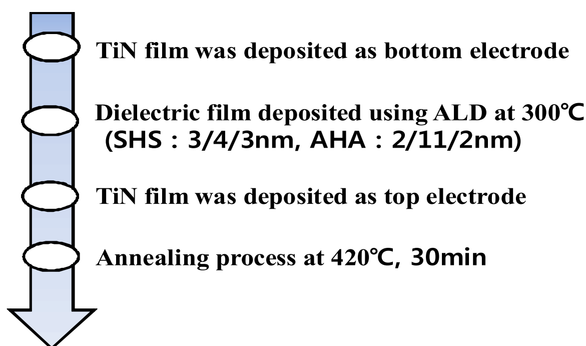
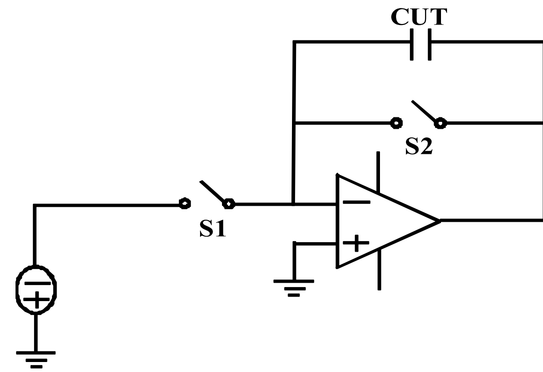
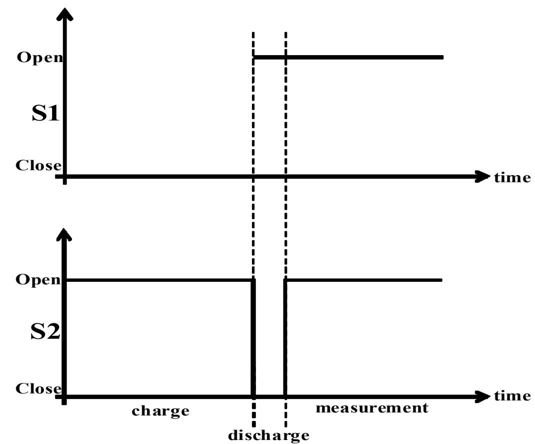


Fig. 1. Process flow for fabrication of MIM capacitor with sandwiched structure.



(a)



(b)

Fig. 2. (a) Measurement system of dielectric relaxation characteristic for MIM capacitor, (b) timing diagram of the switches.

CVS is applied using an Agilent 4156C semiconductor parameter analyzer. The DR characteristic was evaluated using the measurement system shown in Fig. 2(a). Fig. 2(b) shows the clock signals applied to switches for measurement of dielectric relazation. In the charge period, switch 1 is closed and switch 2 is opened. During the discharge period, switch 1 is opened and switch 2 is closed, vice versa. Finally, in the measurement period, switch 1 and switch 2 are opened.

III. RESULT AND DISCUSSION

DR is a carrier absorption/relaxation phenomenon between the electrodes and the interface of dielectric. There are two methods to measure DR characteristic in the time domain. One is the “recovery voltage” technique [10] and the other is the “discharge current” method [11]. For the accurate evaluation of DR characteristic, we used

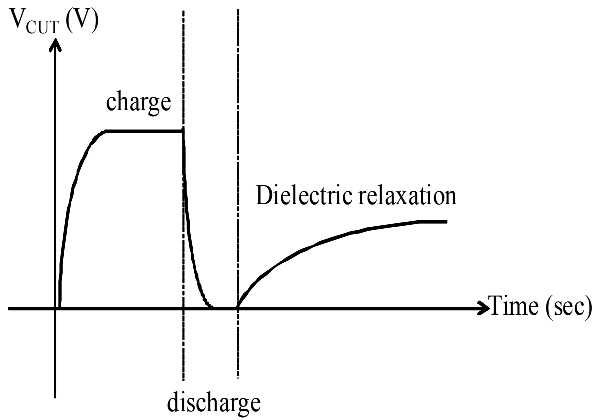


Fig. 3. Normalized voltage across the MIM capacitor during measurement of dielectric relaxation.

the first method. Fig. 3 shows the change of capacitor voltage with measurement time. The positive recovery voltage is measured from negative voltage potential because the charging voltage is applied to the bottom electrode. The top plate may be grounded or left floating, and the bottom plate may be grounded or being charged. Capacitor is charged for a long time then momentarily shorted the capacitor for a short time. Finally, the capacitor remained floating state and the voltage at the terminals is measured over time.

At a given applied charging voltage, traps in the interface of the dielectric become gradually filled over time. Due to the detrapped charged from these trap sites in the dielectric, the voltage of the capacitor rises slowly after the floating period.

Fig. 4 shows the dielectric relaxation level (in ppm), with various dielectric materials of the MIM capacitor. It shows that MIM capacitor with high-k dielectric has a higher DR level than that with a conventional dielectric material, because the high-k dielectrics have more traps in the dielectric than conventional dielectric materials, such as SiO_2, and Si_3N_4.

Fig. 5 shows the increase of DR value after CVS for 2000 sec. We applied the same effective electric field (E_{eff}) to the MIM capacitors for an accurate comparison of the dielectric relaxation characteristics. We normalized the thickness of the dielectric layer in terms of HfO_2 equivalent as defined below. Therefore, the normalized thicknesses (t_{eff}) are defined as (1) and (2).

$$t_{eff.AHA} = t_{HfO_2} + \frac{\varepsilon_{HfO_2}}{\varepsilon_{Al_2O_3}} t_{Al_2O_3} \quad (1)$$

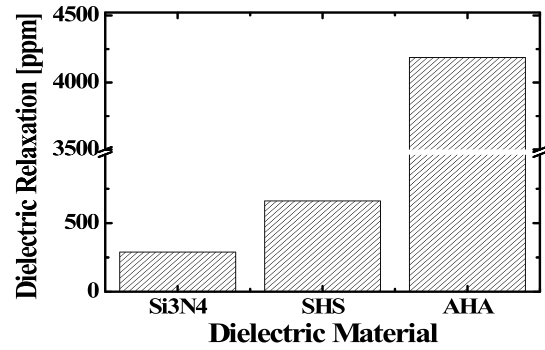
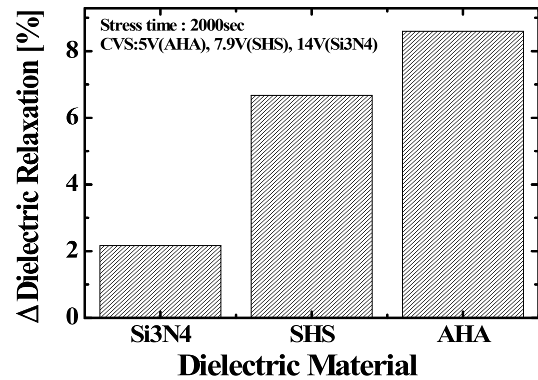
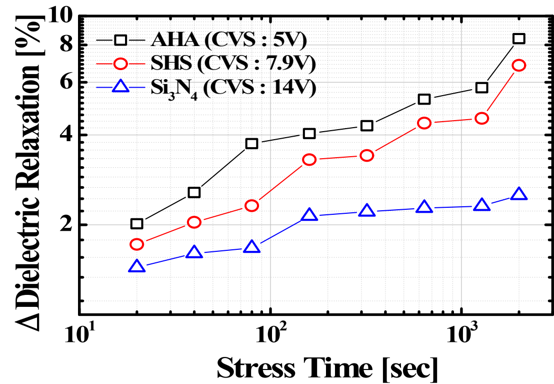


Fig. 4. Dielectric relaxation characteristic of the MIM capacitor with dielectric material.



(a)



(b)

Fig. 5. Time evolution of dielectric relaxation under CVS according to the dielectric material (a) during 2000 sec, (b) like NBTI stressing for 2000 sec.

$$t_{eff.SHS} = t_{HfO_2} + \frac{\varepsilon_{HfO_2}}{\varepsilon_{SiO_2}} t_{SiO_2} \quad (2)$$

Then, the effective electric field is defined as (3).

$$E_{eff} \equiv \frac{V_{AHA}}{t_{eff.AHA}} = \frac{V_{SHS}}{t_{eff.SHS}} = \frac{V_{Si_3N_4}}{t_{eff.Si_3N_4}} \quad (3)$$

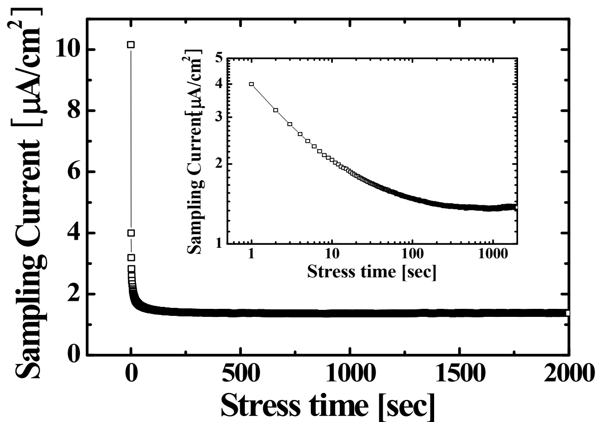


Fig. 6. Characteristic of leakage current with stress time under CVS.

The applied voltage for CVS of AHA, SHS, and Si_3N_4 dielectrics were 5V, 7.9V, and 14V, respectively. Fig. 5 indicates that the high-k dielectrics show a great increase of DR than conventional dielectric material. The largest variation of DR occurs in the AHA structure. This is because HfO_2 has the largest prefactor among the various high-k dielectric materials, related to the charge losses in DRAMs and V_T-shift in MOSFETs [12]. Figs. 5(a) and (b) show a similar increase in DR value.

Fig. 6 shows that the leakage current decreases during CVS for SHS structure. It is caused by the generation of traps and electron trapping in the dielectric. At the initial state under CVS, the reduction of leakage is great, because the generation of traps occurs mainly near the interface of dielectric and the electrode. Figs. 5 and 6 indicate that the charge trapping effect with CVS causes the variation of dielectric relaxation value.

IV. CONCLUSIONS

In this paper, we analyzed the dielectric relaxation characteristics and reliability of MIM capacitors with $Al_2O_3/HfO_2/Al_2O_3$ and SiO2/HfO_2/SiO_2 sandwiched structures under constant voltage stress. It is shown that a MIM capacitor with high-k dielectric has a higher dielectric relaxation (DR) level, and greater increase of DR value uncer constant voltage stree (CVS) than does conventional dielectric material. The leakage current decreases with stress-time under CVS. The charge trapping effect in the dielectric contributes to the variation of the variation of the capacitor parameters.

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