Programming Characteristics on Three-Dimensional NAND Flash Structure Using Edge Fringing Field Effect

Hyung Jun Yang and Yun-heub Song

Abstract—**The three-dimensional (3-D) NAND flash structure with fully charge storage using edge fringing field effect is presented, and its programming characteristic is evaluated. We successfully confirmed that this structure using fringing field effect provides good program characteristics showing sufficient threshold voltage (V_T) margin by technology computer-aided design (TCAD) simulation. From the simulation results, we expect that program speed characteristics of proposed structure have competitive compared to other 3D NAND flash structure. Moreover, it is estimated that this structural feature using edge fringing field effect gives better design scalability compared to the conventional 3D NAND flash structures by scaling of the hole size for the vertical channel. As a result, the proposed structure is one of the candidates of Terabit 3D vertical NAND flash cell with lower bit cost and design scalability.**

Index Terms—**Novel 3D NAND flash structure, edge fringing field effect, scalability**

I. INTRODUCTION

Recently, various 3D NAND flash memory have been suggested to maintain a trend of increasing bit density and reducing bit cost [1-7]. Especially, 3D NAND flash memory with vertical channel type such as BiCS(bit-cost scalable), P-BiCS(Piped-shaped Bit-cost scalable), TCAT(Terabit Cell Array Transistor) and DC-SF(Dual Control gate with Surrounding Floating gate) are widely studied as the promising candidates for the replacement of conventional 2D NAND flash [1-4]. However, some issues are still present in 3D NAND flash structure with vertical channel type. First above all, the BiCS flash cell has much simpler process as compared to the other 3D NAND flash structures but the N+ source junction at the bottom of the channel hole is damaged by thermal budget because of the "gate first" process [1]. Although the P-BiCS developed to improve critical issues of the BiCS, this structure require to complicated pipeline process [2]. Meanwhile, the TCAT with gate-last process and the DC-SF with surrounding FG provide better cell characteristic. However, both structures have still complicated process [3, 4]. Moreover, most of them are not optimal in terms of bit density and bit cost, because of process issues such as the pipeline process, word line separation, and grain boundary limitation. In addition, minimum cell size is limited by the hole for the vertical channel with Poly-Si channel and surrounded ONO [8]. In this paper, we propose a scalable 3D NAND flash structure using fringing field in order to overcome scalability issues of conventional 3D NAND structures. Also, the programming characteristics using edge fringing effect are evaluated by TCAD simulation and discussed for the memory operation. Furthermore, we compared the scalability of the proposed structure with several 3D NAND structures. From these results, we expect that the proposed structure is one of scaling solutions for 3D NAND flash structure.

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Department of Electronic Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : yhsong2008@hanyang.ac.kr

II. A Scalable 3D NAND Flash Structure Using Edge Fringing Field

3D NAND flash structures with vertical channel type are facing to limitation of the hole size for the vertical channel because the effective thickness of O/N/O is estimated to be around 20 nm for a better cell characteristic, and the minimal poly-Si channel diameter is 10 nm for a reliable read current security, then the effective minimum hole size for the vertical channel can be estimated to 50 nm [5]. Therefore, in order to overcome a scalability of current 3D NAND Flash structures with vertical channel type, we investigated a scalable 3D NAND structure using fringing field. Fig. 1 shows the comparison of charge storage region for various 3D NAND cells with vertical channel type. As shown in Fig. 1(a), we expect that the minimum hole size for the vertical channel of BiCS and P-BiCS structure should be limited because the charge storage region is formed in the hole for the vertical channel. In TCAT and DC-SF, Although the charge storage region of both structure is not formed in the hole for the vertical channel, gate region should be larger than BiCS and P-BiCS because ONO(charge-trapping stack) layer and IPD(inter-poly dielectric stack) layer are included in gate region, respectively [3, 4]. However, as shown in Fig. 1(d), the proposed structure can be simultaneously reduce the hole size for the vertical channel and gate region because horizontal thin ONO layers through simple process step such as ALD (Atomic Layer Deposition) process can be easily formed in between two wordlines. Fig. 2(a) shows the cross sectional schematic of the proposed 3D NAND flash structure. One charge trap layer is controlled by edge fringing field of adjacent two control gates (CGs).

The Bird's eye view of the proposed structure is illustrated in Fig. 2(b), showing that the surrounding charge storage is covered by two block oxide layers. Program efficiency is enlarged by edge fringing field between two CGs and it is also enable to operate low bias condition. Fig. 2(c) shows the bias condition for program and erase operation of the proposed structure. The program operation method is achieved by the fringing field from two selected control gate and then erase method is same as conventional bulk erase operation.

The fabrication sequence is briefly as showed in Fig. 3.

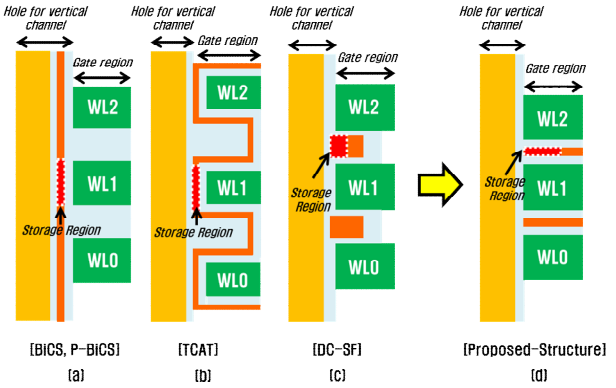

Fig. 1. The comparison of charge storage region between (a)-(c) various 3D NAND cells with vertical channel type, (d) proposed structure.

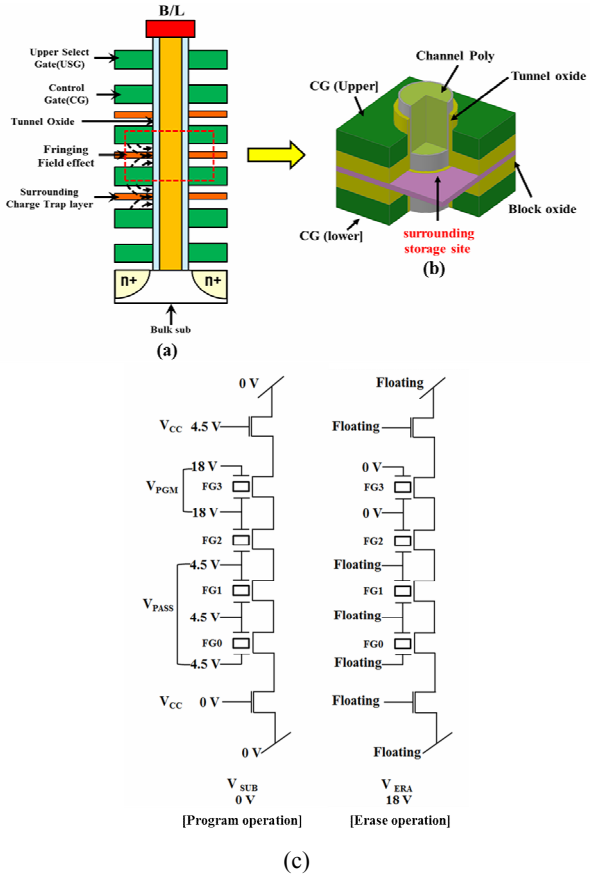

Fig. 2. The (a) cross section schematic, (b) Bird's eye view of proposed 3D NAND flash structure, (c) bias condition for program and erase operation.

The sequential fabrication process is follows; (a) Formation of high doping source line, (b) deposition of insulator and poly-Si electrode for LSG(lower select gate) transistor, (c) repetitive deposition of ONO layer and control gate after lower select gate formation, (d) the

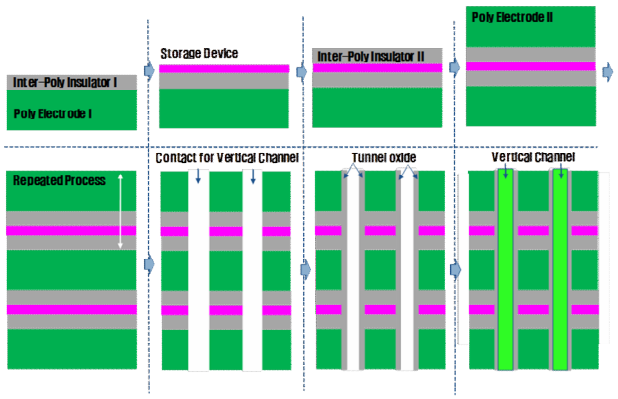

Fig. 3. The fabrication sequence for the proposed structure.

hole for the vertical channel etch for vertical channel formation, (e) deposition of tunnel oxide and (f) deposition of vertical channel. As shown in this figure, Process sequence of the proposed structure has more simple process step than competitive to P-BiCS [2] and TCAT [3] and DC-SF [4]. Thus, we can be expect that by increasing the number of stacking layers, this structure has considerable advantage in terms of bit cost and bit density compared to the conventional 3D NAND structures.

III. Results and Discussion

Structure parameters used during the TCAD simulation are channel hole diameter, tunnel oxide, and thickness of horizontal oxide/nitride/oxide (O/N/O) layers, which are 30 nm, 4 nm, and 10/10/10 nm between two CGs, respectively. The cell gate length is 30 nm. Boron doping concentration of bulk is 1×10^{15} atoms/cm^3 for sufficient hole supply in vertical channel region. The process key parameters summarized in Tabel 1. In order to evaluate the characteristics of the proposed 3D NAND structure, we performed 3D TCAD simulation using cylindrical coordinates for vertical direction. We adjusted the simulation model parameter for cylindrical SONOS device to secure the accurate characteristics of proposed 3D NAND structure and modified parameter such as effective mass for barrier tunneling, total trap density and capture cross section(CCS) as shown in Table 2 [9]. For the device simulation operation, bias conditions of the proposed 3D NAND structure are shown in Fig. 2(c). Fig. 4 shows Id-Vg characteristic of the program when the block oxide thickness is 10 nm. We confirmed that

Table 1. Process key parameter of proposed structure.

Material and Physical dimensions	
Channel material	P-type Poly-Si
channel diameter	30 nm
Gate material	P-type Poly-Si
Gate length	30 nm
Block oxide thickness	10, 20, 30 nm
Tunnel oxide thickness	4 nm
Nitride thickness	10 nm
Optimal doping concentration	
Gate electrode	1×10^{20}/cm^3(Boron)
Channel	Un-doped
Bulk electrode	1×10^{20}/cm^3(Boron)
Source/Drain	1×10^{20}/cm^3(Phosphorus)

Table 2. Optimized simulation physical parameters of proposed structure.

Simulation physical parameter	
Effective mass in nitride	$0.36m_0$
Effective mass in oxide	$0.42m_0$
Effective mass in poly-Si	$0.32m_0$
Oxide dielectric constant	3.9
Nitride dielectric constant	7.5
Capture Cross Section (CCS)	1×10^{-14} cm^{-2}
Trap density (N_T)	5×10^{19} cm^{-3}
Trap energy level(E_T)	1.2 eV

trapped electrons in nitride layer is changed by changing in programming pulse width as shown in Fig. 4(b) in TCAD simulation, and the program V_T was about 5 V during the program voltage of 18 V at 1 ms.

We also performed TCAD simulation for variation of block oxide thickness to investigate program efficiency as shown Figs. 5(a) and (b). As the block oxide thickness increases, program V_T decreases due to lowering the fringing field between adjacent CGs proportionally to block oxide thickness. According to the simulation results, with varying oxide thickness between nitride and control gate to 10 nm / 20 nm / 30 nm, program V_T are 5 V / 2.8 V / 1.8 V each as shown in Fig. 5(a). Therefore, proposed structure requires appropriate block oxide thickness in order to retain similar program V_T compared to conventional 3D NAND flash memory characteristics [1-4].

From the result, we confirmed that program V_T is about 5 V at 1 ms under a bias of V_G = 18 V when the ONO thickness is 10 nm / 10 nm / 10 nm, which is

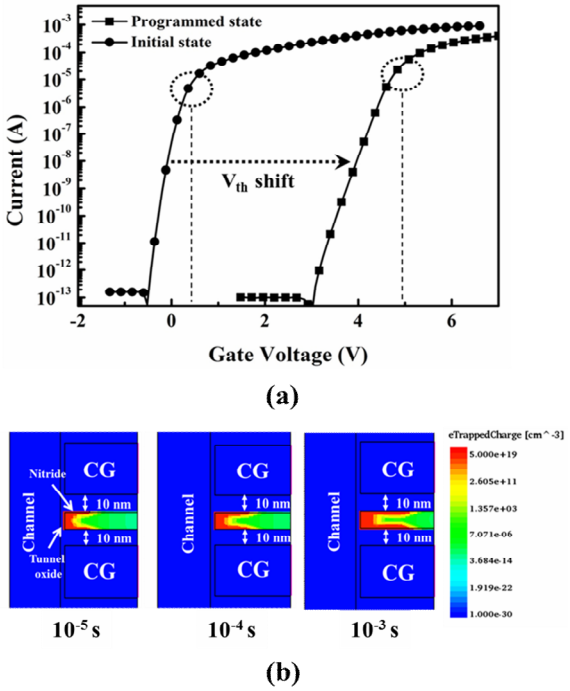

Fig. 4. (a) The program characteristics of during the program operation when O(10)/N(10)/O(10), (b) The program efficiency for O(10)/N(10)/O(10) sample and the status of stored electron depending on programming time.

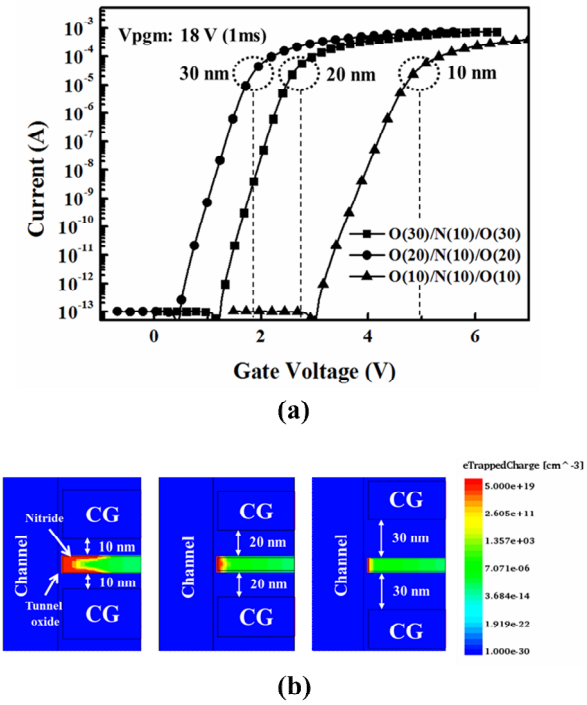

Fig. 5. (a) The effect of program V_T for variation of oxide thickness between nitride and control gate, (b) the simulation result for electron storage.

competitive to the cell characteristics of conventional-3D NAND structures. Furthermore, we generated typical

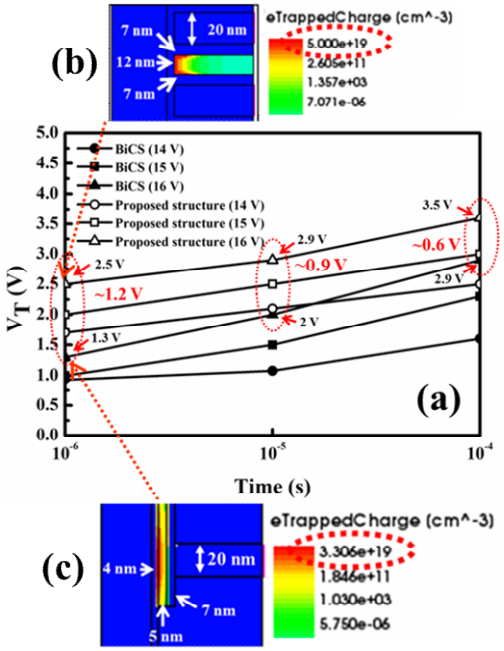

Fig. 6. (a) Program speed characteristics for BiCS and our proposed structure at 1 us, 10 us and 100 us when programming voltage are 14, 15 and 16 V, (b) the simulation result for electron trap density of proposed structure at 1 us, (c) the simulation result for electron trap density of BiCS at 1 us.

BiCS structure in the TCAD simulation in order to compare proposed structure with BiCS having similar physical parameters such as tunnel oxide and block oxide as shown in Figs. 6(b) and (c) for program speed characteristics and simulated by setting the same trap density of BiCS and proposed structure which is 5 x 10^{-19} cm^{-3} for more accurate comparison in the TCAD tool. Fig. 6(a) shows program characteristics and program speed characteristics for proposed structure and BiCS from 1 to 100 us for 14, 15 and 16 V. We confirmed that threshold voltage difference between proposed structure and BiCS are about 1.2 V, 0.9 V and 0.6 V at 10^{-6}, 10^{-5} and 10^{-4} sec, respectively. Also, Comparing proposed structure and BiCS with same gate length and programming voltage, the amount of electron trap charge in silicon nitride of BiCS determined by electric field induced by one control gate, but the amount of electron trap charge in silicon nitride of proposed structure determined by edge fringing field between two control gates Therefore, the amount of electron trap charge is greater than BiCS due to edge fringing field between two control gates as shown in Figs. 6(b) and (c). Thus, initial threshold voltage of proposed structure is about 1.2 V

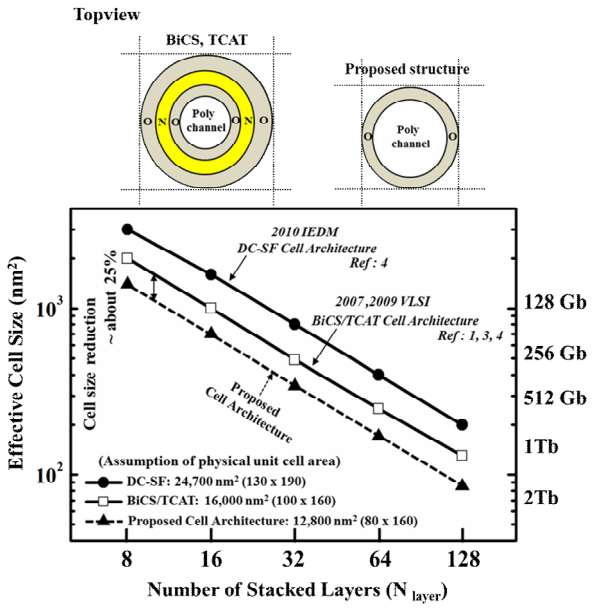

Fig. 7. The comparison of effective cell sizes between proposed structure and conventional 3D NAND flash cells considering scalability.

larger than BiCS. Although threshold voltage increment is slightly smaller than BiCS according to change programming pulse width from 1 to 100 us, since initial threshold voltage of proposed structure is larger than BiCS, we expect that proposed structure relatively reduce programming voltage compared to BiCS assuming proposed structure and BiCS have same trap parameters.

We compared proposed structure with conventional 3D NAND flash structures in terms of the cell size. Effective cell size is estimated and plotted as a function of number of stacked cells as shown in Fig. 7. Proposed structure is assumed to have smaller effective cell size compared to conventional-3D NAND flash structures (BiCS, TCAT, DC-SF), since horizontal ONO layer structure reduces the hole size for the vertical channel. From the result, we confirmed that proposed structure can significantly decrease the number of stacked cells compared to conventional-3D NAND flash structures.

IV. Conclusion

We have proposed the scalable 3D NAND Flash structure using fringing field. It has been successfully simulated by TCAD and the simulation result shows satisfactory program characteristics. We compared similar BiCS and proposed structure for program speed characteristics in the TCAD simulation. From the simulation results, we confirmed that proposed structure relatively reduce programming voltage compared to BiCS. Furthermore, we compared proposed structure and conventional 3D NAND flash structure in terms of bit density with the number of stacked cells. We confirmed that it can realize considerable advantages in terms of bit density. As a result, the proposed 3D NAND flash structure could be a promising candidate for the scalable 3D NAND flash memory architecture.

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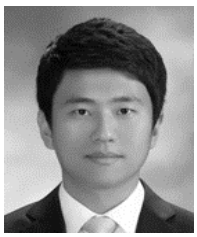

Hyung-Jun Yang received the B.S. degrees in electronics engineering from Hongik University, Seoul, South Korea, in 2010. He is currently pursuing the Ph.D. the M.S. degree in electronics engineering from Hanyang University, Seoul, South Korea, in 2012. His current research interests include 3D GAA SONOS-type memory device modeling and 3D NAND flash architecture.

Yun-heub Song received the B.S. degree in electronics engineering from Kyungpook National University, Daegu, South Korea, in 1984, the M.S. degree in electronics engineering from Hanyang University, Seoul, South Korea, in 1992 and the Ph.D. degree in electrical engineering from Tohoku University, Sendai, Japan in 1999. In 1983, he was with Samsung Electronics Corporation, Ltd., Hwasung, South Korea, where he has been involved in process integration for erasable programmable read-only memory. From 1989 to 1995, he was a Technical Leader for process integration for low-power SRAM and CPU devices. After he received the Ph.D. degree in 1999, he rejoined Samsung Electronics Corporation, Ltd. and worked as a Project Manager (1999-2007) and a Vice President (2007-2008) for the process integration and device development for Flash memory in the Semiconductor R&D Center. In 2008, he joined Hanyang University as an Associate Professor, and became a Professor of department of Electronics and Computer Engineering, Hanyang University in 2014. He is the author of more than 25 articles and more than 40 inventions. His research interests include 3D crossbar array architecture, selective device, switching device, MTJ reliability for STT-MRAM, 3D-Vertical NAND Flash, 3D-PCRAM with synapse, CMOS logic device, biosensor, controlling surface tension, etc.