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A CMOS Stacked-FET Power Amplifier Using PMOS Linearizer with Improved AM-PM

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Abstract

A linear stacked field-effect transistor (FET) power amplifier (PA) is implemented using a 0.18-μm silicon-on-insulator CMOS process for W-CDMA handset applications. Phase distortion by the nonlinear gate-source capacitance (C_{gs}) of the common-source transistor, which is one of the major nonlinear sources for intermodulation distortion, is compensated by employing a PMOS linearizer with improved AM-PM. The linearizer is used at the gate of the driver-stage instead of main-stage transistor, thereby avoiding excessive capacitance loading while compensating the AM-PM distortions of both stages. The fabricated 836.5 MHz linear PA module shows an adjacent channel leakage ratio better than —40 dBc up to the rated linear output power of 27.1 dBm, and power-added efficiency of 45.6% at 27.1 dBm without digital pre-distortion.

Key Words: CMOS, Linear, Power Amplifier (PA), Stacked-FET, W-CDMA

I. INTRODUCTION

Power amplifier (PA) is a key component in mobile handsets, but designing PA is still challenging because high efficiency as well as high linearity is demanded without any compromise for 3G/4G mobile standard applications. For this reason, high performance devices, such as GaAs HBT/HEMT, have mostly been employed for commercial PA fabrication. On the other hand, the CMOS PA has been widely researched to take advantage of its low cost and high integration capability. The weaknesses of the CMOS device/process (e.g., low breakdown voltage and no substrate via hole to the ground) have been overcome by using power combining techniques such as the stacked field-effect transistor (FET) and transformer-based differential cascode structures. Watt-level power amplification has thus been achieved in recent years [1−3]. However, the nonlinear characteristics of the CMOS device have prevented the CMOS PA from being used in actual 3G/4G handset PA applications where stringent linearity is required.

To enhance the linearity of a CMOS PA, several linearization techniques have been proposed. The use of a variable capacitor at the common-gate (CG) FET and envelope-reshaped gate bias technique effectively improved the PA linearity [2, 3]. As explained in [4, 5], one of the major nonlinearities of a CMOS device comes from the gate-source capacitance (C_{gs}) of the common-source (CS) amplifier. This nonlinearity can be compensated using a PMOS device with opposite C_{gs} vs. V_{gs} behavior to NFET [4]. However, the use of a PMOS device at the gate of the main-stage causes capacitance overload. Since the overloaded capacitance makes the gate impedance very low, high-Q inter-stage matching cannot be avoided, which can impact the gain and efficiency as well as the bandwidth, as discussed in [4]. In multi-stage PA design, the nonlinearities from the preceding (driver) stage as well as the main-stage should also be compensated. In [4], the nonlinearity from the driver-stage was not compensated but avoided by supplying high quiescent current to the stage, which may result in efficiency degradation.

In this work, a highly linear and efficient watt-level CMOS PA is implemented using an integrated PMOS linearizer

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for low-band UMTS Tx applications. The problem described above is resolved by employing a PMOS linearizer with optimized AM-PM at the input of the driver-stage, thereby compensating the composite nonlinearity coming from the two amplifiers. In this paper, the detailed circuit design of the proposed linear PA is presented in Section II, followed by the fabrication and measurement results of the PA in Section III.

II. Circuit Design

Fig. 1 shows a schematic of the proposed linear CMOS PA. It is based on a two-stage single-ended stacked-FET amplifier design [1], and is targeted to obtain an output power (P_{out}) of more than a watt using V_{DD} = 4 V for handset applications. Thus, the optimum load impedance (R_{opt}) is designed to be 6 Ω, which is smaller than that described in [1], where V_{DD} = 6.5 V and R_{opt} = 11.5 Ω were used, because P_{out} can be approximated to be $P_{out} = V_{DD}^2 / R_{opt}$. Due to smaller R_{opt}, the FET size should be increased to drive more RF current and avoid high knee voltage of the CMOS device [6]. Thus, a quadruple stacked-FET with a gate width of 20 mm is adopted for main-stage (M_1 to M_4) to attain sufficient voltage and current swings with margin. Each transistor is realized with a 2.5-V standard I/O NFET. According to the stacked-FET PA theory, optimum load impedances should be given for the intermediate FETs (M_1 to M_3 in Fig. 1) as well as the top FET (M_4) for even distribution of RF voltage swing for each FET. Thus, five gate distribution capacitors in both stages (C_{D2}, C_{D3}, C_2, C_3, and C_4), which are the main design parameters for determining optimum loads of the intermediate FETs, are designed based on the analysis in [1]. Even though the gate capacitors are properly designed, however, the load impedances of the intermediate FETs have sub-optimal values due to the excessive parasitic capacitances of a FET with large gate width. To cancel out the parasitic capacitances, three external drain-source Miller capacitors (C_{M2}, C_{M3}, and C_{M4}) are used

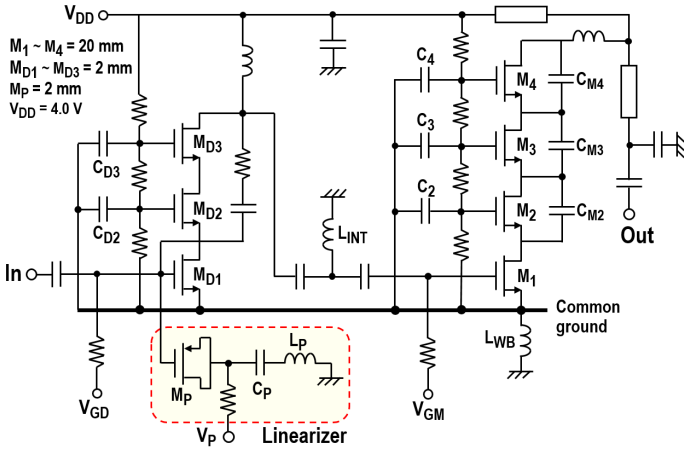


Fig. 1. Schematic of the proposed 2-stage linear CMOS stacked-FET power amplifier.

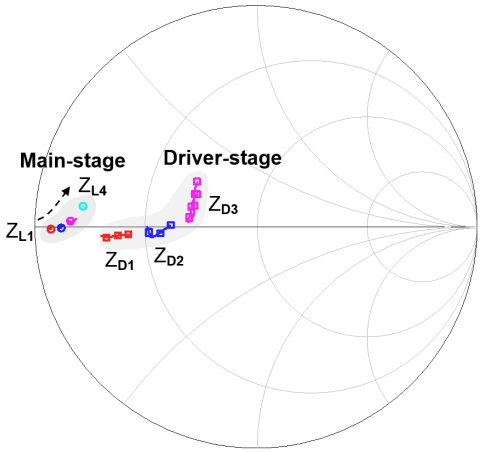


Fig. 2. Simulated load impedances of the main-stage and driver-stage FETs as a function of input power.

and the efficiency can thus be improved [7]. Fig. 2 shows the simulated load impedance of each FET of the driver-stage and main-stage.

As described in [4, 5], the nonlinear gate-source capacitance (C_{gs}) of CS amplifier can be compensated using a PMOS, because a PMOS exhibits the opposite C_{gs} vs. V_{gs} behavior to NMOS and thus the phase distortion is alleviated by flattening the capacitance slope [4]. To resolve the problems mentioned in Section I, a PMOS linearizer is adopted at the gate of the driver-stage CS transistor, as shown in Fig. 1. This linearizer is composed of a PMOS (M_P), a dc block capacitor (C_P), and an inductor (L_P). Contrary to the phase linearizer in [4], L_P is also used. The effective capacitance of the linearizer, C_{LIN}, can be obtained by calculating the reactance sum of M_P, C_P, and L_P as follows:

$$X_{LIN} = -\frac{1}{\omega}\left(\frac{1}{C_{MP}} + \frac{1}{C_P}\right) + \omega L_P \approx \frac{-1}{\omega C_{MP}} + \omega L_P \tag{1}$$

$$\frac{1}{C_{LIN}} = -\omega X_{LIN} \approx \frac{1}{C_{MP}} - \omega^2 L_P . \tag{2}$$

In this work, C_P is a DC blocker and is assumed to be far greater than C_{MP}. As one can see from Eq. (2), C_{LIN} is further increased as C_{MP} is increased by adding L_P, because C_{MP} and L_P connected in series tend to resonate out. Therefore, C_{LIN} can be reconfigured to have a steeper (optimized) capacitance variation slope as a function of input power to additionally optimize the AM-PM of the overall PA.

Fig. 3 shows the simulated capacitance at the gate of the driver-stage and resultant AM-PM of the composite PA. The composite input capacitance ($C_{gN} + C_{LIN}$) at the driver-stage is not flat but has a positive slope to compensate for the phase nonlinearity of the following (main-stage) amplifier as well. By adopting L_P, the capacitance variation slope can be reshaped to achieve optimal nonlinear C_{gs}

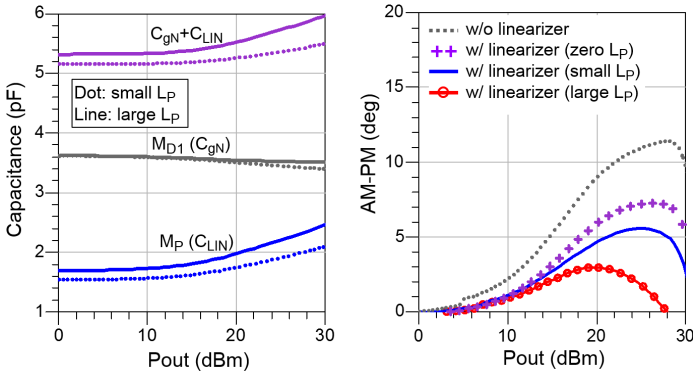


Fig. 3. Simulated results: (a) capacitance at the gate of the driver-stage as a function of output power, (b) AM-PM characteristics of the 2-stage stacked-FET power amplifier.

compensation without using a large PMOS device. As shown in Fig. 3(b), the use of small / large L_P (= 1.2 / 2.7 nH) lowers AM-PM distortion from 12° to 5.5° / 3.5°, respectively. Even if large L_P further lowers the phase distortion near mid output power (P_{out}) level, it causes early AM-PM compression at high P_{out}; thus, small L_P was used in this work. If L_P is not used, the amount of AM-PM correction is limited to 7.5°, which is insufficient to meet the stringent W-CDMA linearity spec.

In addition, investigating the phase deviation by each FET of both stages is worthwhile. Fig. 4 shows the simulated drain voltage phase deviation of each FET. Contrary to

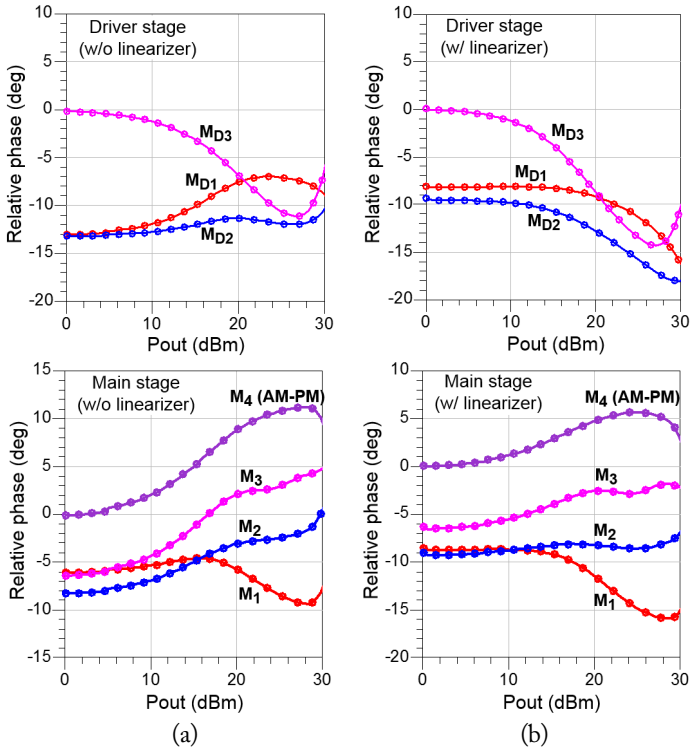


Fig. 4. Simulated drain voltage phase deviation of each FET: (a) Without linearizer and (b) with linearizer.

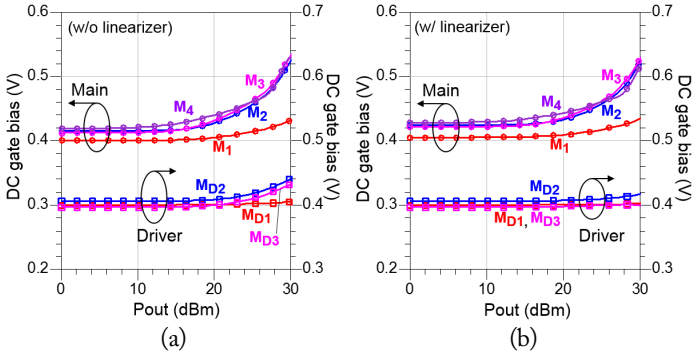


Fig. 5. Simulated DC gate-source bias of each FET: (a) without linearizer and (b) with linearizer.

the result without a linearizer, the phase of driver-stage using the linearizer becomes more pre-distorted, and then the signal is delivered to the main-stage. The phase deviation slope by the main-stage is the opposite direction to the input signal, and thus the resultant AM-PM is improved. Note that the stacked-FET structure is capable of self-phase compensation, because the CS amplifier and CG amplifier have the opposite phase characteristics [8]. Fig. 5 shows the simulated DC gate-source bias of each FET, where no significant difference is observed between the PAs with and without linearizers.

III. Fabrication and Measurement

The designed linear PA was fabricated using a 0.18-μm silicon-on-insulator (SOI) CMOS process with high-resistivity substrate (ρ = 1 kΩ · cm). All the MOSFETs have a gate-length of 0.32-μm and an oxide thickness of 52 nm, which is originally targeted for standard 2.5-V I/O operation. The PA is based on a two-stage amplifier design, and the gate-widths of a single FET for the driver-stage and main-stage were chosen to be 2 and 20 mm, respectively. The capacitances of five gate capacitors for CG-FETs, C_{D2}, C_{D3}, C_2, C_3, and C_4, are 6, 2, 32, 12, and 8 pF, respectively. Three Miller capacitors, C_{M2}, C_{M3}, and C_{M4}, have values of 3, 6, and 10 pF, respectively. The source degeneration effect of this PA was minimized by using multiple bond-wires. Also, a bond-wire is used for L_P (in Fig. 1) implementation and optimization. The fabricated SOI CMOS IC is shown in Fig. 6, and its die size and thickness are 1.6 mm × 0.6

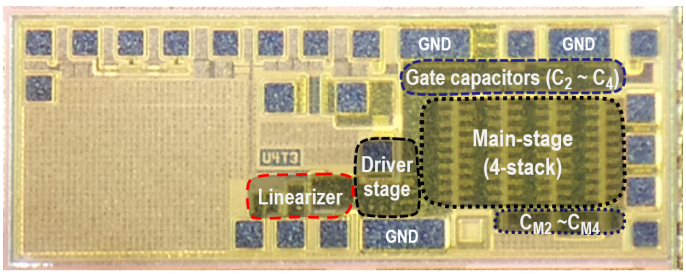


Fig. 6. Chip photograph (size = 1.6 mm × 0.6 mm).

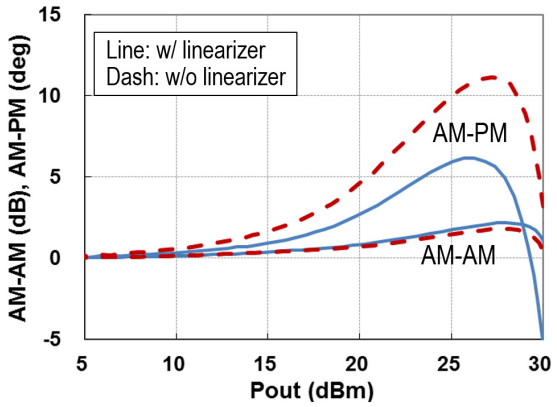


Fig. 7. Measured AM-AM and AM-PM characteristics of the power amplifier using continuous wave signal.

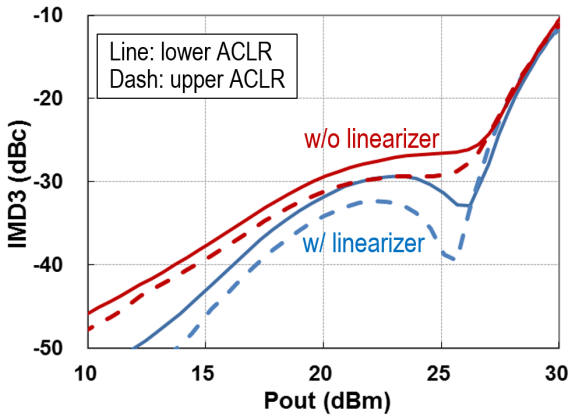
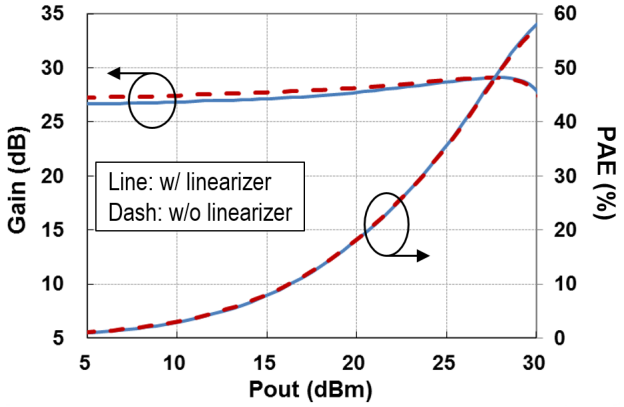


Fig. 8. Measured third-order intermodulation distortion (IMD3) (tone spacing = 4 MHz). ACLR = adjacent channel leakage ratio.

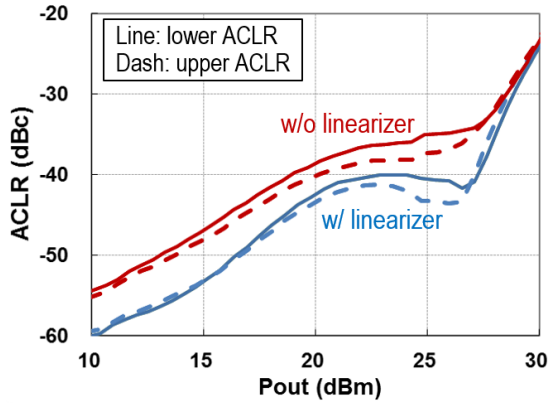
mm and 150 μm, respectively. It was mounted on a 400-μm-thick FR4 substrate ($\varepsilon_r = 4.6$, $\tan\delta = 0.025$), where an off-chip LC network was used for output matching.

The implemented PA module was tested under the 3GPP uplink W-CDMA signal (Rel'99) at 836.5 MHz and a supply voltage of 4 V. The idle current is 75 mA. Prior to the W-CDMA test, the nonlinear characteristics of the PA were measured using single-tone (continuous wave [CW]) and two-tone signals. Fig. 7 shows the measured AM-AM and AM-PM characteristics using a CW signal. The AM-PM deviation of the linearized PA was reduced from 11.5° to 6°, which is close to the simulation result. Fig. 8 shows the two-tone third-order inter modulation distortion (IMD-3). By employing the linearizer, the linear output power meeting IMD3 = −30 dBc is extended.

The measurement results of power gain, power-added efficiency (PAE), and adjacent channel leakage ratio (ACLR) using W-CDMA signal are plotted in Fig. 9. The PA showed a power gain of higher than 27 dB and ACLR better than −40 dBc up to the output power of 27.1 dBm. Output powers / PAEs meeting ACLRs of −40 dBc and −36 dBc were 27.1 dBm / 45.6% and 27.7 dBm / 48.3%, respectively. Compared to the reference PA without a linearizer, which showed ACLR of −36 dBc and PAE of 38.5% at P_{out} = 25.7 dBm, output power and PAE were improved by 2 dB and 9.8%, respectively. The linearization effect of the PA under the W-CDMA condition was validated by measuring the dynamic AM-AM and AM-PM. Fig. 10 shows the dynamic characteristics of the PA at P_{out} = 27 dBm. Compared to the reference PA, the proposed PA showed improved flatness in terms of gain and phase.



(a)



(b)

Fig. 9. Measured W-CDMA results: (a) Gain and power-added efficiency (PAE) and (b) adjacent channel leakage ratio (ACLR).

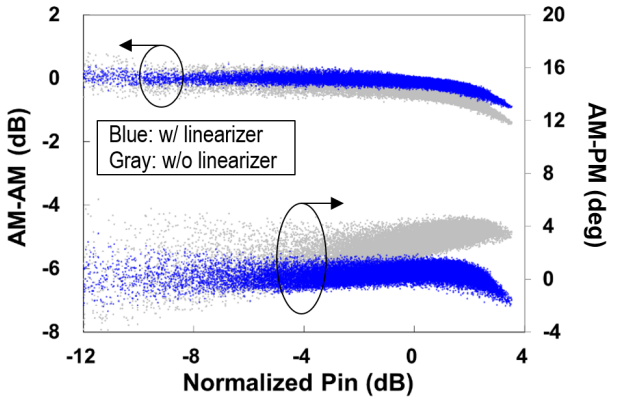


Fig. 10. Measured dynamic AM-AM and AM-PM characteristics at P_{out} = 27 dBm using W-CDMA signal.

Table 1. Performance comparison of recently reported W-CDMA CMOS power amplifiers

Ref.	Technology	P_{out} (dBm)	PAE (%)	ACLR (dBc)	V_{DD} (V)	Freq. (GHz)
[1] [a]	SOI CMOS 0.13 μm	29.4 28.5	41.4 38.7	−33 −38	6.5	1.9
[2] [a]	SOI CMOS 0.18 μm	27.6 27.1	49.5 47.5	−33 −36	4.0	0.837
[3] [b]	CMOS 0.18 μm	26.8	43.3	−37	3.5	1.85
[4] [a]	CMOS 0.5 μm	24	29	−35	3.3	1.75
[9] [a]	GaAs HBT	28	44.5	−38	3.4	1.95
This work [a]	SOI CMOS 0.18 μm	28.2 27.7 27.1	50.6 48.3 45.6	−33 −36 −40	4.0	0.837

PAE = power-added efficiency, ACLR = adjacent channel leakage ratio, SOI = silicon-on-insulator.
[a]Off-chip output matching.
[b]On-chip IPD TLT for output matching.

The performance of the recently reported W-CDMA PAs is summarized in Table 1 for comparison. The linearity and efficiency of the proposed PA is favorable among the reported PAs. Its performance is also comparable to the GaAs-based PA [9].

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IV. Conclusion

A linear stacked-FET PA module has been implemented using SOI CMOS technology for W-CDMA handset applications. The gate-source capacitance nonlinearity of a common-source amplifier is compensated by employing a PMOS linearizer with optimized phase (capacitance) slope at the gate of the driver-stage transistor. Thus, the AM-PM is improved while avoiding capacitance overloading effect at the main-stage. The fabricated PA showed PAE of 45.6% and meets the UMTS linearity requirement with margin (<−40 dBc versus system spec of −33 dBc) at P_{out} = 27.1 dBm. The performance of the PA is favorably comparable to that of GaAs-based PAs.

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