JOURNAL OF ELECTROMAGNETIC ENGINEERING AND SCIENCE, VOL. 14, NO. 2, 61~67, JUN. 2014

http://dx.doi.org/10.5515/JKIEES.2014.14.2.61
ISSN 2234-8395 (Online) · ISSN 2234-8409 (Print)

A 0.13-μm Zero-IF CMOS RF Receiver for LTE-Advanced Systems

Youngho Seo · Thanhson Lai · Changwan Kim*

Abstract

This paper presents a zero-IF CMOS RF receiver, which supports three channel bandwidths of 5/10/40 MHz for LTE-Advanced systems. The receiver operates at IMT-band of 2,500 to 2,690 MHz. The simulated noise figure of the overall receiver is 1.6 dB at 7 MHz (7.5 dB at 7.5 kHz). The receiver is composed of two parts: an RF front-end and a baseband circuit. In the RF front-end, a RF input signal is amplified by a low noise amplifier and G_m with configurable gain steps (41/35/29/23 dB) with optimized noise and linearity performances for a wide dynamic range. The proposed baseband circuit provides a −1 dB cutoff frequency of up to 40 MHz using a proposed wideband OP-amp, which has a phase margin of 77° and an unit-gain bandwidth of 2.04 GHz. The proposed zero-IF CMOS RF receiver has been implemented in 0.13-μm CMOS technology and consumes 116 (for high gain mode)/106 (for low gain mode) mA from a 1.2 V supply voltage. The measurement of a fabricated chip for a 10-MHz 3G LTE input signal with 16-QAM shows more than 8.3 dB of minimum signal-to-noise ratio, while receiving the input channel power from −88 to −12 dBm.

Key Words: CMOS, LTE, LTE Advanced, RF Receiver, Passive Mixer, Wideband OP-Amp.

I. Introduction

Currently, smartphone use continues to increase and is now an essential part of people's daily lives. Mobile applications that utilize long-term evolution (LTE) of 3rd generation partnership project (3GPP) are now popular because of highly responsive mobile voice and data services. However, the development of new mobile communication systems such as LTE-Advanced is required to satisfy demands for high-speed multimedia data communications such as real-time video streaming. The LTE-Advanced system offers a peak data-rate of 1 Gbps downlink, which is 10 times higher than 100 Mbps of the 3G LTE systems [1]. Accordingly, many RF receivers for LTE-Advanced systems have been reported in [2−4]. A high data-rate can be achieved by increasing the modulation level and expanding the signal bandwidth as effective techniques [4].

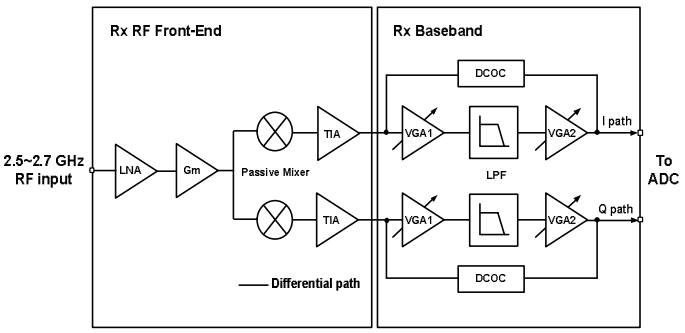


Fig. 1. Simplified block diagram of the proposed RF receiver.

Manuscript received March 11, 2014 ; Revised April 14, 2014 ; Accepted May 16, 2014. (ID No. 20140311-014J)
Department of Electronics Engineering, Dong-A University, Busan, Korea.
*Corresponding Author: Changwan Kim (e-mail: cwkim@dau.ac.kr)

This paper presents a zero-IF CMOS RF receiver for LTE-Advanced system, which can support up to a 40 MHz channel bandwidth for high data-rate applications. The proposed RF receiver operates at an IMT-band of 2,500 to 2,690 MHz and provides a gain from 25 dB (low gain mode) to 99 dB (high gain mode). The simulated noise figure of the receiver is 1.6 dB in channel bandwidth from 5 to 40 MHz and 7.5 dB at 7.5 MHz. Since the sub-carrier channel bandwidth is 15 kHz and a null-tone has been allocated in the LTE-Advanced system, the baseband signal power is located from 7.5 kHz to 10/20/40 MHz.

Fig. 1 shows a block diagram of the proposed zero-IF RF receiver, which consists of two parts: the RF front-end and the baseband circuit. The RF front-end is composed of a narrow-band low noise amplifier (LNA), a G_m (transconductor), a current-driven passive mixer, and transimpedance amplifiers (TIAs). The baseband circuit is composed of several variable gain amplifiers (VGAs), low-pass filters (LPFs), and DC-offset cancellation (DCOC) circuits. Here, a local oscillator (LO) signal for the passive mixer is externally provided from a signal generator.

Ⅱ. RF Front-End Design

As shown in Fig. 2, the proposed LNA is a differential common-source amplifier with an inductive source degeneration to achieve a low noise characteristic and a high voltage gain versus power consumption. The LNA has an *RLC* resonant load centered at 2.6 GHz and provides a voltage gain of 29/35/41 dB by controlling the load resistors R_1 and R_2.

In Fig. 2, the current-driven passive mixer architecture [5], which is composed of the G_m, the quadrature passive mixer core, and the quadrature TIAs, is adopted to overcome a trade-off between signal-to-noise ratio (SNR) and linearity. The G_m has adopted a differential common-source topology and uses inductive loads (L_3 and L_4) to eliminate input parasitic capacitance of the passive mixer [5]. This inductive load provides high impedance to the following TIA through the passive mixer's on-resistor R_{on} so that 1/f noise from the TIAs can be mitigated.

In the passive mixer, a trade-off between linearity and noise figure occurs directly, depending on the LO bias levels. In this work, the on-overlap LO biasing level has been chosen for the proposed passive mixer considering noise figure, conversion gain, and linearity.

The proposed TIA is a common-gate amplifier with low input impedance for the current-to-voltage conversion. It has the 1st-order *RC* load for filtering unwanted spurious noise from the mixing operation and LO leakage. In the TIA, long-channel NMOS devices ($L = 5$ μm) for $M_{11}-M_{18}$ have been used to suppress 1/f noise.

In order to ensure a wide dynamic range of the overall RF receiver, the gain of the RF front-end should be in the range of 41 to 23 dB with a step of 6 dB for the incoming input signal. The gain control from 41 to 29 dB has been achieved in the LNA load by adjusting the value of the resistors (R_1 and R_2). However, even though the LNA has a gain of 23 dB, the following G_m is saturated by the LNA output voltage swing. Thus, a minimum gain mode switch (M_5 and M_6) is added between the LNA and the G_m [6]. As shown in Fig. 2, in order to achieve minimum voltage gain of 23 dB, the cascode transistors (M_3 and M_4) in the LNA and input transistors (M_7 and M_8) in the G_m turn off and the switches (M_5 and M_6) simultaneously turn on. Thus, the LNA's input stage (M_1 and M_2) and the G_m's cascode stage (M_9 and M_{10}) are operated as another new cascode amplifier. Using this method, the RF front-end can achieve the minimum gain of 23 dB without severe distortion for the high input signal of −18 dBm.

Ⅲ. Base-Band Circuit Design

Fig. 3 shows the proposed analog baseband circuit (only I-path), comprising a VGA1, a channel-selection LPF, a VGA chain (VGA2), and a DCOC circuit. A lower noise figure of the receiver is achieved by locating the LPF between VGA1 and VGA2. The gain of the VGA1 suppresses noise from the LPF. The proposed analog baseband circuit provides a voltage gain from −23 to 79 dB in a 0.25 dB gain step.

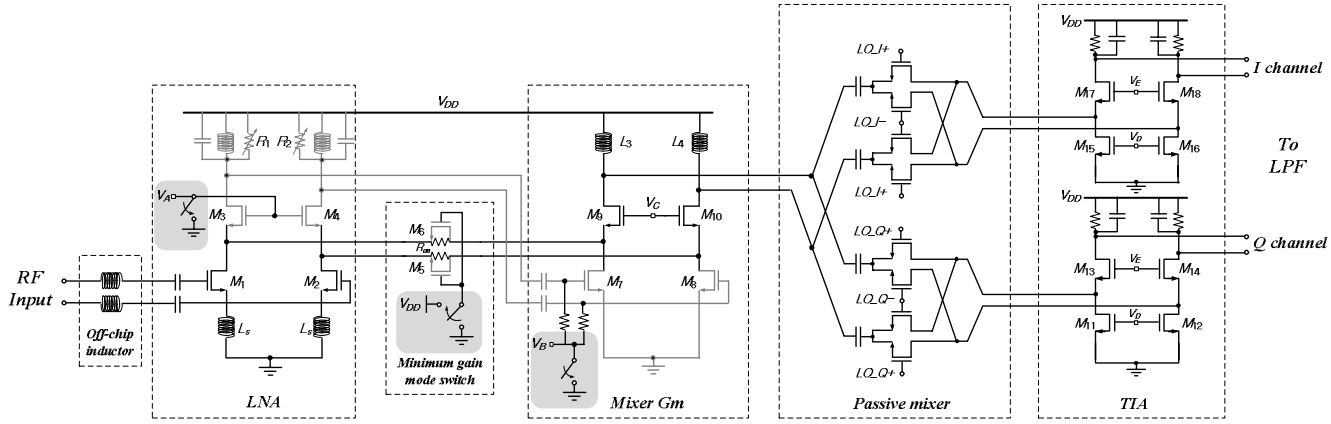


Fig. 2. Schematic of the proposed RF front-end receiver. LNA=low noise amplifier, G_m=transconductor, TIA=transimpedance amplifier.

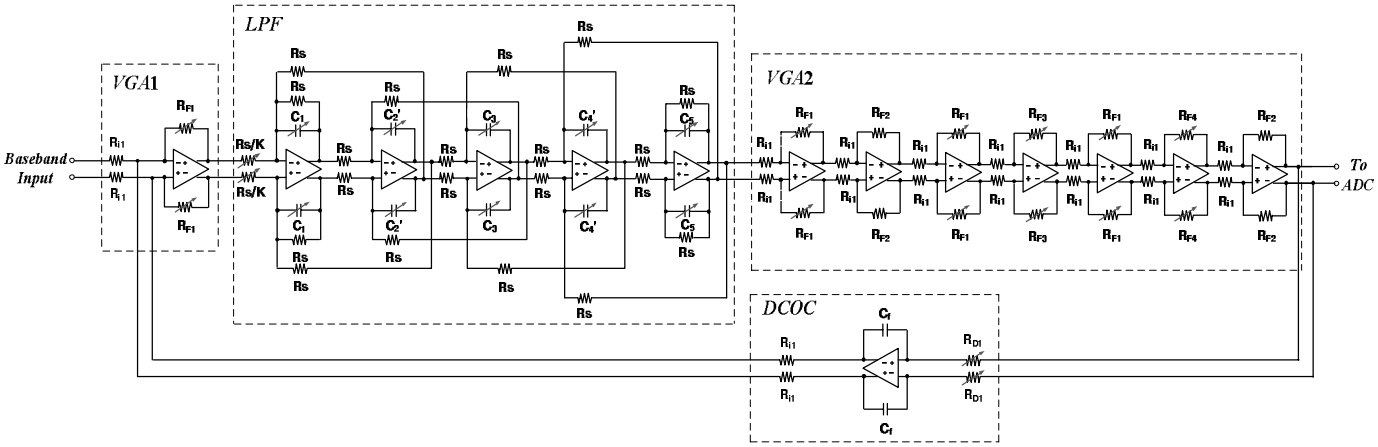


Fig. 3. Block diagram of the proposed base-band circuit (I-path). VGA = variable gain amplifier, LPF = low-pass filter, DCOC = DC-offset cancellation circuit.

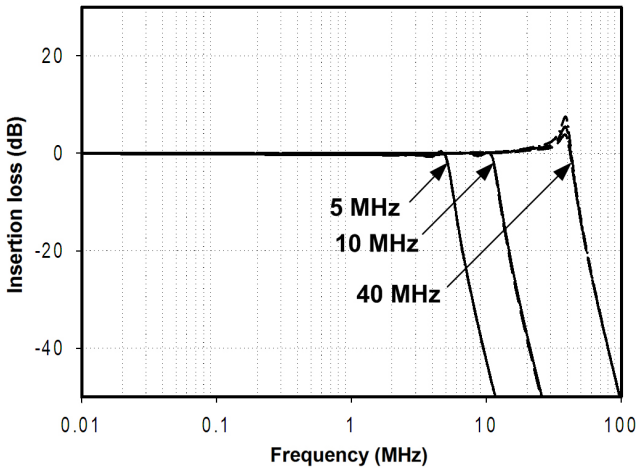


Fig. 4. Frequency response of the proposed low-pass filter.

In general, since active *RC* LPF shows higher linearity than G_m-C LPF, a 5th-order active *RC* Chebyshev LPF is adopted in this work [9−11]. The LPF provides a −1 dB cutoff frequency of 5 MHz, 10 MHz, and 40 MHz with a frequency compensation circuit. The −1 dB cutoff bandwidth of the channel-selection LPF is given by $1/(R_S \cdot C_{1-5})$ and can be changed by varying the capacitance of C_{1-5}. An insertion loss of the LPF is given by $K/2$ where K is a proportionality constant, which is implemented in input resistance of the LPF. In this work, the K of 2 was chosen to make an insertion loss of 0 dB.

Fig. 4 shows the simulated frequency response of the proposed channel-selection LPF, where the cutoff frequencies of 5, 10, and 40 MHz are not much changed for corner states of SS (−80℃), TT (27℃), and FF (40℃) mode. In Fig. 4, the peaking at 40 MHz channel bandwidth comes from the deficient unit-gain bandwidth (UGBW) of 2.04 GHz in the proposed OP-amp. However, from the overall receiver measurements, the receiver does not show any oscillation problem or performances degradation.

The proposed VGAs (VGA1 and VGA2), which are composed of a fully differential OP-amp with a negative feedback resistor for high linearity, are designed to achieve −1 dB cutoff frequency of 50 MHz for the maximum channel bandwidth of 40 MHz [7].

In Fig. 3, the VGA1 provides a voltage gain from −12 to 12 dB with a 6 dB step. The VGA2 provides voltage gain from −11 to 67 dB with a 0.25 dB fine gain step to compensate I-Q gain mismatch. To provide the total gain of 67 dB, the VGA2 consists of 7 stages; the 1st, 3rd, and 5th amplifiers have a voltage gain from −12 to 12 dB with a 6 dB step respectively, the 2nd and 7th amplifiers provide a fixed voltage gain of 12 dB, the 4th amplifier provides a voltage gain from 1 to 6 dB with a 1 dB step, and the 6th amplifier provides a voltage gain from 0 to 1 dB with a 0.25 dB step.

A DCOC in a zero-IF receiver is inevitable, since an unexpected DC-offset may saturate the baseband output. The DC-offset problem is solved by building a DCOC loop based on voltage-current negative-feedback, as shown in Fig. 3. The high-pass cutoff frequency of the DCOC circuits is set to less than 1 kHz to ensure active sub-carriers around DC. However, due to this cutoff frequency of 1 kHz, the required capacitances C_f are 2 μF, which cannot be integrated on a chip. Thus, they are externally implemented at the cost of extra pads. The constant cutoff frequency in the DCOC circuit has been achieved by digital control of the value of input resistor R_{D1} in the DCOC circuit as the variation of voltage gain in the feed-forward path. The post-layout simulation shows that the analog baseband output can be tolerated for up to 700 mV input DC-offset.

Fig. 5 shows the frequency response of the baseband circuit with a cutoff frequency of 10 MHz. The baseband circuit provides a voltage gain from −23 to 79 dB, and the high pass cutoff frequency of less than 1 kHz. The simulated results of the proposed baseband circuit are summarized in Table 1.

To achieve the channel bandwidth of up to 40 MHz, the LPF and VGAs need a wideband OP-amp. Fig. 6 shows the

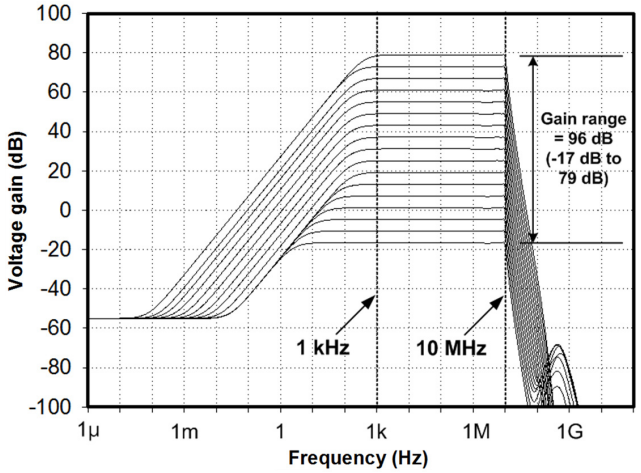


Fig. 5. Frequency response of the proposed baseband circuits.

Table 1. Performance summary of the baseband circuit

Channel BW (MHz)	5, 10, 40
Gain range (dB)	−23 to 79
Gain step (dB)	0.25
Stop-band attenuation @ 2 · fc (dB)	> 40
Group delay (ns)	27 to 226
DC current for I-Q path (mA)	90
Supply (V)	1.2
Technology	0.13-μm CMOS

f_C = −1 dB cutoff frequency.

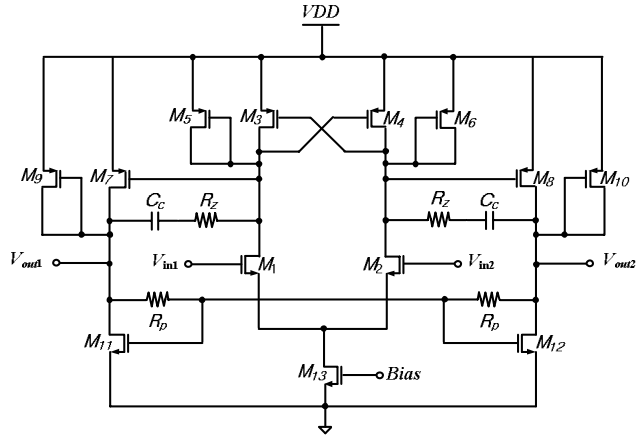


Fig. 6. Schematic of the proposed operational amplifier.

proposed wideband two-stage OP-amp, which uses a cross-connected PMOS load (M_3 to M_6) at the first stage [8]. The cross-connected PMOS load provides a very wideband characteristic of the OP-amp by putting the second pole far away from the dominant pole. However, the cross-connected PMOS load generates nonlinear components such as even-order harmonics. To eliminate this problematic effect, a diode-connected PMOS load (M_9 and M_{10}) is added at the second stage. The even-order harmonics from the first stage

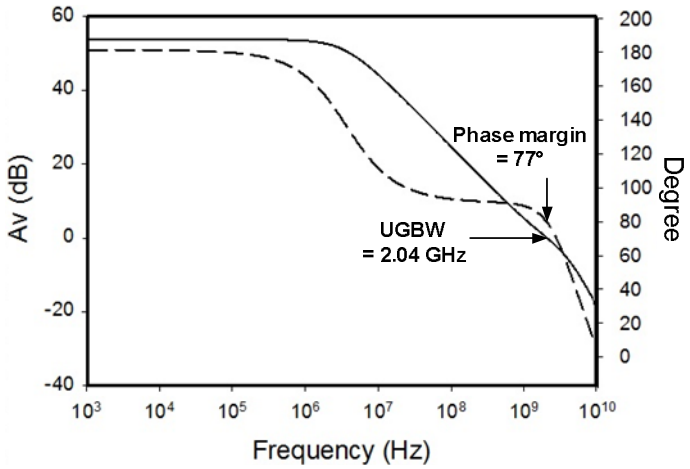


Fig. 7. Phase and gain curve of the operational amplifier. UGBW = unit-gain bandwidth.

can be eliminated after combining with another even-order harmonic from the diode-connected PMOS load (M_9 and M_{10}) of the second stage. Additionally, for immunity of common-mode signals, a diode-connected NMOS load (M_{11} and M_{12}) with a high value of the resistor, which has high common-mode rejection ratio, is used at the second stage. To secure an enough phase-margin of the OP-amp, an *RC* compensation circuit (R_Z, C_C) is adopted between the first and the second stage [10].

Fig. 7 shows simulated results of the proposed wideband OP-amp. The proposed OP-amp provides a phase margin 77° and a UGBW of 2.04 GHz, which is about 50 times the maximum channel bandwidth (40 MHz). An OP-amp consumes 3.47 mA from a 1.2 V supply.

IV. Measurement Results

The proposed zero-IF CMOS RF receiver for LTE-Advanced systems has been implemented in 0.13-μm CMOS technology, as shown in Fig. 8. The receiver consumes 116 (high gain mode)/106 (low gain mode) mA from a 1.2 V supply.

Figs. 9−11 show the measured results of the fabricated chip. A 10-MHz 3G LTE signal only is applied to the input of the chip for measurements, even though the receiver supports multi-channels of 5, 10, and 40 MHz.

Figs. 9 and 10 show the measured an input 1-dB gain compression point ($P_{1\,dB}$) of the proposed RF receiver with the high and low gain modes, respectively. Due to the sufficient linearity for all the signal paths, the proposed RF receiver achieves $P_{1\,dB}$ of −92 dBm (high gain mode) and −18 dBm (low gain mode) for a fixed output power of 6 dBm for 50 Ω loading. At the high and the low gain mode, a simulated overall gain of the RF receiver is 103/29 dB but the measurements show the 99/25 dB because of unexpected parasitic capacitances in the RF paths.

Fig. 11 shows the measured SNR for the 10-MHz 3G

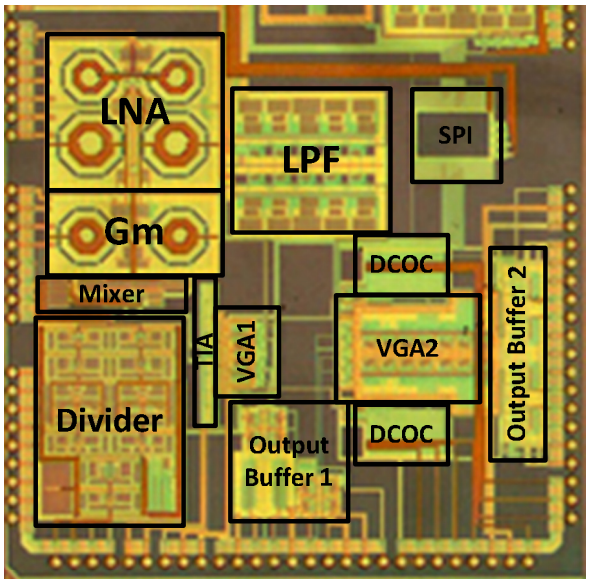


Fig. 8. Chip micrograph. LNA = low noise amplifier, G_m = transconductor, TIA = transimpedance amplifier, LPF = low-pass filter, DCOC = DC-offset cancellation circuit, VGA = variable gain amplifier.

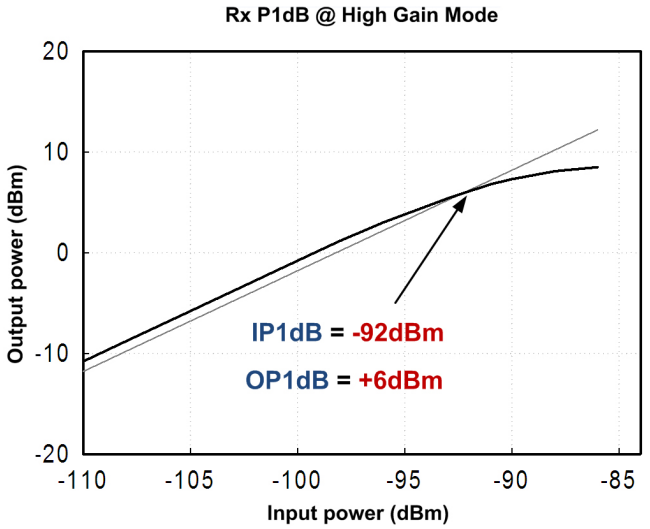


Fig. 9. Measured $P_{1\,dB}$ at the high gain mode.

LTE input signal with 16-QAM. The proposed RF receiver provides more than 8.3 dB of minimum SNR [14], while receiving the input channel power from −88 to −12 dBm.

Table 2 summarizes the measured results and compares them with the state-of-the-art measurements [12, 13]. The proposed RF receiver achieves the widest channel bandwidth, the highest gain, and the lowest noise figure.

V. Conclusion

This paper has presented a zero-IF CMOS RF receiver for LTE-Advanced systems, which is implemented in 0.13-μm CMOS technology. The simulated and the measure-

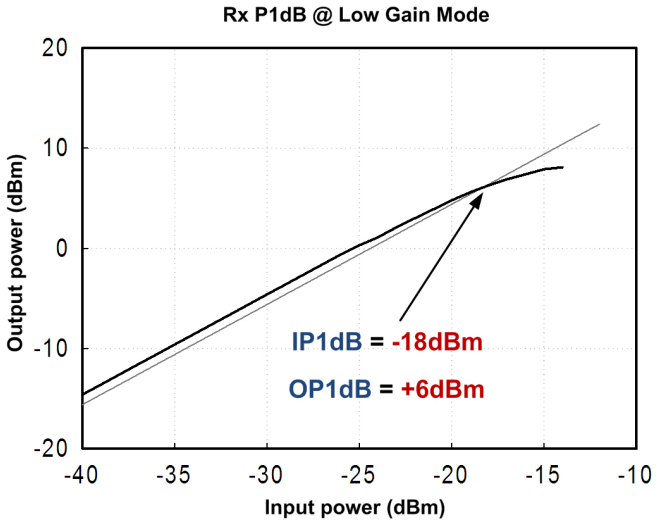


Fig. 10. Measured $P_{1\,dB}$ at the low gain mode.

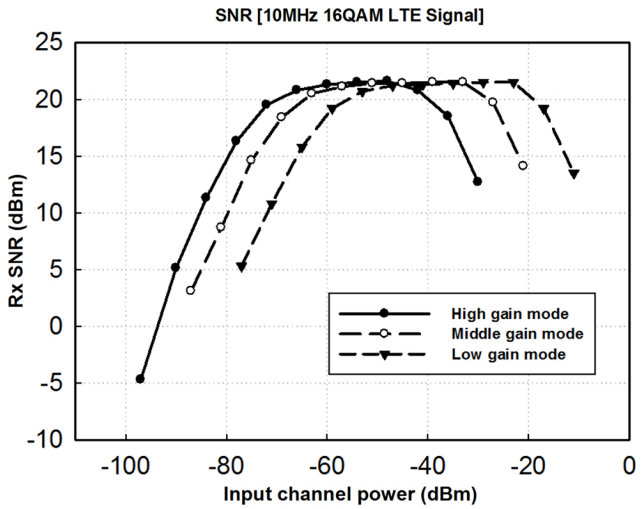


Fig. 11. Measured SNR of the proposed RF receiver using a 10-MHz LTE signal. SNR = signal-to-noise ratio, LTE = long-term evolution.

Table 2. Performance comparison

Parameter	Present study	[12]	[13]
Frequency (GHz)	2.5 – 2.7	0.1 – 6	0.1 – 2.4
Signal BW (MHz)	5/10/40	1 – 40	0.2 – 30
Maximum gain (dB)	94 [a]	68 – 77	67
IIP3 (dBm)	−8	−7.5 – 9	−9 – 7
IP1 dB (dBm)	−18	NA	NA
Noise figure (dB)	1.6 [b]	2.3 – 7	5 – 8
Chip area (mm^2)	2.2 × 2.2	2.5 × 2	2.3
Power (mW)	127/139	54/135	44
Supply (V)	1.2	1.1/2.5	1.2
CMOS technology	0.13 μm	40 nm	90 nm

[a] Measured result with the 10 MHz-16QAM LTE signal.
[b] Simulated result (7.5 dB @ 7.5 kHz).

ment results demonstrate that the proposed RF receiver can favorably support the LTE-Advance systems.

This paper was supported by Dong-A University Research Fund in 2014.

REFERENCES

[1] K. Safjan, V. D'Amico, D. Bultmann, D. Martin-Sacristan, A. Saadani, and H. Schoneich, "Assessing 3GPP LTE-advanced as IMT-advanced technology: the WINNER+ evaluation group approach," *IEEE Communications Magazine*, vol. 49, no. 2, pp. 92−100, Feb. 2011.

[2] S. Rodriguez, A. Rusu, and M. Ismail, "4G CMOS nanometer receivers for mobile systems: challenges and solutions," in *Proceedings of* the *International Symposium on Signal, Circuits and Systems*, Iasi, Romania, 2009, pp. 1−4.

[3] A. Parssinen, "Multimode-multiband transceivers for next generation of wireless communications CMOS," in *Proceedings of the 37th European Solid-State Circuits Conference*, Helsinki, Finland, 2011, pp. 25−36.

[4] Z. Xu, J. Zhou, Z. Yu, W. Huang, Y. Ni, F. Huang, and Y. Chu, "Design of high performance RF transceiver for next generation wireless communications," in *Proceedings of* the *International Conference on Microwave and Millimeter Wave Technology*, Shenzhen, China, 2012, pp. 1−4.

[5] A. Mirzaei, H. Darabi, J. C. Leete, X. Chen, K. Juan, and A. Yazdi, "Analysis and optimization of current-driven passive mixers in narrowband direct-conversion receiver," *IEEE Journal of Solid-State Circuit*, vol. 44, no. 10, pp. 2678−2688, Oct. 2009.

[6] M. C. Kuo, S. W. Kao, C. H. Chen, T. S. Hung, Y. S. Shih, T. Y. Yang, and C. N. Kuo, "A 1.2 V 114 mW dual-band direct-conversion DVB-H tuner in 0.13 μm CMOS," *IEEE Journal of Solid-State Circuit*, vol. 44, no. 3, pp. 740−750, Mar. 2009.

[7] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York, NY: John Willey & Sons Inc., 2001.

[8] A. T. Phan, R. Farrell, J. Lee, and S. G. Lee, "380 MHz low-power sharp-rejection active-RC LPF for IEEE 802.15.4a UWB WPAN," in *Proceedings of International Symposium on Circuits and Systems*, Taipei, Taiwan, 2009, pp. 1369−1372.

[9] L. Thomas, "The Biquad: Part I. Some practical design considerations," *IEEE Transactions on Circuit Theory*, vol. 18, no. 3, pp. 350−357, May 1971.

[10] L. Thomas, "The Biquad: Part II. A multipurpose active filtering systems," *IEEE Transactions on Circuit Theory*, vol. 18, no. 3, pp. 358−361, May 1971.

[11] C. W. Kim, "A MB-OFDM UWB 0.18-μm CMOS RF front-end receiver," *Journal of the Korean Institute of Electromagnetic Engineering and Science*, vol. 8, no. 1, pp. 34−39, Mar. 2008.

[12] M. Ingels, V. Giannini, J. Borremans, G. Mandal, B. Debaillie, P. Van Wesemael, ⋯ J. Craninckx, "A 5 mm^2 40nm LP CMOS 0.1-to-3 GHz multistandard transceiver," in *Proceedings of the IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2010, pp. 458−459.

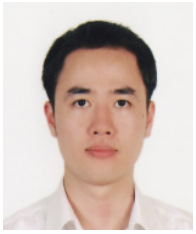
[13] M. Kitsunezuka, H. Kodama, N. Oshima, K. Kunihiro, T. Maeda, and M. Fukaishi, "A 30 MHz−2.4 GHz CMOS receiver with integrated RF filter and dynamic-range-scalable energy detector for cognitive radio," in *Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium*, Baltimore, MD, 2011, pp. 1−4.

[14] O. Werther, "LTE: from RF PHY specifications to RF circuits," Apr. 2012; http://rslteforum.com/LTE_RF-PHY_specs.php

Youngho Seo

received the B.S. and M.S. degree in electronics engineering from Dong-A University, Busan, Korea, in 2009 and 2011, respectively. He is currently working toward the Ph.D. degree at Radio Frequency Integrated Circuit (RFIC) laboratory, Dong-A University. His main research interests are CMOS analog and RF IC design for wireless local area network and cellular applications.

Thanhson Lai



was born in Hanoi, Vietnam, in 1986. He received the B.S. degree in electronics and telecommunications from Hanoi University of Science and Technology, Hanoi, Vietnam, in 2009 and the M.S. degree from Dong-A University, Busan, Korea, in 2014. He is currently working toward the Ph.D. degree at RFIC Laboratory, Dong-A University. His research interests are CMOS RF circuit and transceiver design.

Changwan Kim

received the B.S. degree from the School of Electrical Engineering and Computer Science, Kyungpook National University, Korea, in 1997, and the M.S. and Ph.D. degrees in engineering from the Information and Communications University (ICU), Daejeon, Korea, in 2003 and 2006, respectively. From 2006 to 2007, he worked for Electronics and Telecommunications Research Institute (ETRI), Daejeon, Korea. Since 2007, he has been with the Department of Electronic Engineering, Dong-A University, Busan, Korea, where he is now an associate professor. His main research interests are wideband/multiband CMOS RF transceiver design and system-level integration of transceivers.