

# A High Gain and High Harmonic Rejection LNA Using High Q Series Resonance Technique for SDR Receiver

Byungjoon Kim · Duksoo Kim · Sangwook Nam\*

## Abstract

This paper presents a high gain and high harmonic rejection low-noise amplifier (LNA) for software-defined radio receiver. This LNA exploits the high quality factor (Q) series resonance technique. High Q series resonance can amplify the in-band signal voltage and attenuate the out-band signals. This is achieved by a source impedance transformation. This technique does not consume power and can easily support multiband operation. The chip is fabricated in a 0.13- $\mu\text{m}$  CMOS. It supports four bands (640, 710, 830, and 1,070 MHz). The measured forward gain ( $S_{21}$ ) is between 12.1 and 17.4 dB and the noise figure is between 2.7 and 3.3 dB. The IIP3 measures between  $-5.7$  and  $-10.8$  dBm, and the third harmonic rejection ratios are more than 30 dB. The LNA consumes 9.6 mW from a 1.2-V supply.

**Key Words:** High Gain, High Harmonic Rejection, High Quality Factor Series Resonance, Impedance Transformation, SDR.

## I. INTRODUCTION

Recently, the number of wireless communication services has been increasing steadily. With an ever-increasing number of frequency bands and diverse wireless communication standards, front-end complexity and costs have risen. Therefore, the conventional receiver architecture requires more chips. Consequently, a software-defined radio (SDR) receiver is needed to reduce complexity and costs [1]. An SDR receiver can accomplish this, but it can also suffer from out-of-band interferences because it deals with wideband signals at the RF front-end [2].

Among various mixer architectures in SDR receivers, a hard-switching mixer is preferred, due to its superior gain and low noise characteristic [3, 4].

However, the desired signal is aliased with the interferences which are located around local oscillator (LO) odd order harmonic frequencies when down-converted to the baseband at the hard-switching mixer stage. Multi-phase mixers have been suggested to suppress RF signals around LO harmonics

[3, 5, 6]; however, they have the following drawbacks: 1) the seventh harmonic is not rejected and causes aliasing; 2) the third and fifth harmonic rejection (HR) performance is restricted by amplitude and phase mismatches; and 3) the complexity and size increase. The third HR ratio at the mixer stage is practically constrained to 30 to 40 dB, but much more rejection is needed to attenuate harmonic interferences with  $-40$  to  $0$  dBm power down to the noise floor [7]. Therefore, a high HR ratio is required before the mixer stage.

In [8], a design technique is provided for high HR; however, this does not address the resistance of the inductor or the induced gate noise. In [9], the research also neglects these noise sources and the fabricated and measured results are not described. The present paper analyzes a high Q resonance technique with these noise sources and provides a design guideline.

In this paper, Section II discusses the high Q series resonance technique, while Section III describes the circuit implementation in detail. Section IV shows the experimental

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School of Electrical Engineering and Computer Science, Institute of New Media and Communications, Seoul National University, Seoul, Korea.

\*Corresponding Author: Sangwook Nam (e-mail: [snam@snu.ac.kr](mailto:snam@snu.ac.kr))

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results of the demonstrated low-noise amplifier (LNA) circuit. Finally, a conclusion is given in Section V.

## II. THE HIGH Q SERIES RESONANCE TECHNIQUE

A MOSFET senses a voltage at the gate-source capacitor. Series resonance amplifies the in-band signal voltage and attenuates the out-band signal voltage at capacitor. Among the LNA architectures that use series resonance, the inductively degenerated LNA (L-CS LNA) [10] is popular and widely used. However, the voltage gain and HR are limited because the  $Q$  is constrained. A source degeneration technique simply provides input matching, although it decreases the  $Q$ .

Techniques for improving the  $Q$  of the LNA input passive network have previously been presented [8]. In [8], theoretically, a value of  $Q$  that can be obtained approximately two times larger than the L-CS LNA can be obtained when all parameters and conditions are same except input network. This is achieved by abandoning the degeneration inductor. However, an even higher  $Q$  is still needed to attain sufficiently high gain and a high HR ratio with low power operation. Moreover, this study did not consider the resistance of the inductor or the induced gate noise.

A high  $Q$  series resonance LNA (HQ-LNA) can overcome these problems, as shown in Fig. 1. A source impedance transformation provides higher  $Q$  resonance, as well as high gain and high HR. A source impedance transformation can be attained by a variety of methods, and a transmission line is a good approach. A multiband operation is also easily achieved by adjusting the resonance frequency, and this can be accomplished by changing the gate-source capacitor  $C_{tot}$ . The smallest  $C_{tot}$  equals  $C_{gs}$  ( $S_1$  and  $S_2$  are off), while largest  $C_{tot}$  equals  $C_{gs} + C_1 + C_2$  ( $S_1$  and  $S_2$  are on).

Fig. 2 shows the equivalent circuit of the proposed technique. The source voltage  $v_s$  and the source impedance  $R_s$  are transformed to  $v_{st}$  and  $Z_{st}$ , respectively. These values are determined by the transmission line parameters, which are the characteristic impedance  $Z_0$  and length of the line  $l_{TL}$ .

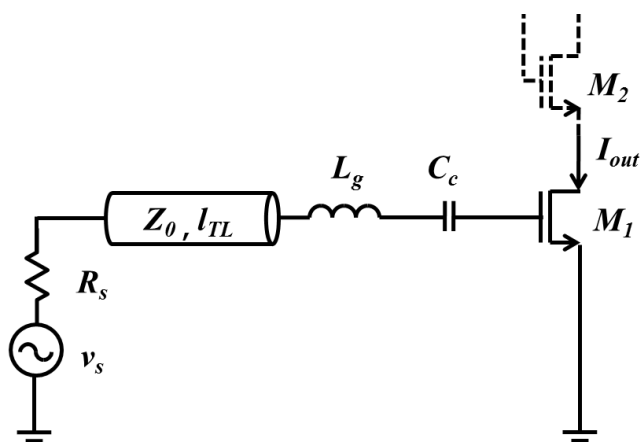


Fig. 1. Simplified schematic of the high  $Q$  series resonance low-noise amplifier input network.

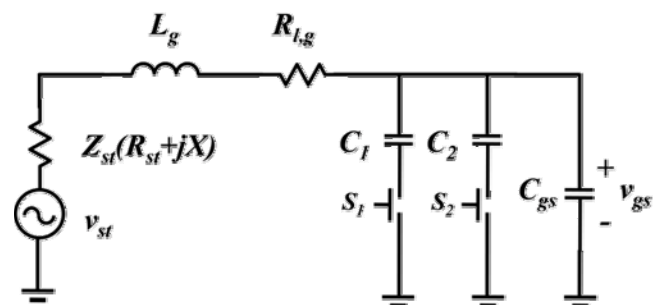


Fig. 2. The equivalent input circuit of the high  $Q$  series resonance low-noise amplifier.

Therefore, a transmission line with proper characteristic impedance and length can produce a low source resistance,  $R_{st}$ , which is the resistive part of  $Z_{st}$ . As a result, high  $Q$  series resonance is obtained. An inductor,  $L_g$ , is used for resonance with capacitance, and the  $R_{l,g}$  is the resistance of the inductor  $L_g$ .

The following analyses (gain and harmonic rejection ratio analysis) were performed with exclusion of the bonding effect. In this work, we minimized this effect by carried out multiple down bonding. Parasitic capacitances (routing parasitic capacitances, pad capacitances) also result in resistive input. If the bonding effect generates several tens of resistive impedance, then the effect must be included in the analysis. In that case, the  $R_{l,g}$  changes to  $R_{l,g} + R_{bond}$ , where  $R_{bond}$  signifies resistive impedance from the bonding effect. The noise figure (NF) analysis is not changed.

### 1. Gain Analysis

The transformed source impedance  $Z_{st}$  can be written as:

$$Z_{st} = Z_0 \frac{R_s + jZ_0 \tan \beta l_{TL}}{Z_0 + jR_s \tan \beta l_{TL}} = R_{st} + jX_{st}. \quad (1)$$

Therefore, the  $Q$  of the circuit can be written as:

$$Q = \frac{1}{\omega_0 C_{in}} \cdot \frac{1}{R_{st} + R_{l,g}}, \quad (2)$$

where  $\omega_0$  is the series resonance frequency,  $C_{in}$  is the equivalent input capacitance (equal to  $C_{tot}$  when the  $X_{st}$  is in the inductive region, and equal to  $C_{tot}/C_{st}$  when the  $X_{st}$  is in the capacitive region and  $C_{st}$  is an equal capacitance to  $X_{st}$ ), and  $R_{l,g}$  is the inductor resistance. If the transmission line is assumed to be lossless, then power is conserved. The input passive network voltage gain  $A_v$  is calculated as:

$$A_v = \left| \frac{v_{gs}}{v_s} \right| = \sqrt{\frac{R_{st}}{R_s}} \cdot \frac{1}{\omega_0 C_{tot}} \cdot \frac{1}{R_{st} + R_{l,g}}. \quad (3)$$

Fig. 3 shows that the  $Q$  and voltage gain are related to the resistance part of the source impedance.

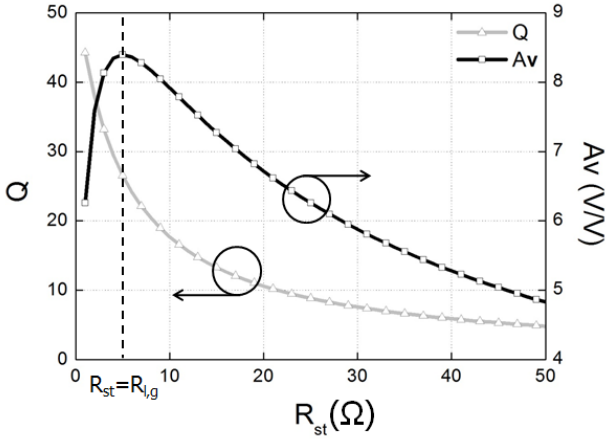


Fig. 3. Calculated  $Q$  and input network voltage gain  $A_v$  versus the resistance part of the source impedance,  $R_{st}$ . (The  $C_{tot} = 0.56$  pF and  $R_{l,g} = 5$   $\Omega$  are assumed.  $\omega_0 = 1.07$  GHz).

The calculated  $Q$  and  $A_v$  are compared with the  $Q$  and  $A_v$  of the L-CS LNA as follows:

$$Q = Q_{L-CS} \cdot \frac{2R_s}{R_{st} + R_{l,g}} \quad (4)$$

and

$$A_v = \sqrt{R_{st} R_s} \cdot \frac{2}{R_{st} + R_{l,g}} \cdot A_{v,L-CS}, \quad (5)$$

where  $Q_{L-CS}$  is  $Q$  of the L-CS LNA and  $A_{v,L-CS}$  is  $A_v$  of the L-CS LNA.

Eqs. (4) and (5) indicate that the HQ-LNA can have a much higher  $Q$  and voltage gain than the L-CS LNA if the source impedance  $R_s$  (usually 50  $\Omega$ ) is much higher than the inductor resistance, and this is correct under several GHz ranges.

### 2. Harmonic Rejection Ratio Analysis

The third HR ratio can be calculated in a similar manner to the gain analysis. The third HR ratio is shown as:

$$HR_{3rd} = 20 \log_{10} \left( \sqrt{\frac{R_{st}}{R_{st3rd}}} \cdot \frac{\left| R_{st3rd} + R_{l,g} + j(X_{st3rd} + 3\omega_0 L_g - \frac{1}{3\omega_0 C_{tot}}) \right|}{R_{st} + R_{l,g}} \right), \quad (6)$$

where  $R_{st3rd}$  is the resistive part of the transformed source impedance at the third harmonic frequency. This equation reveals that if the reactance part is much larger than the  $R_{st3rd}$ , then large  $L_g$ , small  $R_{st}$ , or small  $R_{st3rd}$  makes high HR.

### 3. Noise Figure Analysis

Gain and HR are important factors in an LNA. The derived equations show that gain is maximized when  $R_{st}$  equals  $R_{l,g}$  (usually under several ohms). However, the NF is also an important factor in an LNA, and an optimum  $R_{st}$  value exists for the minimum NF. The noise factor can be calculated in a similar manner to that shown in [10–12]:

$$F = 1 + \frac{R_{l,g}}{R_{st}} + \gamma \chi g_{d0} R_{st} \left( \frac{\omega_0}{\omega_T} \cdot \frac{C_{tot}}{C_{gs}} \right)^2, \quad (7)$$

where

$$\chi = 1 - 2|c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} + \frac{\delta \alpha^2}{5\gamma} (1 + Q_L^2), \quad (8)$$

$$Q_L = \frac{1}{\omega_0 C_{in} R_{st}}. \quad (9)$$

Here,  $\omega_T$  is the unity gain frequency (equal to  $g_m/C_{gs}$ ),  $g_{d0}$  is the zero-bias drain conductance of the device,  $\gamma$  is the coefficient of the channel thermal noise,  $\alpha$  is the ratio between the device transconductance and the zero-bias drain conductance,  $\delta$  is the factor of the induced gate noise, and  $c$  is the correlation coefficient between the induced gate noise and the drain noise.

From (8), the optimum source impedance,  $R_{st\_Fmin}$ , can be determined:

$$R_{st\_Fmin} = \left( \frac{\omega_T}{\omega_0} \cdot \frac{C_{gs}}{C_{tot}} \right) \sqrt{\frac{R_{l,g} + \frac{1}{5C_{in}^2} g_{d0} \left( \frac{1}{\omega_T} \cdot \frac{C_{tot}}{C_{gs}} \right)^2 \delta \alpha^2}{\gamma g_{d0} (1 - 2|c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} + \frac{\delta \alpha^2}{5\gamma})}}. \quad (10)$$

As the  $R_{st}$  of the source impedance decreases to a given point, the noise factor decreases due to the increased gain suppressing the MOSFET channel noise. However, as the resistive part of the source impedance decreases beyond a given point, the inductor resistance and the induced gate noise become the dominant noise sources, and they increase. The optimum  $R_{st}$  depends on the process, bias, and resistance of the inductor.

## III. HQ-LNA IMPLEMENTATION

A HQ-LNA was designed and implemented using 0.13- $\mu\text{m}$  CMOS technology, as shown in Figs. 4 and 5. The amplifiers had cascode configurations to improve the reverse isolation and reduce the Miller capacitance between the gate and the drain of the transistor,  $M_1$ . The LNA was biased at 8 mA with a 1.2-V supply. The transistor size was carefully chosen. A large transistor consumes a great deal of power and generates large gate-source capacitances. On the other hand, a small transistor can easily suffer from other parasitic

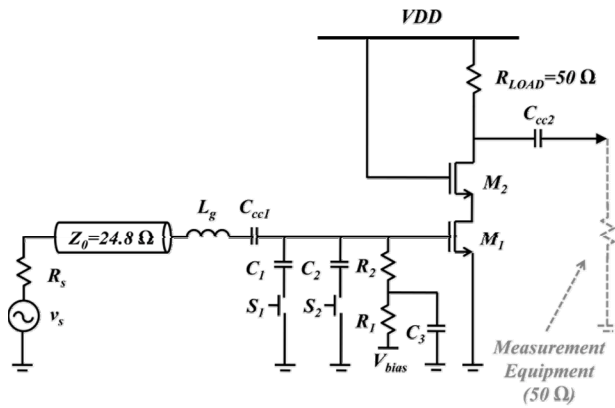


Fig. 4. Complete schematic of the LNA with the proposed technique.

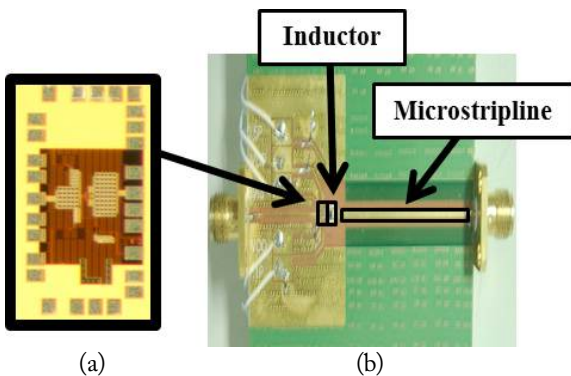


Fig. 5. (a) Chip photograph of the low-noise amplifier (LNA) and (b) photograph of the fabricated LNA on the printed circuit board.

capacitances, including pad capacitance and routing capacitances. The active region of this chip is  $270 \mu\text{m} \times 450 \mu\text{m}$ , excluding pads size.

Next, the proper transmission line was chosen. A  $24.8\text{-}\Omega$  characteristic impedance with  $3.7 \text{ cm}$  length line was selected to transform the source impedance,  $R_s$ , which was  $50 \Omega$ , to  $15.5$ ,  $14.4$ ,  $13.0$ , and  $12.1 \Omega$  at  $0.64$ ,  $0.70$ ,  $0.82$ , and  $1.07 \text{ GHz}$ , respectively.

The inductor,  $L_g$ , and the capacitors,  $C_1$  and  $C_2$ , were chosen to generate series resonance at the above-mentioned frequencies. In our case, the inductor and capacitors were  $39 \text{ nH}$ ,  $0.6 \text{ pF}$ , and  $1.1 \text{ pF}$ , respectively. The switches,  $S_1$  and  $S_2$ , were implemented by MOSFET.

Finally, the load stage was composed of only a  $50 \Omega$  resistor for measurement. This creates a low gain; however, it rarely contributes to the gain-frequency relation. Therefore, it will not interrupt the verification of the high  $Q$  resonance technique. In a practical case, the load stage can be composed of a wideband resonance circuit or high value resistor, and this provides more gain.

Fig. 6 and Table 1 show the simulation results for the HQ-LNA and the conventional L-CS LNA. They have the same architecture (cascade), same transistor size (width and length), same bias voltage ( $0.67 \text{ V}$ ), and same supply voltage ( $1.2 \text{ V}$ ); only the input matching part is different. The

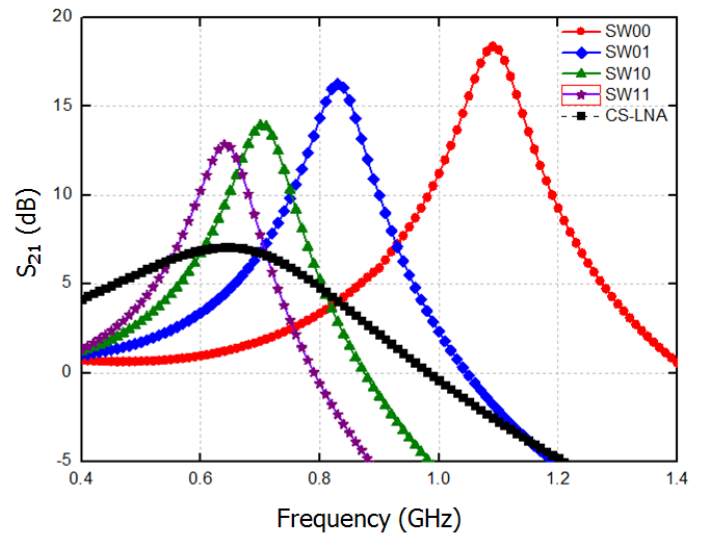


Fig. 6. Simulated gain of the high  $Q$  series resonance low-noise amplifier (HQ-LNA) and conventional the inductively de-generated low-noise amplifier (L-CS LNA).

Table 1. The HQ-LNA and conventional L-CS LNA simulation results

	SW00	SW01	SW10	SW11	L-CS LNA
Frequency (GHz)	1.07	0.82	0.7	0.64	0.64
$S_{21}$ (dB)	18.3	16.1	13.7	12.6	7.1
NF (dB)	2.1	1.4	1.3	1.2	1.3
Third HR (dB)	46	38	33	33	23

LNA = low-noise amplifier, HQ-LNA = high  $Q$  series resonance LNA, L-CS LNA = the inductively de-generated LNA, NF = noise figure, HR = harmonic rejection.

HQ-LNA SW11 mode is compared with the L-CS LNA, and the HQ-LNA exhibited higher gain, higher HR, and lower NF.

In the analysis, the  $R_{st}$  decreased as with the gain and the HR increased as. The simulation results show that. Moreover, as predicted, the SW00 mode NF increased dramati-

Table 2. Comparative summary about the frequency, NF, and third HR of LNAs

	Freq. (GHz)	$S_{21}$ (dB)	NF (dB)	Third HR (dB)	No. of inductors
HQ-LNA					1
SW11	0.64	12.1	2.7	32	
SW10	0.71	13.2	2.9	32	
SW01	0.83	15.4	2.8	35	
SW00	1.07	17.4	3.3	43	
[3]	0.8–6	18–20	3–3.5	No	2
[8]	0.3–0.8	22–27	0.8–4.2 <sup>a</sup>	33	2

NF = noise figure, HR = harmonic rejection, LNA = low-noise amplifier, HQ-LNA = high  $Q$  series resonance LNA.

<sup>a</sup> The NF of [8] is complete receiver NF, and maximum NF is estimated by figure.

cally because the  $R_{sr}$  decreased beyond the optimal value for the minimum NF. In this region, the inductor resistance noise and the gate-induced noise became dominant noise sources.

#### IV. MEASUREMENT RESULTS

Fig. 7 shows the measured scattering ( $S$ ) parameters. Series resonance occurred at 0.64, 0.71, 0.83, and 1.07 GHz, corresponding to the SW11, SW10, SW01, and SW00 modes, respectively. The measured  $S_{21s}$  of the LNA were 12.1, 13.2, 15.4, and 17.4 dB at each resonance frequency with the corresponding SW modes. The measured  $S_{22s}$  were well below  $-10$  dB when the frequency was higher than 0.4 GHz, indicating that the load stage has little effect on  $S_{21}$  when the frequency is higher than 0.4 GHz. Fig. 8 shows the measured NFs. The measured NFs were 2.7, 2.9, 2.8, and 3.3 dB in the SW11, SW10, SW01, and SW00 modes, respectively. The measured third HR ratios are over 30 dB at each mode. The achieved maximum third HR ratio is 43 dB at SW00 mode. These high third HR ratios will relax

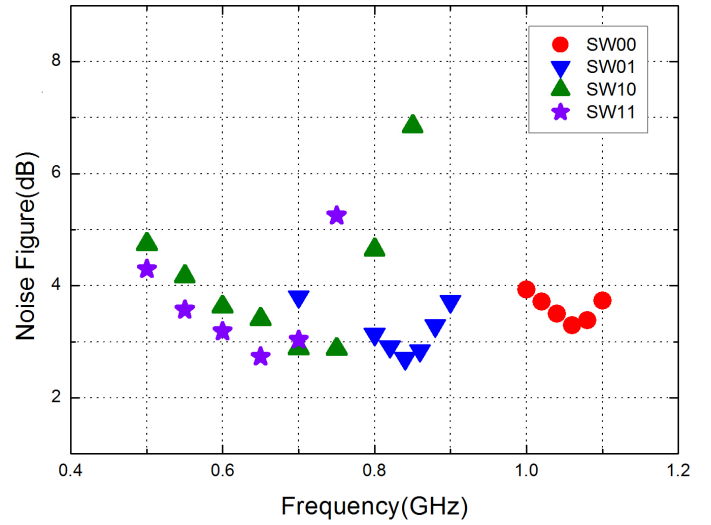


Fig. 8. Measured noise figure of the high Q series resonance low-noise amplifier (HQ-LNA).

the specification of the filter design for an SDR receiver. The gain, NF, and HR results were well matched with the

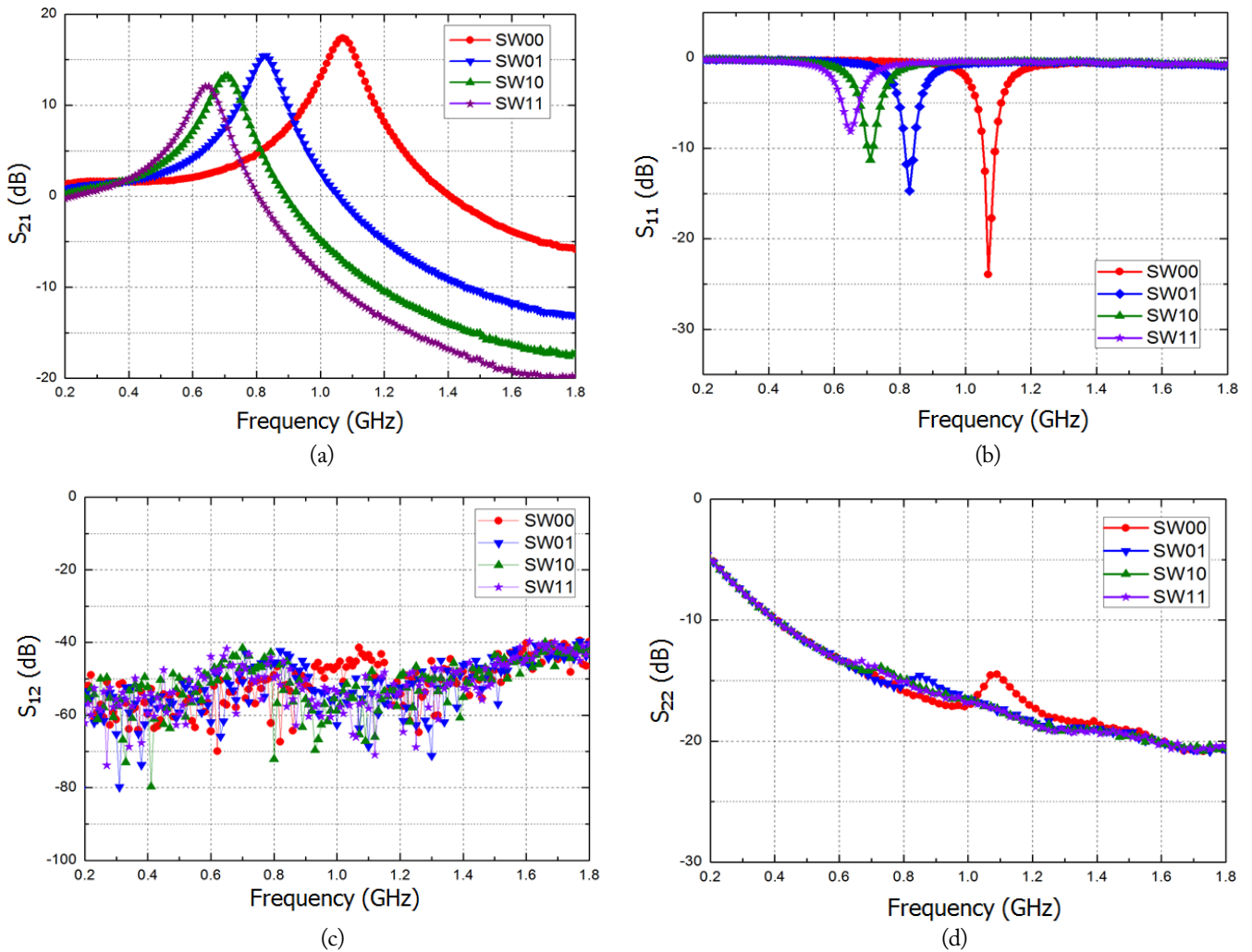


Fig. 7. Measured  $S$ -parameters of the high Q series resonance low-noise amplifier (HQ-LNA): (a)  $S_{21}$ , (b)  $S_{11}$ , (c)  $S_{12}$ , and (d)  $S_{22}$ .



analysis and simulation results.

Linearity was measured by two tone input signals, which are separated 1 MHz from the center frequency at the upper and lower sides in each operating mode. The measured IIP3s were  $-5.7$ ,  $-6.1$ ,  $-8$ , and  $-10.8$  dBm in the SW11, SW10, SW01, and SW00 modes, respectively.

For comparison, Table 2 gives a summary of the measured results of operation frequency, NF, and third HR for several LNAs. A wideband LNA in [3] does not provide third HR. The SW00 mode achieves the highest third HR ratio. HQ-LNA has slightly lower gain, due to it uses 130-nm CMOS process and load stage consists of pure  $50 \Omega$  resistor. This  $50 \Omega$  resistor load provides more precise observation about input network effects; however, it provides low gain. In practice, a load can consist of a resonance circuit or a higher resistor, and it can provide more gain.

## V. CONCLUSION

In this paper, we presented a high  $Q$  input series resonance LNA to obtain high voltage gain, a high HR ratio, and low NF, as well as to support multiband operation for an SDR receiver. This technique was simply achieved by exploiting switchable capacitor banks, one inductor, and a transmission line. The high HR will relax the specification of the filter when using a hard-switching mixer.

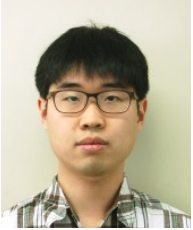
These effects were demonstrated by measurement of the implemented LNA. The LNA supports four operation bands (0.64, 0.71, 0.83, and 1.07 GHz) with high forward gain (12.1, 13.2, 15.4, and 17.4 dB), low NF (2.7, 2.9, 2.8, and 3.3 dB), high third HR ratios (32, 32, 35, and 43 dB), and low power consumption (9.6 mW with 1.2 V). The proposed technique is a promising option for high-performance, low-cost SDR receivers.

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### Byungjoon Kim



received the B.S. degree in electrical engineering from the Seoul National University, Seoul, Korea, in 2009 and is currently working toward the Ph.D. degree. His main interests are RF components and radar system.

### Sangwook Nam (S'87 - M'88 - SM'11)



received the B.S. degree from Seoul National University, Seoul, Korea, in 1981, the M.S. degree from the Korea Advanced Institute of Science and Technology (KAIST), Seoul, Korea, in 1983, and the Ph.D. degree from The University of Texas at Austin, Austin, TX, USA, in 1989, all in electrical engineering. From 1983 to 1986, he was a Researcher with the Gold Star Central Research Laboratory, Seoul, Korea. Since 1990, he has been a Professor with the School of Electrical Engineering and Computer Science, Seoul National University. His research interests include analysis/design of electromagnetic (EM) structures, antennas, and microwave active/passive circuits.

### Duksoo Kim



received the B.S. degree in electrical engineering from the Seoul National University, Seoul, Korea, in 2011 and is currently working toward the Ph.D. degree. His main interests are RF components and radar system.