New Memristor-Based Crossbar Array Architecture with 50-% Area Reduction and 48-% Power Saving for Matrix-Vector Multiplication of Analog Neuromorphic Computing

Son Ngoc Truong and Kyeong-Sik Min*

Abstract—**In this paper, we propose a new memristor-based crossbar array architecture, where a single memristor array and constant-term circuit are used to represent both plus-polarity and minus-polarity matrices. This is different from the previous crossbar array architecture which has two memristor arrays to represent plus-polarity and minus-polarity connection matrices, respectively. The proposed crossbar architecture is tested and verified to have the same performance with the previous crossbar architecture for applications of character recognition. For areal density, however, the proposed crossbar architecture is twice better than the previous architecture, because only single memristor array is used instead of two crossbar arrays. Moreover, the power consumption of the proposed architecture can be smaller by 48% than the previous one because the number of memristors in the proposed crossbar architecture is reduced to half compared to the previous crossbar architecture. From the high areal density and high energy efficiency, we can know that this newly proposed crossbar array architecture is very suitable to various applications of analog neuromorphic computing that demand high areal density and low energy consumption.**

Index Terms—**Memory array circuit, memristor, artificial neural network, synaptic weight, character recognition**

Manuscript received Feb. 18, 2014; accepted May. 8, 2014
School of Electrical Engineering, Kookmin University
E-mail : mks@kookmin.ac.kr

I. INTRODUCTION

As high performance computation is demanded increasingly, the conventional von Neumann architecture becomes less efficient in terms of energy consumption, compared to biological systems such as human brains [1]. To overcome the limitation of von Neumann architecture, neuromorphic systems that can mimic the capabilities of biological perception and information processing have gained more attention since C. Mead introduced the term "neuromorphic engineering" in his pioneering work [2].

For implementing neuromorphic systems, various research activities that are based on CPUs, GPUs, FPGAs, analog circuits, memory circuits, etc. have been carried out both in academia and industry [3-10]. Among them, simple crossbar array architecture has been one of strong candidates for promising neuromorphic architectures, because crossbar architecture can be made with high density and low cost [11].

In realizing crossbar array for neuromorphic systems, nano-scale two-terminal device such as memristors that can emulate synaptic plasticity with high energy efficiency can be a critical element [12, 13]. Memristors mathematically predicted by Leon O. Chua in 1971 as the fourth basic circuit element [14] were experimentally found in 2008 [15]. Since the first prediction of memristors, they have been thought as potential candidate that can mimic various synaptic functions of biological neural systems [12]. This is because memristors can be integrated with 3-D array that may be as dense as neuronal array in human brains [11]. In

addition, memristors that can store analog values are useful in representing synaptic weights to emulate synaptic plasticity [12].

There are several ways that mimic synaptic behavior of human brains using CMOS-memristor hybrid circuits [16-20]. One simple example of the CMOS-memristor hybrid circuits for emulating the synaptic plasticity was proposed by Hui Wang et al. [17], where the artificial synapse was implemented by combining one transistor (1T) with one memristor (1M). Here, the transistor (1T) is used as a selecting device that can choose a specific memristor to be programmed [17]. In the 1T-1M synaptic circuit, the array density is decided by transistor's area not by memristor's area. Thus it seems difficult to realize high-density of 1T-1M array because selection devices such as transistors occupy much larger area than memristors [17]. In addition, in terms of 3-D integration, the 1T-1M array is thought to be more difficult to be stacked layer by layer compared to the passive memristor array that is composed of only passive memristors without any selection devices [17].

A crossbar array that is made of only passive memristors without any selection devices such as diodes and transistors was proposed and analyzed by Miao Hu et al. [20]. They used two memristor crossbar arrays that represent plus-polarity and minus-polarity connection matrices, respectively, for performing matrix-vector multiplication that is the most frequent operation in neuromorphic computing [1, 2].

In this paper, to improve energy efficiency and areal density better than the previous memristor-based crossbar architecture [20], we propose new crossbar array architecture, where both plus-polarity and minus-polarity connection matrices can be realized by single crossbar array and simple constant-term circuit. The new memristor-based neuromorphic architecture with only single crossbar array instead of two crossbar arrays can improve the areal density of crossbar array nearly double. Moreover, the energy efficiency can be better by 48% compared to the previous memristor-based crossbar architecture [21].

II. NEW MEMRISTOR-BASED CROSSBAR ARRAY

Fig. 1(a) shows a simple diagram of neural network with synapse array, in which the input neurons are connected to the output neurons through the synaptic network. Fig. 1(b) shows a conceptual diagram of the previous crossbar architecture of analog neuromorphic computing systems containing both plus-polarity and minus-polarity connection matrices that are represented by the crossbar array of $M^{+}(g^{+}_{j,k})$ and $M^{-}(g^{-}_{j,k})$, respectively [20]. Here $g^{+}_{j,k}$ and $g^{-}_{j,k}$ are memristor's conductance values of the plus-polarity and minus-polarity memristor arrays, respectively. $V_{IN,j}$ is the jth

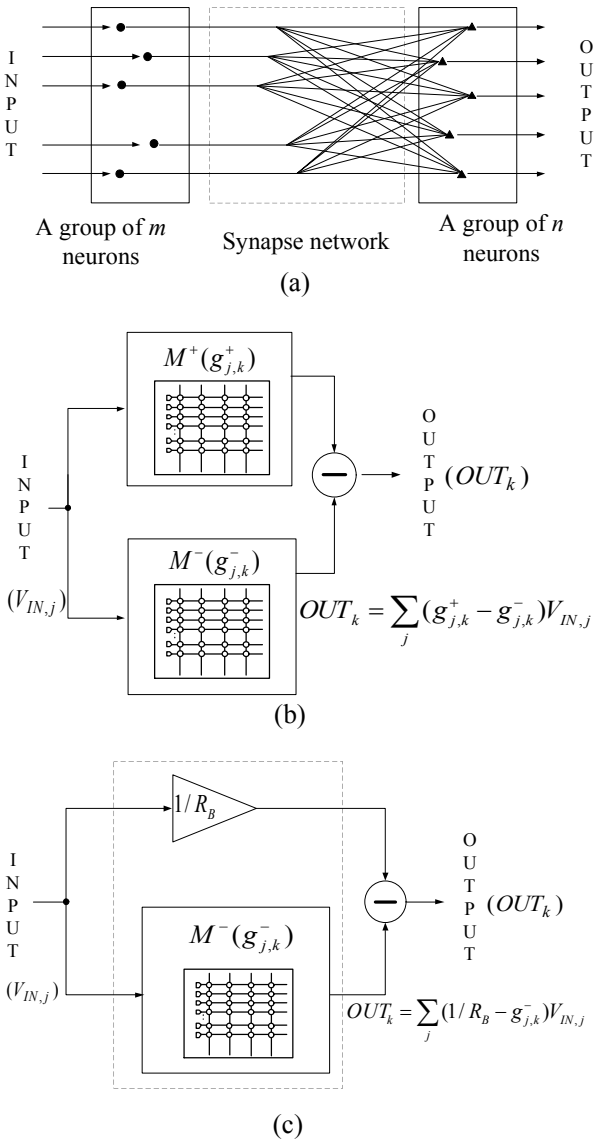

Fig. 1. (a) A simple diagram of neural network with synapse array, (b) A conceptual diagram of the previous memristor-based crossbar architecture with plus-polarity and minus-polarity connection matrices that are represented by the two crossbar arrays of M+(g+j,k) and M-(g-j,k), respectively [20], (c) A conceptual diagram of the proposed memristor crossbar architecture with the single crossbar array of M-(g-j,k) and the constant-term circuit of $1/R_B$.

input voltage which is applied to the connection matrices of $M^+(g+_{j,k})$ and $M^-(g-_{j,k})$. OUT_k is the kth output voltage of Fig. 1(b).

The two crossbar arrays of $M^+(g^+_{j,k})$ and $M^-(g^-_{j,k})$ that are needed to calculate $\left(g^+_{j,k} - g^-_{j,k}\right)V_{IN,j}$ can be replaced with the single crossbar array of $M^-(g^-_{j,k})$ and the constant-term circuit of $1/R_B$. As shown in Fig. 1(c), if we implement $\left(1/R_B - g^-_{j,k}\right)V_{IN,j}$ using the single memristor crossbar array of $M^-(g^-_{j,k})$ and the constant-term circuit of $1/R_B$, we can reduce both the area and power consumption of two crossbar arrays of $M^+(g^+_{j,k})$ and $M^-(g^-_{j,k})$ in Fig. 1(b). Here, if $g^-_{j,k}$ is smaller than $1/R_B$, $1/R_B$-$g^-_{j,k}$ has plus polarity. On the contrary, if $g^-_{j,k}$ is larger than $1/R_B$, $1/R_B$-$g^-_{j,k}$ becomes negative, thus, we can realize both plus and minus polarities as indicated in Fig. 1(c). The obvious advantage illustrated in Fig. 1(c) over Fig. 1(b) implies lower power consumption and smaller area of crossbar array for performing matrix-vector multiplication.

The detailed schematic of memristor-based crossbar arrays of plus-polarity and minus-polarity connection matrices is shown in Fig. 2 [20]. Here $M^+(g^+_{j,k})$ and $M^-(g^-_{j,k})$ are the crossbar arrays of the connection matrices with plus and minus polarities, respectively [20]. $g^+_{1,1}$ is memristor's conductance at the crossing point between the first row and first column of M^+ array. $g^+_{j,k}$ is memristor's conductance of the jth row and kth column of M^+ array. And, $g^-_{1,1}$ and $g^-_{j,k}$ in M^- array are conductance values that are located at the same crossing points with each $g^+_{1,1}$ and $g^+_{j,k}$, respectively, in M^+ array. $V_{IN,1}$ and $V_{IN,2}$ are the input voltages applied to the first row and second row, respectively. $V_{IN,j}$ is the applied voltage for the jth row. $V_{C+,1}$ and $V_{C+,2}$ are the column voltages of the first and second columns, respectively, in M^+ array. $V_{C+,k}$ is for the kth column in M^+ array. Similarly, $V_{C-,1}$, $V_{C-,2}$, and $V_{C-,k}$ are the first, second, and kth column voltages, respectively, in M^- array. G^+_1 and G^-_1 are inverting OP amps for the first columns in M^+ and M^- crossbar array, respectively. R_1 and R_2 are negative-feedback resistors of G^+_1 and G^-_1, respectively. $V_{O+,1}$ and $V_{O-,1}$ are the output voltages of G^+_1 and G^-_1, respectively. G_1 is the difference OP amp that amplifies the difference between $V_{O+,1}$ and $V_{O-,1}$. The output of G_1 is $V_{O,1}$. In Fig. 2, R_3 and R_4 constitute the negative feedback configuration of G_1. R_5 and R_6 act as the voltage divider.

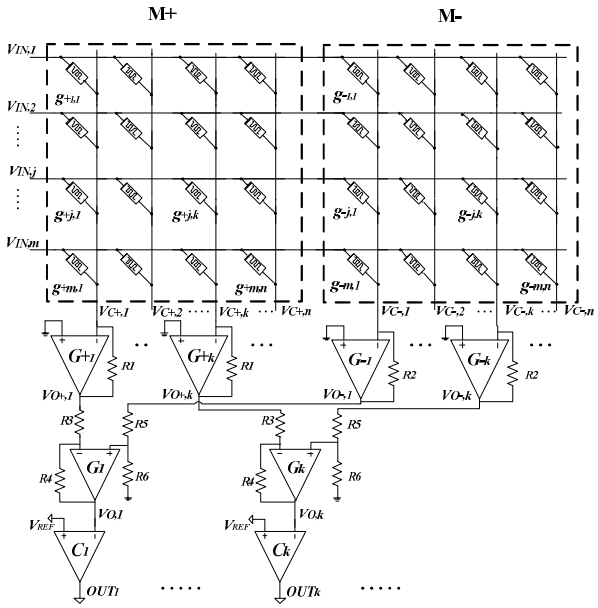

Fig. 2. The previous memristor-based crossbar arrays of $M^+(g^+_{j,k})$ and $M^-(g^-_{j,k})$ that represent plus-polarity and minus-polarity connection matrices, respectively [20].

$V_{O,1}$ enters C_1 that compares $V_{O,1}$ and V_{REF} to decide the final output, OUT_1.

Applying Kirchhoff current and voltage laws to Fig. 2, $V_{O,k}$ can be calculated with the difference of $V_{O+,k}$ and $V_{O-,k}$.

$$V_{O,k} = -V_{O+,k}\left(\frac{R_4}{R_3}\right) + V_{O-,k}\left(\frac{R_6}{R_5+R_6}\right)\left(\frac{R_3+R_4}{R_3}\right)$$
$$where\ V_{O+,k} = -R_1\sum_{j=1}^{m} V_{IN,j}\,g^+_{j,k}\ \ and$$
$$V_{O-,k} = -R_2\sum_{j=1}^{m} V_{IN,j}\,g^-_{j,k} \tag{1}$$

If we assume that R_6=R_4, R_3=R_5, and R_1=R_2, we can obtain:

$$V_{O,k} = \left(\frac{R_4}{R_3}\right)\left(V_{O-,k} - V_{O+,k}\right)$$
$$= \left(\frac{R_4}{R_3}\right)R_1\sum_{j=1}^{m} V_{IN,j}\left(g^+_{j,k} - g^-_{j,k}\right) \tag{2}$$

Each $V_{IN,j}$ is multiplied by a coefficient defined by

$\left(\frac{R_4}{R_3}\right)R_1\left(g^+_{j,k}-g^-_{j,k}\right)$. By choosing the appropriate conductance values of $g^+_{j,k}$ and $g^-_{j,k}$ in Eq. (2), we can obtain either positive or negative polarity of $g^+_{j,k}-g^-_{j,k}$ in Eq. (2). By doing so, the coefficients which are represented by M+ and M- in Fig. 2 can have both positive and negative values according to the programmed conductance values of memristors in the arrays.

Fig. 3 shows a new synaptic array circuit that is composed of the single crossbar array of $M^-(g_{j,k})$ and the constant-term circuit of $1/R_B$. Here $g_{j,k}$ is memristor's conductance at the crossing point between the jth row and kth column. $V_{IN,j}$ is input voltage applied to the jth row. $V_{C,k}$ is column-line voltage on the kth column. The column line, $V_{C,F}$, that is shown in dotted box is added in Fig. 3. The column line, $V_{C,F}$ is connected to all the applied input voltages from $V_{IN,1}$ to $V_{IN,m}$ through R_B. In Fig. 3, $V_{C,F}$ enters G_F that constitutes the inverting OP amp with the negative feedback resistor R_{F1}. The output voltage of G_F is V_F that is connected to all column lines from $V_{C,1}$ to $V_{C,n}$ via R_{F2}, as shown in Fig. 3. By applying Kirchhoff current law to the column line, $V_{C,F}$, we can calculate V_F with Eq. (3).

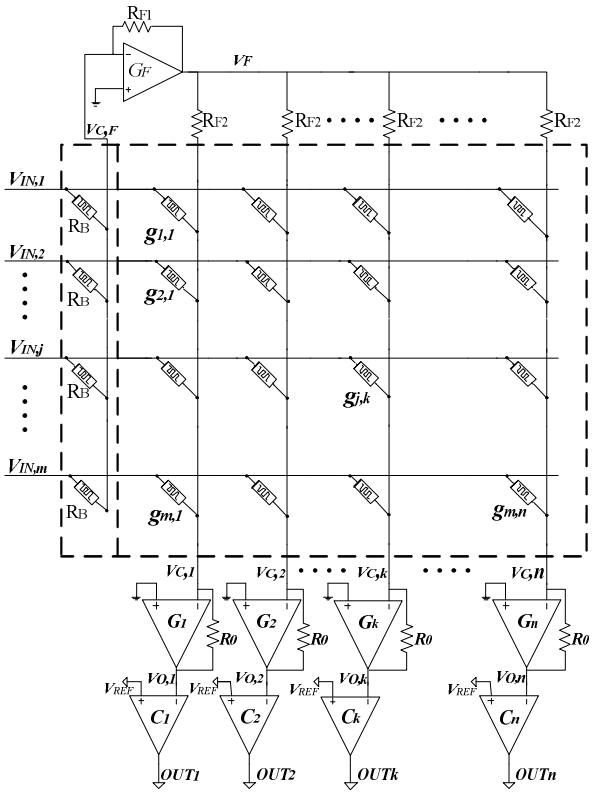

Fig. 3. The proposed memristor-based crossbar architecture, where two crossbar arrays of $M^+(g^+_{j,k})$ and $M^-(g^-_{j,k})$ are replaced with the single crossbar array, $M^-(g_{j,k})$ and the constant-term circuit, $1/R_B$.

$$V_F = -\sum_{j=1}^{m}\frac{R_{F1}}{R_B}V_{IN,j} \tag{3}$$

For the column lines, as you can see in Fig. 3, each column line is connected to its inverting amplifier, from G_1 to G_n. For example, $V_{C,1}$ enters G_1 with the negative feedback resistor, R_0. $V_{O,1}$ is the output voltage of G_1. Similarly, $V_{C,k}$ goes into G_k and $V_{O,k}$ is the output voltage of G_k. $V_{O,k}$ can be calculated with Eq. (4).

$$V_{O,k} = -\left[\sum_{j=1}^{m}\left(R_0\cdot g_{j,k}\cdot V_{IN,j}\right)+\frac{R_0}{R_{F2}}V_F\right] \tag{4}$$

Assuming that R_{F1}=R_{F2} and combining Eq. (4) with Eq. (3), the following Eq. (5) can be obtained as follows.

$$V_{O,k} = -\left[\sum_{j=1}^{m}\left(R_0\cdot g_{j,k}-\frac{R_0}{R_B}\right)V_{IN,j}\right] \tag{5}$$

If $-\left(R_0\cdot g_{j,k}-\frac{R_0}{R_B}\right)$ is defined by the synaptic weight of the jth row and kth column, $w_{j,k}$, we can rewrite Eq. (5) with Eq. (6).

$$V_{O,k}=\sum_{j=1}^{m}w_{j,k}V_{IN,j}$$
$$where\ w_{j,k}=R_0\left(\frac{1}{R_B}-g_{j,k}\right)=R_0\left(\frac{1}{R_B}-\frac{1}{M_{j,k}}\right)$$
$$and\ g_{j,k}=\frac{1}{M_{j,k}} \tag{6}$$

Here $M_{j,k}$ is memristance value between the jth row and the kth column. By keeping R_B to be constant, the synaptic weight, $w_{j,k}$ can be decided by the programmable memristance, $M_{j,k}$ and the feedback

resistor, R_0. Adding the comparator, C_k to the output voltage, $V_{O,k}$, we can decide if the neuron's output of kth column, OUT_k should be activated or not. V_{REF} is the reference voltage for the comparators from C_1 to C_n. When $V_{O,k}$ is larger than V_{REF}, OUT_k becomes 1. On the other hand, if $V_{O,k}$ is smaller than V_{REF}, OUT_k is decided to be 0, as indicated in Eq. (7).

$$OUT_k = \begin{cases} 1, \text{ if } V_{O,k} \geq V_{REF} \\ 0, \text{ if } V_{O,k} < V_{REF} \end{cases} \quad (7)$$

III. SIMULATION RESULTS

1. Training of the Memistor-Based Crossbar Array

The chip-in-the-loop algorithm is used to train the circuit variables in Fig. 3 [19, 22]. The conceptual diagram of the chip-in-the-loop learning algorithm is shown in Fig. 4. Here $w_{j,k}$ is the weighting value associated with the jth input and kth output. t_k is the target value of output. $V_{O,k}$ is the kth output. η is the learning rate. D is a set of training examples. $V_{IN,j}$ is the jth input. According to the chip-in-the-loop algorithm, the target network is learned on the host computer. All the outputs of memristor-based crossbar array are stored in the host computer's memory. $\Delta w_{j,k}$ is calculated using the equation shown in Fig. 4. $w_{j,k}$ is updated by $\Delta w_{j,k}$ until E_d becomes smaller than the predetermined error value.

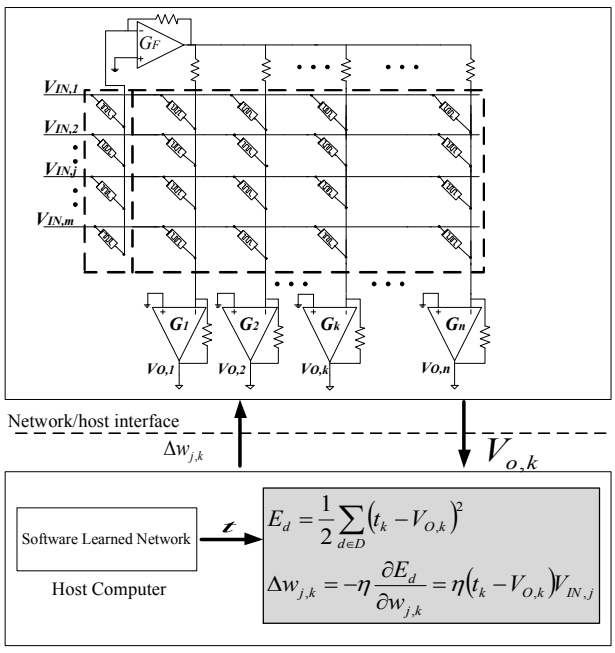

Fig. 4. The chip-in-the-loop algorithm is used to update the synaptic weight, $w_{j,k}$ in the proposed memristor-based crossbar architecture shown in Fig. 3.

2. Application of Character Recognition

The proposed memristor crossbar architecture demonstrated in Fig. 3 is tested for the application of character recognition. Fig. 5(a) shows an image of alphabet 'D' that is composed of 8x8 black-and-white pixels. Similarly, we can have the images of the other characters such as 'A', 'B', 'C', etc. To recognize 26 alphabet characters, the memristor crossbar array is designed to have 26 columns that are corresponding to the alphabet characters from 'A' to 'Z', respectively. Each column of the crossbar array is applied by 64 rows that are given by 64 input voltages, respectively. The 64 input voltages are obtained from 8x8 pixels of the character to be recognized. Let us try to recognize the character 'D', as shown in Fig. 5(a). Before recognizing 'D', the proposed crossbar array in Fig. 3 should be trained to recognize all character images. The memristance values are trained by the chip-in-the-loop learning algorithm that is shown in Fig. 4.

Fig. 5(c) shows the simulation result of character recognition for the previous crossbar array architecture that is shown in Fig. 2. From this Fig. 5(c), we can see that the output voltage of the 4th column, $V_{O,4}$ in the previous crossbar array, is activated for the input vector of character 'D'. In Fig. 5(c), we tested the input vectors from the character 'A' to the character 'Z' to the previous crossbar architecture in Fig. 2.

The simulation result of the proposed new crossbar architecture is shown in Fig. 5(d). Comparing Figs. 5(c) and (d), we can know that the discrepancy in $V_{O,4}$ between the previous crossbar architecture and the proposed architecture is less than 2% in average from the character 'A' to the character 'Z'. This comparison tells us that the performance of character recognition of the proposed crossbar architecture is the same with the previous crossbar architecture. In Figs. 5(c) and (d), V_{REF} means the threshold voltage for recognizing the target character. The simulation results that are shown in Figs. 5(c) and (d) are obtained by the SPECTRE simulator that is provided by Cadence Design Systems Inc. In this work,

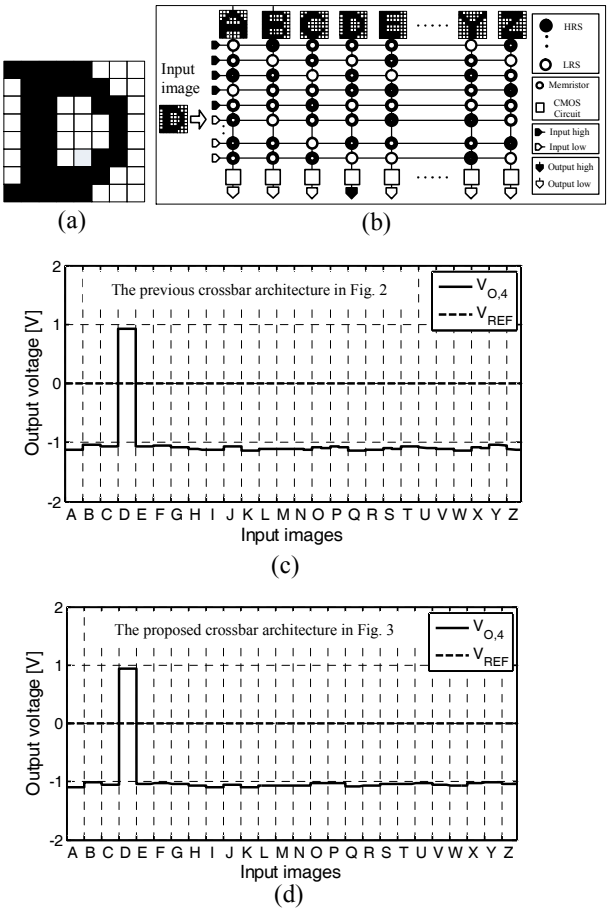

Fig. 5. (a) The 8x8 pixel image of character 'D', (b) The schematic of the character recognition circuit that is based on the memristor-based crossbar architecture for training to recognize the character 'D', (c) The simulation result of character recognition for the previous memristor-based crossbar architecture that has two crossbar arrays of $M^+(g^+_{j,k})$ and $M^-(g^-_{j,k})$ in Fig. 2, (d) The simulation result of character recognition for the proposed memristor-based crossbar architecture that has the single crossbar array of $M^-(g_{j,k})$ and the constant term, $1/R_B$. Here V_{REF} means the threshold voltage for recognizing the target character.

the memristor-CMOS hybrid circuits are simulated by SPECTRE using the memristor's Verilog-A model [23] and the CMOS model parameters which were given by SAMSUNG 0.13-μm process technology.

In Fig. 6, we compared the power consumption between the previous crossbar architecture in Fig. 2 and the proposed crossbar architecture in Fig. 3 in recognizing 26 alphabet characters from 'A' to 'Z'. The power consumption of the proposed crossbar is 0.5211 mW in average for 26 characters. This power consumption is smaller by 48% than the power consumption of the previous architecture that consumes

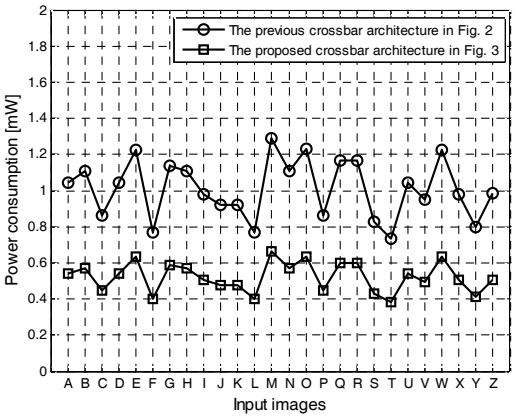

Fig. 6. Comparison of power consumption between the previous crossbar architecture and the proposed crossbar architecture for 26 characters from 'A' to 'Z'.

1.0098 mW. The smaller amount of power consumption in the proposed crossbar in Fig. 3 is mainly due to the fact that only single crossbar array is used instead of two arrays in Fig. 2.

V. CONCLUSIONS

In this paper, we proposed the new memristor-based crossbar architecture with the single crossbar array and the constant-term circuit of $1/R_B$. This is different from the previous crossbar architecture that has two M^+ ($g^+_{j,k}$) and $M^-(g^-_{j,k})$ arrays representing the positive and negative connection matrices. The proposed crossbar architecture was tested and verified to have the same performance with the previous crossbar architecture for the application of character recognition. For the areal density, the proposed crossbar architecture can have double density than the previous architecture, because single array is used instead of two arrays. Moreover, the power consumption of the proposed architecture can be smaller by 48% than the previous one because the number of memristors in the proposed crossbar architecture is only half smaller than the previous crossbar. From this high areal density and high energy efficiency, we can know that the newly proposed crossbar architecture is very suitable to various applications of analog neuromorphic computing that demand high areal density and high energy efficiency.

ACKNOWLEDGMENTS

The work was financially supported by NRF-2011-220-D00089, NRF-2011-0030228, NRF-2013K1A3A1-A25038533, NRF-2013R1A1A2A10064812, and BK Plus with the Educational Research Team for Creative Engineers on Material-Device-Circuit Co-Design (Grant No: 22A20130000042), funded by the National Research Foundation of Korea (NRF). The CAD tools were supported by IC Design Education Center (IDEC), Daejeon, Korea.

REFERENCES

[1] C. Mead, "Neuromorphic electronic systems," *Proceedings of the IEEE*, vol. 78, no. 10, pp. 1629-1636, Oct. 1990.

[2] C. Mead, Analog VLSI and neural system, *Addison-Wesley*, 1989.

[3] I. P. Morns and S. S. Dlay, "Analog design of a new neural network for optical character recognition," *IEEE Trans. Neural Netw.*, vol. 10, no. 4, pp. 951-953, Jul. 1999.

[4] J. B. Lont and W. Guggenbühl, "Analog CMOS implementation of a multilayer perceptron with nonlinear synapses," *IEEE Trans. Neural Network, vol. 3, no. 3, May 1992.*

[5] J. Mirsa and I. Saha, "Artificial neural networks in hardware: A survey of two decades of progress," *Neurocomputing*, vol .74, iss. 1-3, pp. 239-255, Dec. 2010.

[6] K. Mohamad, M. F. O. Mahmud, F. H. Adnan, and W. F. H. Abdullah, "Design of single neuron on FPGA," *IEEE Symposium on Humanities, Science and Engineering Research*, pp. 133-136, Jun. 2012.

[7] S. Himavathi, D. Anitha, and A. Muthuramalingam, "Feedforward neural network implementation in FPGA using layer multiplexing for effective resource utilization," *IEEE Trans. Neural Netw.*, vol. 18, no. 3, pp. 880-888, May 2007.

[8] S. A. Al-Kazzaz, "FPGA implementation of artificial neuron: Comparison study," *International Conference on Information and Communication Technologies*, pp. 1-6, Apr. 2008.

[9] J. M. Granado, M. A. Vega, R. Pérez, J. M. Sánchez, and J. A. Gómez, "Using FPGAs to implement artificial neural networks," *IEEE International Conference on Electronics, Circuit and System*, pp. 934-937, Dec. 2006.

[10] T. Shima, T.Kimura, Y.Kamatani, T.Itakura, Y.Fujita, and T.Iida, "Neuro chips with on-chip back-propagation and/or Hebbian learning," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1868-1875, Dec. 1992.

[11] C. Kügeler, M. Meier, R. Rosezin, S. Gilles, and R. Waser, "High density 3D memory architecture based on the resistive switching effect," *Solid State Electron*, vol. 53, no. 12, pp. 1287-1292, Dec. 2009.

[12] S. H. Jo, T. Chang, I. Ebong, B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett*., vol. 10, no. 4, pp. 1297-1301, Mar. 2010.

[13] W. Lu, K. H. Kim, T. Chang, and S. Gaba, "Two-terminal resistive switches (memristors) for memory and logic applications," *Design Automation Conf.,* pp. 217-223, Jan. 2011.

[14] L. O. Chua, "Memristor – the missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507-519, Sep. 1971.

[15] D. B. Strukov, G. S. Sinder, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80-83, May 2008.

[16] Y. Kim and K. Min, "Synaptic weighting circuits for cellular neural networks," *13th International Workshop on Cellular Nanoscale Networks and Their Applications,* pp. 1-6, Aug. 2012.

[17] H. Wang, H. Li, and R. E. Pino, "Memristor-based synapse design and training scheme for neuromorphic computing architecture," *International Joint Conference on Neural Networks*, pp. 1-5, Jun. 2012.

[18] H. Kim, M, Pd. Sad, C. Yang, T. Roska, and L. O. Chua, "Neural synapse weighting with a pulse-based memristor circuit," *IEEE Trans. Circuit and System*, vol. 59, no. 1, pp. 148-158, Jan. 2012.

[19] S. P. Adhikari, C. Yang, H. Kim, and L. O. Chua, "Memristor bridge synapse-based neural network and its learning," *Trans. Neural Network and Learning System*, vol. 23, no. 9, pp. 1426-1435, Sep. 2012.

[20] M. Hu, H, Li, Q. Wu, G. S. Rose, and Y. Chen, "Memristor crossbar based hardware realization of BSB recall function," *International Joint*

Conference on Neural Networks, pp. 1-7, Jun. 2012.

[21] K. Min, "Memristor circuits for neuromorphic systems," *Workshop on Memristor-based Systems for Neuromorphic Applications*, Turin in Italy, Sep. 2013.

[22] S. M. Tam, B. Gupta, H. A. Castro, and M. Holler, "Learning on analog VLSI network chip," *in Proc. IEEE Int. Conf. Syst., Man and Cybern*., pp. 701-703, Nov. 1990.

[23] S. J. Ham, H. S. Mo, and K. S. Min, "Low-power $V_{DD}/3$ write scheme with inversion coding circuit for complementary memristor array," *IEEE Trans. Nanotechnology,* vol. 12, no. 5, pp. 851-857, Sep. 2013.

Son Ngoc Truong received the B.S. and M.S. degrees in Electronic Engineering from The University of Technical Education Ho Chi Minh City, Vietnam, in 2006 and 2011, respectively. He is currently working toward the Ph.D degree at Kookmin University, Seoul, Korea. His research interests include circuit design, memristor and its application to neuromorphic systems.

Kyeong-Sik Min received the B.S. degree in Electronics and Computer Engineering from Korea University, Seoul, Korea, in 1991, and the M.S.E.E. and Ph.D. degrees in Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1993 and 1997, respectively. In 1997, he joined Hynix Semiconductor Inc., where he was engaged in the development of low-power and high-speed DRAM circuits. From 2001 to 2002, he was a research associate at University of Tokyo, Tokyo, Japan, where he designed low-leakage memories and low-leakage logic circuits. In September 2002, he joined the faculty of Kookmin University, Seoul, Korea, where he is currently a Professor in the School of Electrical Engineering. He was a visiting professor at University of California, Merced, from Aug. 2008 to July 2009. Prof. Min served on various technical program committees such as Asian Solid-State Circuits Conference (A-SSCC), International SoC Design Conference (ISOCC), and Korean Conference on Semiconductors (KCS). He and his students received IDEC CAD & Design Methodology Award (2011), IDEC Chip Design Contest Award (2011), and IDEC Chip Design Contest Award (2012). He is a member of Institute of Electrical and Electronics Engineers (IEEE), Institute of Electronics Engineers of Korea (IEEK), and Institute of Electronics, Information, and Communication Engineers (IEICE) in Japan. His research interests include low-power VLSI, memory design, and power IC design.