A Low-Jitter Phase-Locked Loop Based on a Charge Pump Using a Current-Bypass Technique

Yongsam Moon

Abstract—**A charge-pump circuit using a current-bypass technique, which suppresses charge sharing and reduces the sub-threshold currents, helps to decrease phase-locked loop (PLL) jitter without resorting to a feedback amplifier. The PLL shows no stability issues and no power-up problems, which may occur when a feedback amplifier is used. The PLL is implemented in 0.11-μm CMOS technology to achieve 0.856-ps RMS and 8.75-ps peak-to-peak jitter, which is almost independent of ambient temperature while consuming 4 mW from a 1.2-V supply.**

Index Terms—**Phase-locked Loop, charge pump, sub-threshold current, charge sharing, jitter**

I. INTRODUCTION

Phase-locked loops (PLLs) have been typically employed in communication integrated-circuits and data interfaces for clock generation and clock recovery. One of the most important PLL characteristics is jitter, which is generated in both transmitter and receiver. Transmitter clock signals are generated by a transmitter-side PLL (TXPLL). Since these clocks switch the serializer, the outgoing data stream inherits the jitter of TXPLL-generated clock signals. Receiver clock signals sample the incoming data with their own jitter. Thus, the equivalent jitter is the sum of the jitter components in both transmitter and receiver. Because a transceiver operates at higher frequencies and the bit time becomes shorter, the jitter will occupy a greater portion of the bit time and then the equivalent eye-opening will narrow. Therefore, for a lower bit-error rate (BER), jitter must be reduced in both the transmitter and receiver as the frequency increases.

However, in deep submicron CMOS technology (e.g. 0.11-μm CMOS technology used in this design), switch transistors of a charge pump in a PLL exhibit a considerable sub-threshold current when they turn off, thereby injecting leakage current into a loop filter and generating a noisy ripple on a PLL control voltage. Therefore, the PLL jitter increases.

In this paper, a charge pump with reduced sub-threshold current is proposed. This paper is organized as follows. Section II discusses the imperfections and solutions of conventional charge-pump circuits. Section III presents the proposed charge-pump circuit for low sub-threshold currents. The experimental results are provided in Section IV. Finally, Section V concludes and summarizes this paper.

II. CONVENTIONAL CHARGE-PUMP CIRCUITS

1. Improving Matching between UP/DN Currents

As shown in Fig. 1(a), a conventional PLL consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a divider. Several imperfections in the charge-pump circuit lead to high ripple on the PLL control voltage (*Vctrl*) even in the locked state. Among these non-idealities, the major issue is the mismatch between the up (UP) and down (DN) currents due to channel-length modulation of the current sources. The process, voltage,

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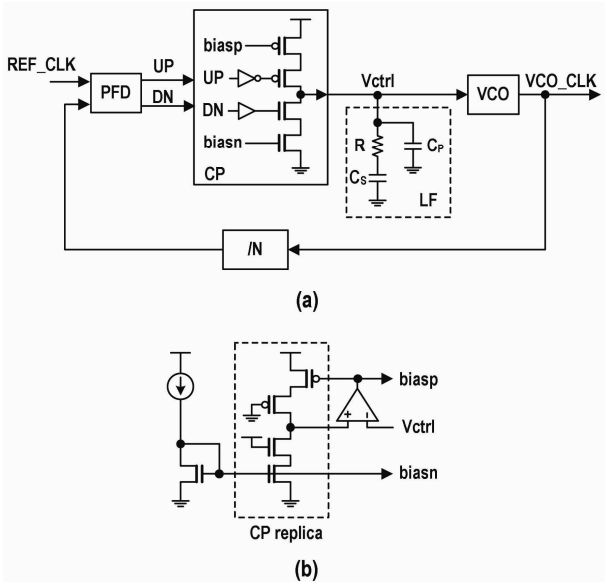


Fig. 1. (a) Block diagram of a conventional PLL, (b) a charge-pump bias circuit.

and temperature (PVT) variations of *Vctrl* inevitably lead to opposite changes in the drain-source voltages of the UP and DN current sources, thereby incurring a large mismatch.

This issue can be solved by introducing feedback with a single op-amp into the biasing scheme as shown in Fig. 1(b) [1, 2]. The op-amp senses *Vctrl* and compares it with the drain voltage of the switch transistors in a CP replica circuit. If this drain voltage is higher than *Vctrl*, the op-amp output (*biasp*) increases and the UP current of the CP replica circuit decreases slightly, forcing both the UP and DN currents of the charge-pump circuit to be almost equal, regardless of the output voltage.

2. Sub-threshold Current Issue

Another problem with a conventional charge pump is sub-threshold current. If UP and DN signals are zero, the switch transistors (MP2 and MN2) turn off and the UP/DN currents are expected to be zero. However, in deep submicron technology, considerable sub-threshold currents ($I_{up.sub}$ and $I_{dn.sub}$) exist as shown in Fig. 2, although the switch transistors are off. The sub-threshold current of MN2 ($I_{dn.sub}$) is approximated with the following expression:

$$I_{dn.sub} = I_S e^{\frac{V_{GS}-V_{TH}}{n \cdot kT/q}} \left(1 - e^{-\frac{V_{DS}}{kT/q}}\right)\left(1 + \lambda V_{DS}\right) \qquad (1)$$

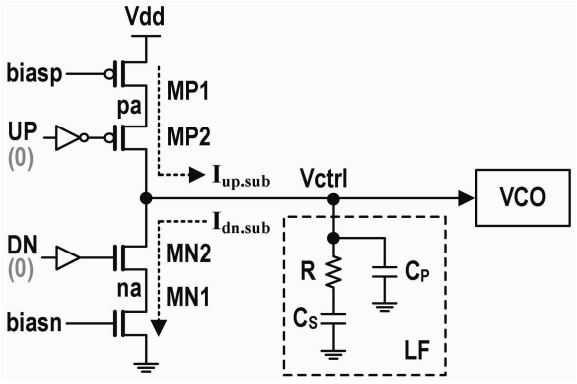


Fig. 2. Sub-threshold currents of a conventional charge-pump circuit.

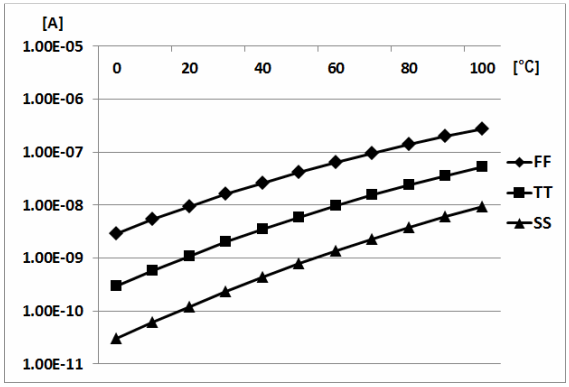
Here, the equation of the sub-threshold current of MP2 ($I_{up.sub}$) is omitted for simplicity. As shown in Fig. 2, when the switch transistors (MP2 and MN2) are off, MP1 charges node *pa* to *Vdd* and MN1 discharges node *na* to ground. Therefore, the gate-source voltages of the switch transistors are almost zero. The sub-threshold current of MN2 can be expressed as follows (here, V_{DS} of MN2 is *Vctrl*):

$$I_{dn.sub@V_{GS}=0\&V_{DS}=Vctrl} = I_S e^{\frac{-V_{TH}}{n \cdot kT/q}} \left(1 - e^{-\frac{Vctrl}{kT/q}}\right)\left(1 + \lambda Vctrl\right) \qquad (2)$$

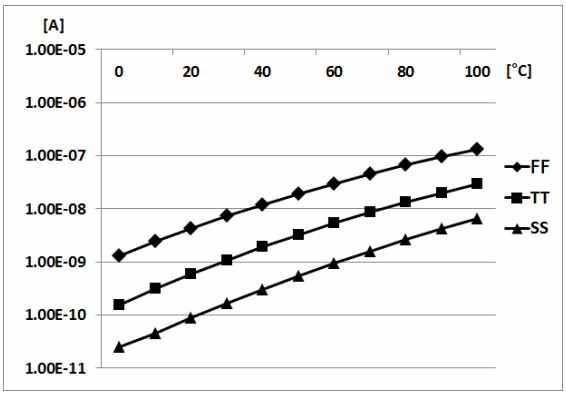
As shown in in Fig. 3, simulations using 0.11–μm CMOS technology show that the fast-fast (FF) process-corner model-parameter exhibits relatively larger sub-threshold currents compared with the typical-typical (TT) or slow-slow (SS) process-corner model-parameter at the same temperature. The reason is that an FF process-corner transistor has the smaller threshold voltage (V_{TH}). These results coincide with Eq. (2): the sub-threshold currents increase with the decrease in V_{TH}. As also shown in Fig. 3, if temperature is swept, V_{TH} generally decreases with the temperature, allowing the sub-threshold currents to increase. These sub-threshold currents are injected into a loop filter and generating a noisy ripple on *Vctrl*. Therefore, the sub-threshold currents should be reduced.

3. Reducing Sub-threshold Current

Fig. 4 shows a charge-pump circuit with a unity-gain



(a)



(b)

Fig. 3. (a) UP sub-threshold current ($I_{up.sub}$), (b) DN sub-threshold current ($I_{dn.sub}$) of a conventional charge-pump circuit.

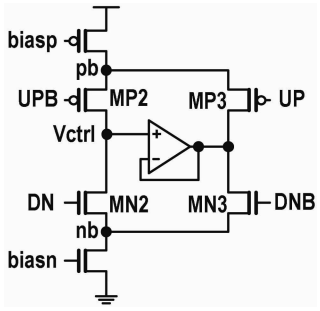


Fig. 4. A charge-pump circuit with a unity-gain amplifier.

amplifier. This circuit was originally designed to suppress charge sharing [3, 4]. As shown in Fig. 4, nodes *pb* and *nb* are connected to *Vctrl* by auxiliary switch transistors (MP3 and MN3) after phase comparison is finished. At the next phase-comparison instant, the main switch transistors (MP2 and MN2) turn on and the nodes *pb* and *nb* start with a voltage equal to *Vctrl*. Therefore, very little charge-sharing can occur between *Vctrl* and the parasitic capacitances at nodes *pb* and *nb*.

When the main switch transistors (MP2 and MN2) turn off, the auxiliary switch transistors (MP3 and MN3) turn on and the voltage of nodes *pb* and *nb* is set to *Vctrl*. Therefore, V_{GS} of MN2 is '$-Vctrl$' and V_{DS} of MN2 is nearly zero. Therefore, the sub-threshold current of MN2 ($I_{dn.sub}$) can be expressed with Eq. (3). Compared with Eq. (2), Eq. (3) shows a much reduced sub-threshold current.

$$I_{dn.sub@V_{GS}=-Vctrl\&V_{DS}\approx 0} \approx I_S e^{\frac{-Vctrl-V_{TH}}{n\cdot kT/q}}\left(1-e^{-\frac{0}{kT/q}}\right) \tag{3}$$

In conclusion, this unity-gain amplifier and the auxiliary switch transistors play a role in not only suppressing charge sharing but also reducing sub-threshold currents. However, the unity-gain amplifier may bring some operational problems. Generally speaking, *Vctrl* can have a very wide voltage range according to the PVT variations. So, the unity-gain amplifier needs to work over all the PVT variations and especially over an almost rail-to-rail range of *Vctrl*. However, the unity-gain amplifier is a feedback circuit so it may have stability issues in a specific PVT corner or at a specific *Vctrl*. In particular, the unity-gain amplifier may malfunction in a power-up state, resulting in *Vctrl* being stuck to ground or *Vdd*.

III. Proposed Charge-Pump Circuit using a Current-Bypass Technique

The proposed charge-pump circuit is shown in Fig. 5. Two current bypasses are attached to the original circuit. The UP-current bypass consists of MN4, MN5, MP6, MP1 transistors. The DN-current bypass consists of MP4, MP5, MN6, and MN1 transistors. The transistors in the same row have the same transistor sizes as Eq. (4):

$$\begin{aligned}&(W/L)_{MP1}=(W/L)_{MP4},\\&(W/L)_{MP2}=(W/L)_{MP5}=(W/L)_{MP6},\\&(W/L)_{MN2}=(W/L)_{MN5}=(W/L)_{MN6}, \text{ and}\\&(W/L)_{MN1}=(W/L)_{MN4}.\end{aligned} \tag{4}$$

When UP = '0' and DN = '0', both the current bypasses turn on as shown in Fig. 6(a) and the drain

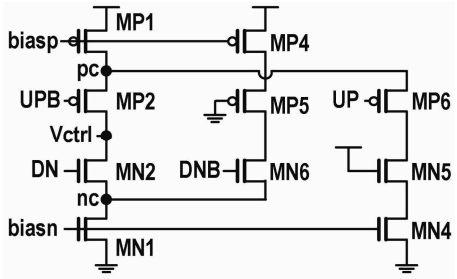


Fig. 5. The proposed charge-pump circuit using a current-bypass technique.

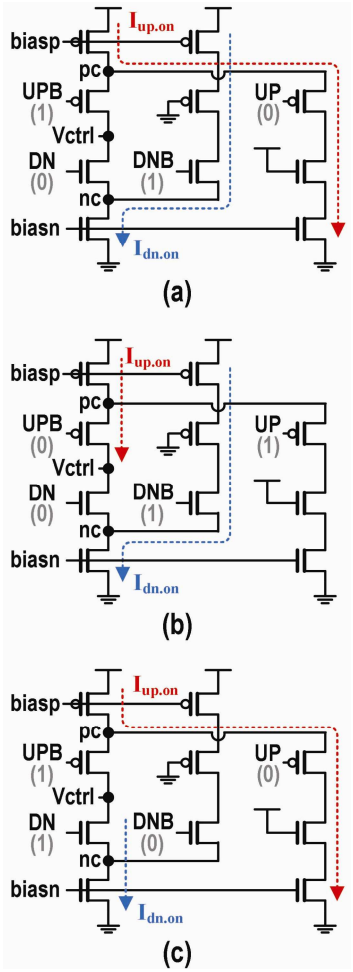


Fig. 6. The current bypasses of the proposed charge-pump circuit (a) when UP = '0' and DN = '0', (b) when UP = '1' and DN = '0', and (c) when UP = '0' and DN = '1'.

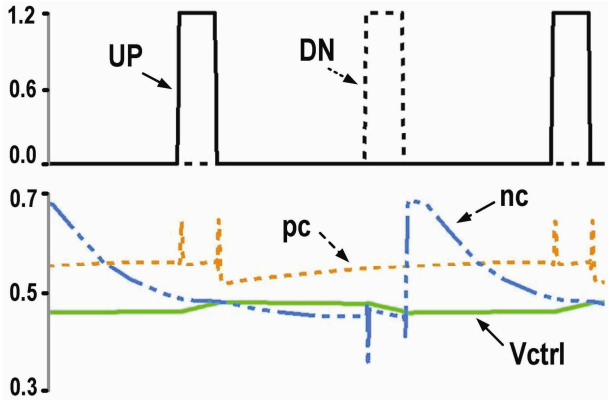
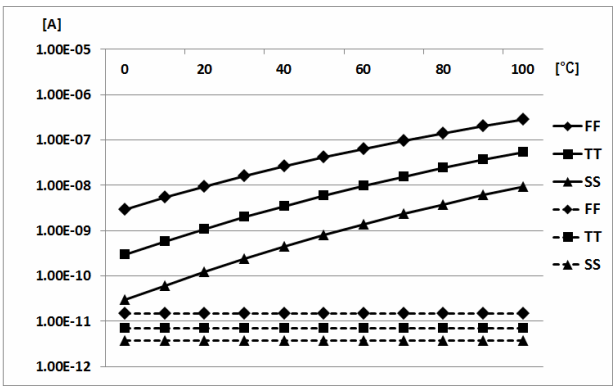
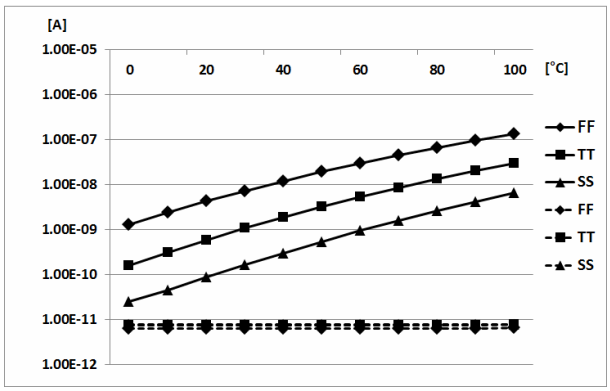


Fig. 7. The simulated voltage waveforms of the proposed charge-pump circuit.



(a)



(b)

Fig. 8. (a) UP sub-threshold current ($I_{up.sub}$), (b) DN sub-threshold current ($I_{dn.sub}$) of the proposed charge-pump circuit. (They are indicated by dotted lines.)

voltages of the transistors in both the current bypasses are close to *Vctrl* since MN5, MP6, MP5, and MN6 transistors operate in linear region with small turn-on resistance. So, the voltages of nodes *pc* and *nc* stay close to *Vctrl* as shown in Fig. 7. V_{GS} of MN2 is close to '$-Vctrl$' and V_{DS} of MN2 is nearly zero. Therefore, the sub-threshold currents of the proposed circuit are reduced to be similar to those of the charge-pump circuit with a unity-gain amplifier in Fig. 4.

When UP becomes '1' and switch transistor MP2 in the main UP-current path turns on as shown in Fig. 6(b), node *pc* starts with a voltage close to *Vctrl* as shown in

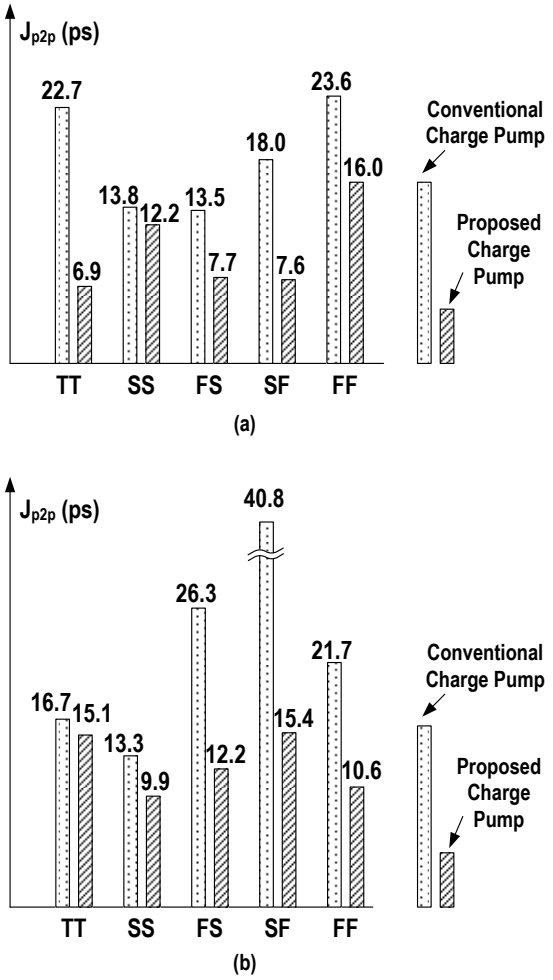


Fig. 9. Peak-to-peak jitter of a 1.5-GHz VCO clock in various process corners (a) at 0°C, (b) at 100°C.

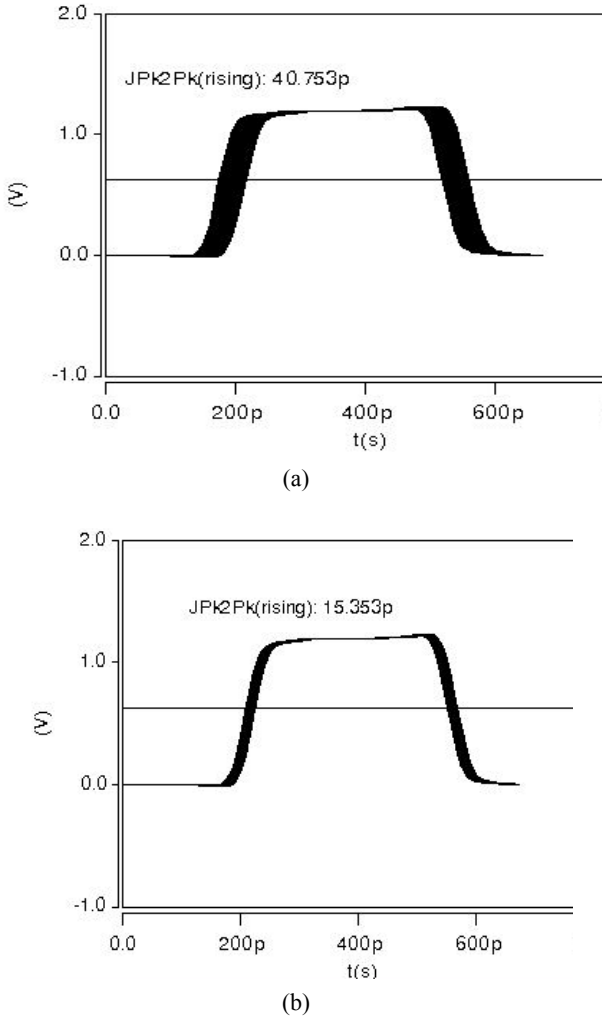


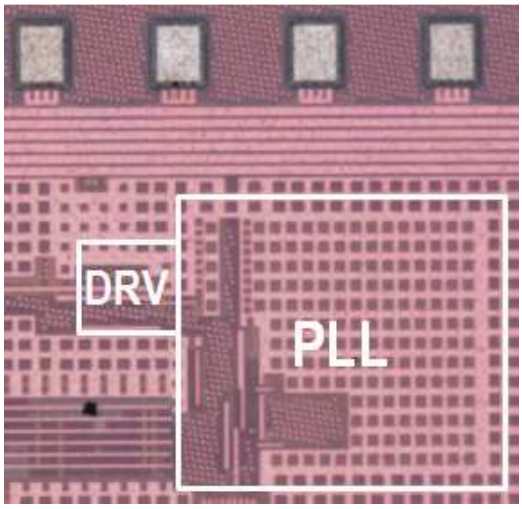
Fig. 10. Simulated eye diagrams and peak-to-peak jitter of the VCO clock in the SF process corner at 100°C using (a) the conventional charge pump and (b) the proposed charge pump.

Fig. 7. When DN becomes '1' and switch transistor MN2 in the main DN-current path turns on as shown in Fig. 6(c), node *nc* starts with a voltage close to *Vctrl* as shown in Fig. 7. Therefore, very little charge-sharing can occur.

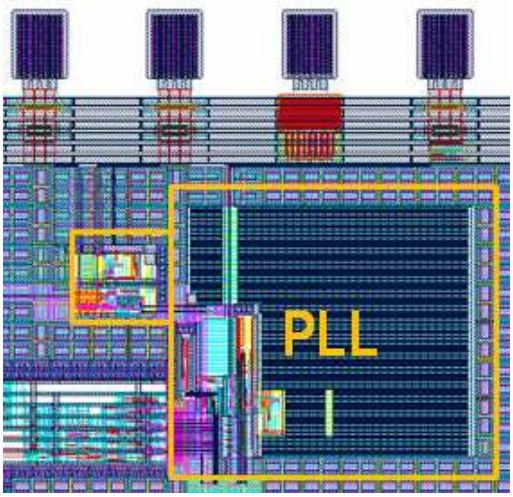
According to the simulation results as shown in Fig. 8, the proposed circuit has lower sub-threshold currents (indicated by dotted lines) whereas the original circuit in Fig. 1 has higher sub-threshold currents (indicated by solid lines). The sub-threshold currents of the proposed circuit are around 10 pA and show little dependency on process and temperature variations.

In order to evaluate the effect of the proposed charge pump on jitter, a test circuit for simulation was set up using the PLL configuration shown in Fig. 1 with a 30-MHz reference clock (*REF_CLK*) and a division ratio (*N*) of 50. Simulations were repeated using the conventional charge pump and the proposed charge pump. Fig. 9 shows peak-to-peak jitter of a 1.5-GHz VCO clock (*VCO_CLK*) in various process corners such as TT, SS, FS (fast NMOS and slow PMOS), SF (slow NMOS and fast PMOS), and FF. Fig. 9(a) shows the jitter at a temperature of 0°C and Fig. 9(b) at a temperature of 100°C.

Simulation results show that the proposed charge pump exhibits relatively lower jitter than the conventional charge pump. Especially in the SF process corner and at 100°C, the conventional charge pump shows the maximum peak-to-peak jitter of 40.8 ps as shown in Fig. 10(a). The reason is that the difference between the UP and DN sub-threshold currents ($I_{up.sub}$ and $I_{dn.sub}$) is the largest. By contrast, the proposed charge pump shows a reduced amount of 15.4ps as shown in Fig. 10(b).



(a)



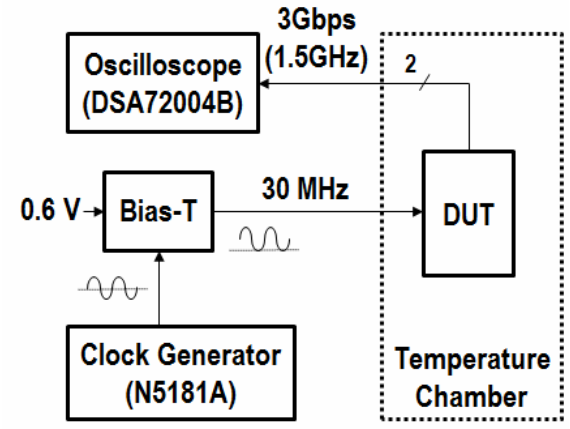
(b)

Fig. 11. (a) Prototype-chip microphotograph, (b) the corresponding layout pattern.

IV. Experimental Results

Fig. 11(a) shows a microphotograph and Fig. 11(b) shows the corresponding layout pattern of the prototype chip. The prototype chip includes a PLL and an output driver. The output driver receives the 1.5-GHz VCO clock (*VCO_CLK*) from the PLL and transmits a 3.0-Gbps differential clock (1010) pattern through the cables. The prototype chip has been fabricated with 0.11–μm 1-poly 6-metal logic CMOS technology. Compared with the conventional charge pump, the layout area and current consumption of the proposed charge pump increased by 100 μm^2 and 200 μA, respectively. The active area of the PLL is 288 μm × 270 μm. The power

(a)



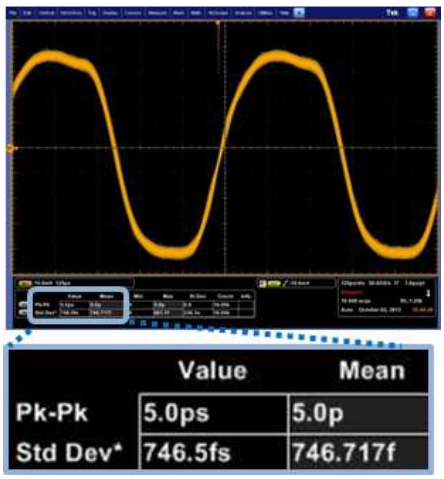
(b)

Fig. 12. (a) Photograph, (b) configuration of the measurement setup.

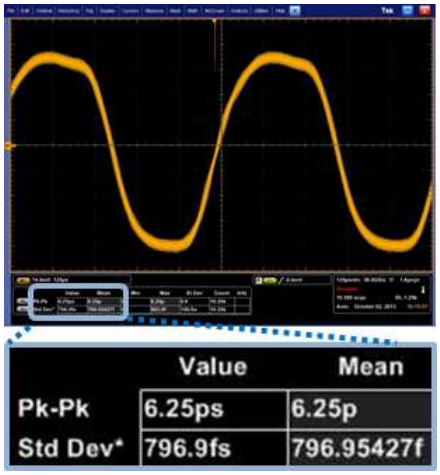
dissipation is approximately 4 mW (excluding the output driver) with a 1.2-V supply voltage. The die is directly attached to a test board in a chip-on-board (COB) style.

Fig. 12 shows the measurement setup. An Agilent N5181A generates a 30-MHz clock signal. Through a bias-T circuit, it is used as the reference clock of the PLL in the device under test (DUT). The 3.0-Gbps differential clock signals from the DUT are connected to a Tektronix DSA72004B real-time oscilloscope. The DUT is contained in a temperature chamber, which controls the ambient temperature of the DUT.

With the sweep of the ambient temperature, the eye diagram of the differential driver output, which has a clock (1010) pattern, is measured as shown in Fig. 13. The 3.0-Gbps eye diagram at a chamber temperature of 0°C shows 0.747-ps RMS and 5.0-ps peak-to-peak jitter (where the hit count is 10k) as shown in Fig. 13(a). In the eye diagram at 50°C shown in Fig. 13(b), the measured



(a)



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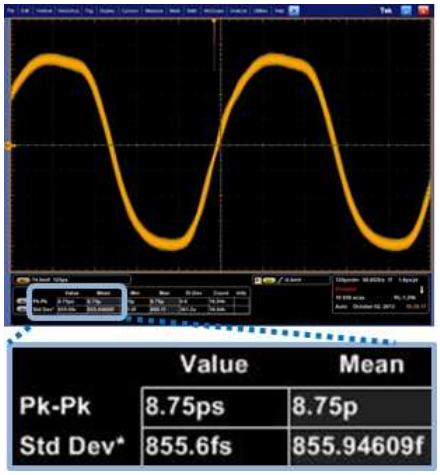

(c)

Fig. 13. Eye diagrams and jitter measurement of the 3.0-Gbps driver output using a clock (1010) pattern at (a) 0°C, (b) 50°C, (c) 100°C.

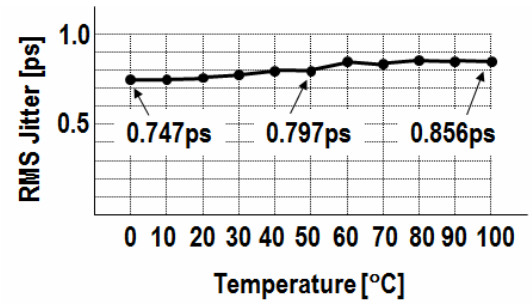

Fig. 14. RMS jitter measurement with the sweep of the chamber temperature.

Table 1. Performance Summary (measurements)

Process	0.11 μm 1P6M CMOS
Circuits	PLL + Driver for test
VCO Frequency (f_{VCO})	0.82 – 2.6 GHz @ 1.2 V (nominally 1.5 GHz)
VCO Gain (K_{VCO})	6.0 GHz/V @ 1.5-GHz f_{VCO}
Measured Jitter (@ 0 – 100°C)	< 0.856-ps RMS < 8.75-ps peak-to-peak
Power Consumption (PLL)	4 mW @ 1.5 GHz, 1.2 V
Active Area (PLL)	288 μm × 270 μm

jitter is 0.797-ps RMS and 6.25-ps peak-to-peak. In the eye diagram at 100°C shown in Fig. 13(c), the measured jitter is 0.856-ps RMS and 8.75-ps peak-to-peak. Fig. 14 shows the RMS jitter measurement with the sweep of the chamber temperature. The RMS jitter barely increases with the temperature. Table 1 summarizes the measured performance of the PLL. The VCO shows the frequency range of 0.82 – 2.6 GHz with a 1.2-V supply voltage.

The PLL operates without a reset signal or an initialization circuit and exhibited no locking problems during the measurements.

V. CONCLUSIONS

In this paper, we propose a charge-pump circuit using a current-bypass technique. This charge-pump circuit not only suppresses the charge sharing but also reduces sub-threshold currents, allowing the PLL jitter to decrease without resorting to a feedback amplifier. The PLL shows no stability issues and no power-up problems, which can occur when a feedback amplifier is used. The PLL in 0.11-μm CMOS technology achieves 0.856-ps RMS and 8.75-ps peak-to-peak jitter, which is almost independent of ambient temperature while consuming 4 mW from a 1.2-V supply.

ACKNOWLEDGMENTS

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