Polar Transmitter with Differential DSM Phase and Digital PWM Envelope

Bo Zhou and Shuli Liu

***Abstract*—A low-power low-cost polar transmitter for EDGE is designed in 0.18μm CMOS. A differential delta-sigma modulator (DSM) tunes a three-terminal voltage-controlled oscillator (VCO) to perform RF phase modulation, where the VCO tuning curve is digitally pre-compensated for high linearity and the carrier frequency is calibrated by a dual-mode low-power frequency-locked loop (FLL). A digital intermediate-frequency (IF) pulse-width modulator (PWM) drives a complementary power-switch followed by an LC filter to achieve envelope modulation with high efficiency. The proposed transmitter with 9mW power dissipation relaxes the time alignment between the phase and envelope modulations, and achieves an error vector magnitude (EVM) of 4% and phase noise of −123dBc/Hz at 400kHz offset frequency.**

***Index Terms*—Polar transmitter, curve compensation, three-terminal voltage-controlled oscillator (VCO), dual-mode frequency-locked loop (FLL), delta-sigma modulator (DSM), pulse-width modulator (PWM)**

I. INTRODUCTION

Wireless communication is becoming more and more important and ubiquitous in modern society. To support numbers of standards in the same handheld devices, there are growing demands for flexible transmitters supporting multimode multiband communications. Polar is a good choice for the goal. Polar transmitters can achieve high power efficiency and good linearity and become growing popular in modern wireless systems [1].

Polar modulation utilizes envelope A and phase Φ components to represent the baseband symbols instead of the conventional I/Q format. A constant-envelope phase-only signal going through a phase-modulation path is multiplied with the signal envelope going through an envelope-modulation path in a switched-mode power amplifier (PA) to reconstruct the original baseband complex signal (I + jQ). The high power efficiency is achieved by using a nonlinear switched-mode PA to handle the constant-envelope phase-modulated RF signal, and the good linear transmission is accomplished by modulating the signal envelope through the supply voltage of the switched-mode PA [2]. Fig. 1 gives the block diagram of polar transmitters.

The existing transmitter [3] with intermediate-frequency (IF) pulse-width modulation (PWM), is prone to low spectrum purity, especially for low carrier-frequency (CF) cases where IF interferences closer to the carrier are difficult to be eliminated only by a band-pass filter (BPF) and without any IF filter. The existing design [4] with all-digital phase-locked loop (PLL) based phase and digital delta-sigma (Δ-Σ) modulator (DSM) based envelope paths, introduces large fractional spurs and

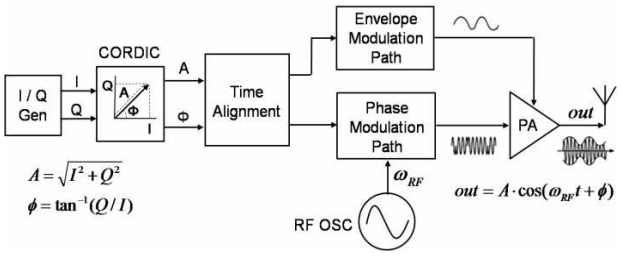


Fig. 1. Block diagram of polar transmitters.

Manuscript received Dec. 3, 2013; accepted Apr. 17, 2014
School of Information and Electronics, Beijing Institute of Technology.
E-mail : zhoubo07@bit.edu.cn

requires strict energy match between power branches. The existing architectures, with digital pre-compensation [5] or two-point modulation [6] based phase and closed-loop analog power switching [7, 8] based envelope paths, degrade time alignment between the phase and envelope paths with complex path transfer functions (TFs). The existing single- or multi-bit DSM based transmitter [9] encounters difficult tradeoff between quantization noise suppression and multi-level power implementation. The existing digital implementation [10] with AM replica feedback linearization requires multiple PAs or the PA array, complicating circuit design. The existing designs with envelope paths based on closed-loop dual-switching [11] or ΔΣ switching [12] methods, either feature complex envelope TF which degrades time alignment, or need a power diode rectifier which is not prone for CMOS on-chip integration.

In this work, with the phase path based on a differential delta-sigma modulated three-terminal voltage-controlled oscillator (VCO) where the carrier frequency is calibrated by a dual-mode frequency-locked loop (FLL) and VCO tuning curve is digitally pre-compensated for high linearity, and with the envelope path employing a digital IF PWM based power switch followed by an LC filter eliminating IF interferences, a polar transmitter for EDGE is proposed, with relaxed time alignment, high linearity and efficiency, low power, noise and complexity.

II. ARCHITECTURE

Fig. 2 shows the proposed polar transmitter with differential DSM phase and digital PWM envelope. 6.5 MHz I/Q components are generated based on a look-up table (LUT) technique [13]. The coordinate rotation digital computer (CORDIC) [14] algorithm accomplishes the conversion from I/Q to polar coordinate A/Φ with the original signal bandwidth of 200 kHz spread to more than 600 kHz [8]. Here, dual path bandwidths are set to 1 MHz for keeping signal spectrum energy. Considering VCO inherently contains a multiplication factor of K_{VCO} (tuning gain) and an integrator of frequency-phase conversion in function [15], both a differentiator with phase-frequency conversion and a divider-by-K_{VCO} are introduced before the phase path. Another divider-by-2 is also included since the VCO is differential architecture.

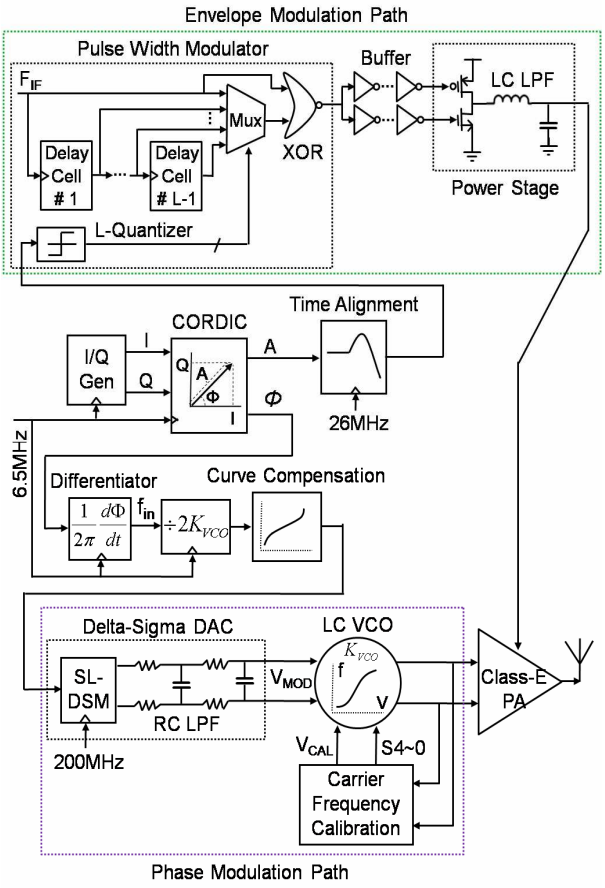


Fig. 2. Proposed polar transmitter.

The full-differential phase path, consisting of a 1-bit quantized single-loop DSM (SL-DSM) with 200 MHz clock, a RC filter with a cut-off frequency of 1 MHz, and a three-terminal pseudo-differential VCO, conveys digital frequency component to RF analog phase one. Considering K_{VCO} of a few MHz/V (such as 5 MHz/V) and baseband frequency component f_{in} of −340-340 kHz [16] for 8PSK, the VCO with differential architecture features high tuning linearity under small input voltage V_{MOD} (such as −70-70 mV). Modulation linearity is further improved by introducing a tuning-curve compensation module, which detects and eliminates the slight tuning distortion from the VCO differential varactor pair. The carrier frequency f_C is digitally calibrated by a dual-mode FLL, while RF phase modulation is performed by the VCO.

The envelope path, including a digital PWM [3] with the quantization level of 256 and IF clock f_{IF} of 3.25 MHz, an inverter-chain based driver buffer with a perfect push-pull dead zone, a complementary power switch

with low on resistor, and a 2nd-order LC filter with a cut-off frequency of 1MHz, performs the mapping from multi-bit digital envelope to the pulse-width of the IF clock, which is then low-pass filtered to generate the analog envelope at the PA supply. The large-sized power switch consisting of complementary power transistors, works in class-D mode with 0.3ns dead zone to provide large-current driver capability for the PA supply.

Under a sampling clock of 200MHz, the signal TF (STF) of the SL-DSM is nearly closer to 1 and the phase-path TF is simplified to that of the RC filter. And the envelope-path TF depends on that of the LC filter, considering linear transmission of the PWM without any delay and ignoring little buffer delay. Hence, it is easy to achieve time alignment between the envelope and phase paths, by introducing an infinite impulse response (IIR) based digital high-pass filter with 26MHz clock to match the TFs between the RC and LC filters.

III. DESIGN IMPLEMENTATION

Detail implementations about *I*/*Q* generation of 8PSK and CORDIC algorithm could be found in [13, 14] and are omitted here. The derivation algorithm, for the phase-frequency conversion under 6.5 MHz clock, employs five-point-interpolation method and is shown in Eq. (1). The baseband frequency component f_{in}, divided by $2K_{VCO}$ and sent to the sequent SL-DSM, has a limited normalized range (such as 0.43~0.57), which is small enough for the SL-DSM input (with a normalized range of 0.25~0.75) not to cause the DSM overflow. The external class-E narrow-band PA with the output power of 10 dBm and efficiency of 70%, employs the conventional architecture with the circuit and parameter analysis clarified clearly in [12, 17], and thus is omitted here. This work focuses on digital PWM envelope and differential DSM phase paths.

$$f_{in,k} = \frac{6.5\times10^6}{24\pi}(\varphi_{k-2} - 8\varphi_{k-1} + 8\varphi_{k+1} - \varphi_{k+2}) \quad (1)$$

1. Phase Path Implementation

Fig. 3 shows the block diagram of the proposed 2nd-order 1-bit quantized SL-DSM with a normalized input range of 0.25~0.75. 200MHz sampling clock is chosen

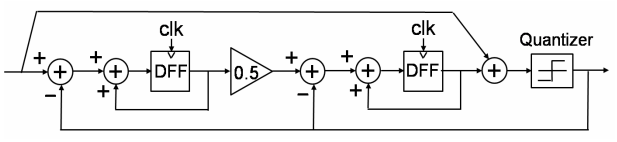


Fig. 3. Block diagram of proposed SL-DSM.

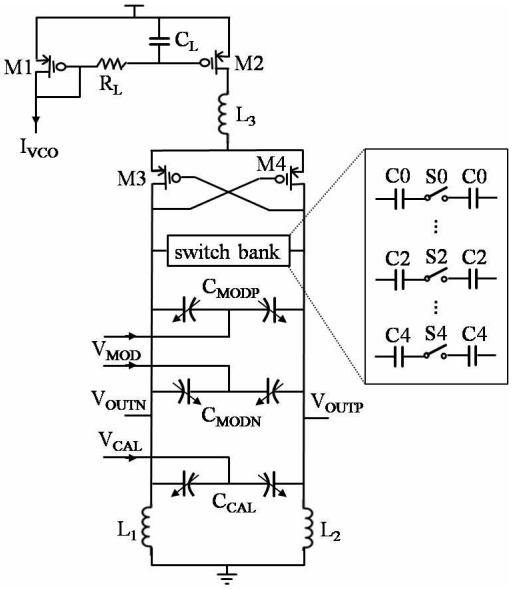


Fig. 4. Proposed three-terminal pseudo-differential VCO.

with high over-sampling ratio (OSR) for enough quantization noise suppression. 2nd-order butterworth attenuation is introduced to the denominator of the noise TF (NTF), and contributes to reducing out-of-band quantization noise. The SL-DSM STF is shown in Eq. (2). Considering the input signal frequency *f* less than 1MHz is far smaller than the sampling frequency f_s of 200MHz, the STF is nearly closer to 1, which simplifies the phase-path TF as mentioned above.

$$STF = \frac{1-2z^{-1}+1.5z^{-2}}{1-z^{-1}+0.5z^{-2}} \approx 1-4\pi\frac{f}{f_s} \quad (2)$$

Fig. 4 gives the proposed three-terminal VCO which employs the conventional cross-coupled three-transistor architecture with LC tank. An inductor L_3 inserted between the current source M2 and the cross-couple pair M3-M4 reduces the second-order harmonic noise. A resistor R_L and a capacitor C_L make a low-passed filter (LPF) to suppress the bias noise. The differential-pair (C_{MODP}, C_{MODN}) and single-ended (C_{CAL}) varactors and switched-capacitor array (C4~0), together with the

inductor pair (L_1, L_2), form a resonator cavity. The VCO has two parallel working paths: the differential input V_{MOD} with a pseudo-differential pair of NMOS accumulation-mode varactors, used for phase modulation path where VCO instantaneous output frequency responds quickly, and avoiding the tuning nonlinearity caused by single varactor; the other single-ended varactor fine-tuning input V_{CAL}, together with 5-bit coarse-tuning word *S4~0* controlling a binary-weighted MIM capacitor array, designed for f_C calibration path without affecting VCO phase modulation path, since it is the average or center rather than instantaneous output frequency that is adjusted slowly.

Define the VCO tuning gain for phase modulation controlled by V_{MOD} as modulation gain K_{VCO}, and the VCO tuning gain for f_C calibration adjusted by V_{CAL} as calibration gain $K_{VCO,CAL}$, respectively. Obviously, low $K_{VCO,CAL}$ and K_{VCO} contribute to low phase noise, and coarse-tuning control word *S4~0* helps to widen f_C calibration range without degrading the phase noise.

Although differential varactor pair contributes to optimizing the tuning linearity of the VCO modulation path especially under small V_{MOD} range, in fact, slight nonlinearity still exists in the tuning curve. A digital pre-compensation module depicted in Fig. 5 is employed to offset the slight tuning-curve distortion. The digital module has two work modes: the VCO modulation path firstly open-loop working intermittently in mode "1" where the differential tuning curve is measured and linear gain error is detected and digitally stored in a read-only memory (ROM); then the VCO modulation path working continuously in mode "2" under which the stored gain error is multiplied to the phase-modulation path and compensates for the sequent tuning-curve distortion. For the given VCO, the tuning curve is fixed and only needs to be measured again when the VCO working environment (such as temperature and f_C) changes. With low power and parallel f_C calibration, the environment parameters change slowly, hence, it is enough for the VCO modulation path to work in mode "1" once every ten seconds.

To ensure f_C stable, the VCO needs to work in a closed-loop system. Fig. 6 shows a dual-mode closed-loop frequency negative-feedback system, called by FLL, consisting of a high-frequency current-mode-logic (CML) divider, a frequency detector (FD) configured by the

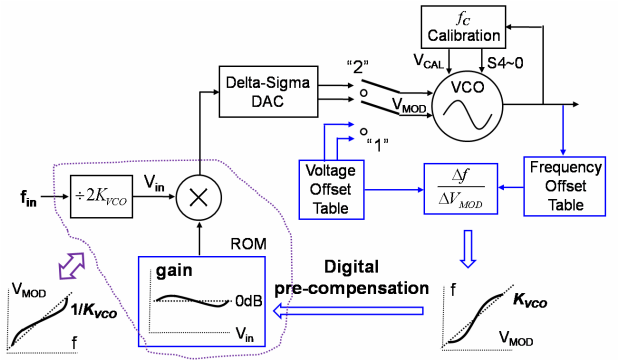


Fig. 5. Proposed digital compensation for VCO tuning curve.

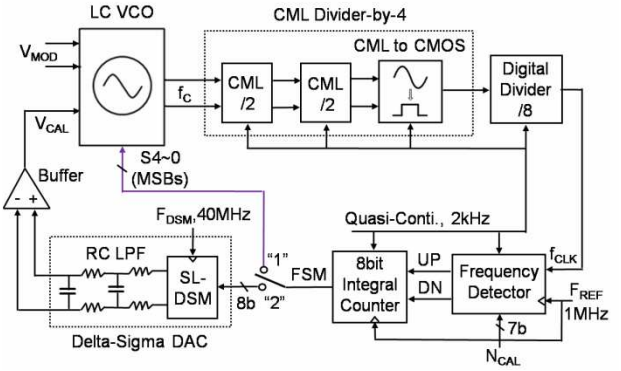


Fig. 6. Proposed dual-mode low-power f_C calibration loop.

control word N_{CAL}, a bidirectional integral counter and a full-differential 8-bit Δ-Σ digital-analog converter (DAC) with an isolation buffer which avoids kickback noise from the LC VCO. The carrier frequency divided by 32 (4×8) is compared to a certain reference frequency of $N_{CAL}\times F_{REF}$ in the FD whose results cause the sequent 8-bit integral counter self-addition or -subtraction by 1, which inversely modifies the control voltage V_{CAL} and digital control words *S4~0*, and thus calibrates f_C deviation. While RF phase modulation is performed by the VCO modulation path, any slow f_C deviation can be corrected simultaneously by the embedded VCO calibration path.

The proposed FLL has two work modes: 5-bit high-speed coarse-tuning mode "1" working on power-on state where large f_C deviation exists, used to reduce the VCO calibration gain with phase noise optimization and ensure wide f_C calibration range; Δ-Σ low-speed fine-tuning mode "2" operating on normal state and compensating for small f_C deviation, to ensure the calibration resolution and achieve low loop noise with low-passed filtering on the CML divider.

The 8-bit Δ-Σ DAC with 40-MHz sampling clock is designed with a low cut-off frequency of 100Hz and thus time constant of 1.6ms, which ensures the low-power operation of the high-speed CML frequency divider dominating the FLL power dissipation. Under 10% duty cycle, during each control clock period of 0.5 ms (control frequency of 2 kHz), the CML divider with the tail current source on/off steered by the control clock is active for 0.05 ms and disabled for 0.45 ms while the output of the integral counter is kept and the loop with 1.6 ms time constant holds V_{CAL} and *S4~0* and thus f_C until the next clock cycle arrives. That is, f_C is only calibrated in 10% time slot and kept in the rest during each control clock period. With low power dissipation of only 0.4 mW and the reference clock F_{REF} of 1 MHz, The FLL ensures f_C stability at the digitally configurable value of N_{CAL}×32 MHz.

Different from existing calibration methods, the narrowband DAC is able to hold the VCO calibration voltage until the next calibration clock cycle arrives, which supports low-power quasi-continuous operation. In addition, dual-mode architecture contributes to good tradeoff between wide f_C calibration range and high calibration resolution.

2. Envelope Path Implementation

Fig. 2 shows the proposed envelope path, employing a digital IF PWM based open-loop power switch followed by an LC filter. The principle and design of digital IF PWM, based on delay multiplexer with inverter based delay line and unit-delay auto-calibration, has been clearly clarified in [3]. By employing an *L*-level quantizer and an *L*-stage delay line with an unit delay of $1/(2L\times f_{IF})$, the multi-bit baseband envelope components are equidistantly quantized to *L* discrete values and mapped to *L* discrete rising-edge lags, and correspond to *L* discrete pulse-widths of the IF clock, which are low-pass filtered to reconstruct the analog envelope components at the PA supply with large-current driver capability provided by the class-D power switch. The envelope-modulation linearity strongly depends on the quantization level *L*. Here, *L*=256 is chosen to trade off the modulation linearity and design complexity.

With an envelope range of 0.22-1.44 V [16] for 8PSK, for the power supply of 1.8 V, the normalized envelope range of 0.12-0.80 is achieved. That means the minimum and average conduction time of the power switch are $0.06/f_{IF}$ and $0.23/f_{IF}$, which inversely set the maximum and average switching frequencies $f_{IF}/0.12$ and $f_{IF}/0.46$ for the power switch, respectively.

Lower switching frequency contributes to larger power transistor size, which inversely causes smaller on resistor and thus higher power efficiency. To ensure high efficiency of the envelope path which dominates the transmitter efficiency, lower f_{IF} is better. But on the other side, higher f_{IF} contributes to IF aliasing suppression by the LC filter with 1-MHz cut-off frequency. Here, f_{IF} =3.25 MHz is chosen with a tradeoff between IF suppression and transmitter efficiency. The unit delay of 0.6 ns, the maximum and average switching frequencies of 27 MHz and 7 MHz, are fixed, respectively.

The time alignment between the envelope and phase paths is achieved by introducing a 2^{nd}-order IIR digital compensation filter with 26 MHz clock in the envelope path to match the TFs between the RC and LC filters, as discussed above. That is, the zeros of the IIR filter match the poles of the LC filter, and the poles of the IIR filter match the poles of the RC filter. Considering the poles of both RC and LC filters always vary with process, voltage and temperature (PVT) deviations but the digital IIR filter has a fixed TF independent of PVT, it is difficult to ensure strict TF match between the RC and LC filters only by employing a parameter-fixed IIR high-passed filter.

In order to ensure high robustness of time alignment over PVT, on one hand, digitally reconfigurable binary-weighted switched-capacitor array is employed to the RC filter for keeping the product of the resistor and capacitor constant, which stabilizes the poles of the RC filter and thus matches the fixed poles of the IIR filter; on the other hand, the IIR filter with reconfigurable numerator and constant denominator in the TF, which has adjusted zeros and fixed poles, is considered to match the variable poles of the LC filter without affecting the stabilization of the IIR filter. Of course, with the external rather than on-chip RC and LC filters, the IIR digital filter will be simplified without considering the robustness over PVT.

3. Performance Estimation on Proposed Architecture

With full-differential VCO architecture and tuning-

curve compensation module, high modulation linearity is achieved. Under low switching frequency with an average value of 7 MHz, high transmitter efficiency is ensured. Since the noise of the CML divider is low-pass filtered by the narrowband FLL with 100-Hz bandwidth and the quantization noise of the SL-DSM is little with an OSR higher than 100, the transmitter noise is dominated by the VCO, which aims for low phase noise with low modulation and calibration gains. Except for the LC VCO, CML divider and external PA, other transmitter modules are either digital or passive, and only the LC VCO and external PA dominate the power dissipation. In addition, simplified time alignment is employed. All these contribute to low cost and low power.

Therefore, the proposed transmitter contributes to high efficiency and linearity, low power, low noise and low complexity.

IV. Experimental Results

The proposed polar transmitter is designed in 0.18 μm CMOS with 9 mW power dissipation from a 1.8V supply and achieves the power efficiency of 70%, excluding the external class-E PA. Fig. 7 shows differential modulation- and single-ended calibration-curves of the proposed VCO. Both a differential modulation gain of 5 MHz/V with slight distortion less than 3% under the control voltage range of −70-70 mV, and an average single-ended calibration gain of 14 MHz/V with the carrier frequency range of ±10% from the oscillating frequency of 1.8 GHz, are observed. The phase noise depicted in Fig. 8 is −123 dBc/Hz at 400 kHz offset frequency from 1.8 GHz, meeting EDGE requirement (−107 dBc/Hz @ 400 kHz offset).

Fig. 9 gives f_C calibration performances of FLL with continuous and quasi-continuous operations, by watching the loop locking procedure, which is inversely estimated by observing V_{CAL} curves. With duty-cycle control, the FLL or CML divider only works at 10% time slot, that is, f_C is only calibrated in first 10% period and kept in the rest during each control clock period. The voltage V_{CAL} of the duty-cycled case goes through ten times as locking time and reaches to the same locking value as that of the continuous one, indicating the quasi-continuous mode does not affect loop locking and thus f_C calibration with only one-tenth power dissipation.

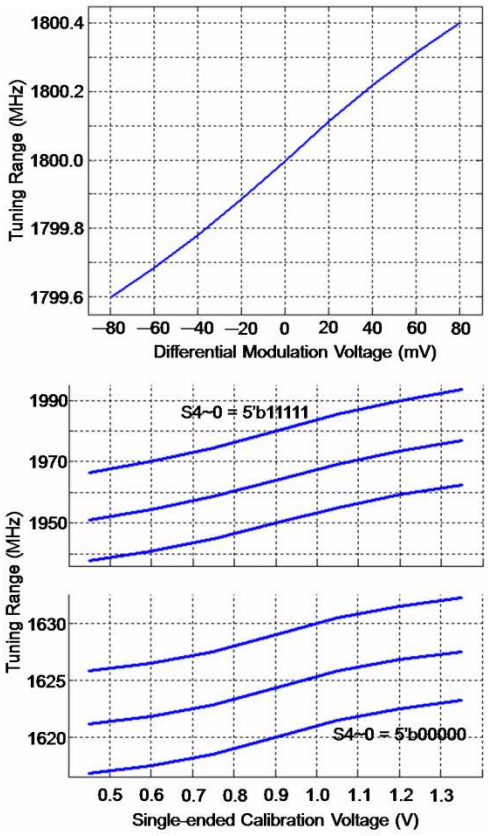


Fig. 7. Modulation and calibration curves of proposed VCO.

Fig. 8. Phase noise of proposed VCO.

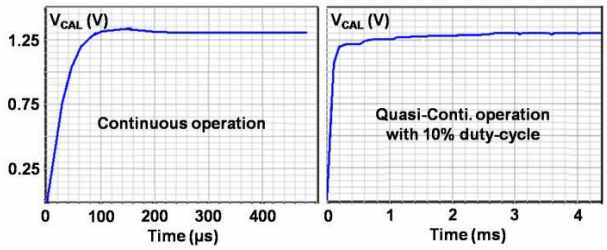


Fig. 9. f_C calibration performances of proposed FLL.

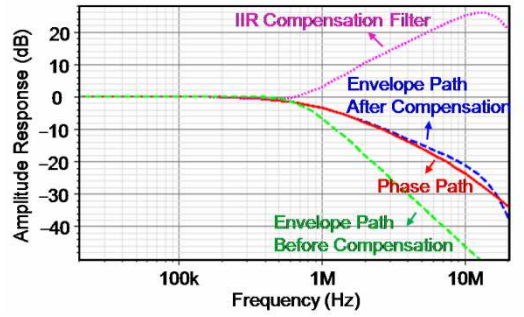


Fig. 10. Path frequency responses w/i & w/o time alignment.

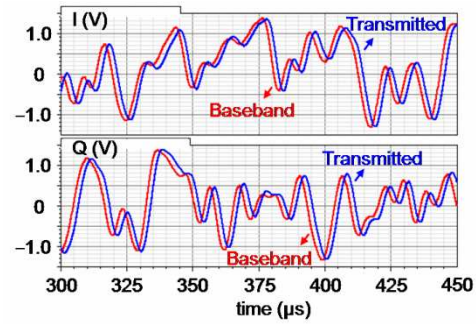


Fig. 11. I/Q components of 8PSK: transmitted vs. baseband.

Fig. 10 shows frequency responses of the envelope and phase paths with and without time alignment. Without TF compensation, the envelope path is not synchronous to the phase one. With a digital 2nd-order IIR compensation filter, the time alignment is achieved by matching the path TFs within the desired frequency range up to 1 MHz.

Fig. 11 shows *I*/*Q* components through the proposed transmitter with comparison to the baseband ones for 8PSK. Little envelope offsets result from the limited quantization resolution of the digital PWM and the slight push-pull unsymmetry of the power switch, and slight phase ripples are caused by the SL-DSM quantization noise and VCO phase noise. The root-mean-square (rms) error vector magnitude (EVM) is about 4%, meeting the system requirement of 9% for EDGE.

Fig. 12 gives transmitter output constellation for 8PSK. Little deviation of the symbol vectors from the eight homocentric points is observed in the constellation, resulting from limited PWM resolution, switch unsymmetry, DSM and VCO noise, which are mentioned above.

Fig. 13 shows simulated transmitter output spectrum. The power spectral density at the 400 kHz offset is shown to be −59 dB, which meets the mask requirement (−54 dB @ 400 kHz offset) for EDGE.

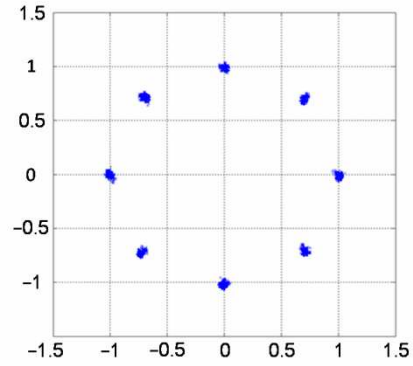


Fig. 12. Transmitter output constellation for 8PSK.

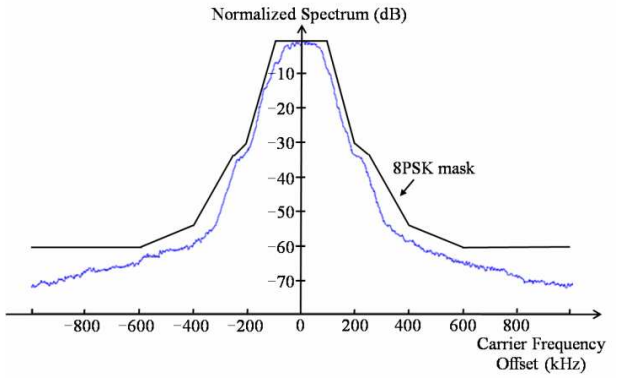


Fig. 13. Transmitter output spectrum for 8PSK.

Table 1. Transmitter performance summary and comparison

References	f_C (GHz)	Noise (dBc/Hz)	Efficiency (%)	RMS EVM (%)	Spectrum (dB)
This Work	1.62-1.98	−123 @ 400kHz	70(50)*	4	−59 @ 400kHz
[1]	0.8-2.4	-	52	6	−60 @ 400kHz
[2]	1.7-1.8	-	-	3	−64 @ 400kHz
[3]	0.95-2.4	-	-	1.9-6.1	−40
[4]	1.68	−114 @ 400kHz	8.3	3.2-7.0	−45
[6]	0.9-2.4	−119 @ 400kHz	-	2.4	−61 @ 400kHz
[10]	1.5-2.7	-	32	2.8-4.1	-

* The transmitter efficiency is 70% and 50% with the ideal and real PAs, respectively

The performance of the proposed transmitter is summarized and compared to the existing designs in Table 1. The presented architecture features good linearity, high efficiency and low noise.

V. Conclusions

With differential Δ-Σ VCO based phase and digital PWM power switch based envelope paths, a low-power low-cost polar transmitter with tuning-curve pre-compensated and carrier-frequency calibrated is implemented in 0.18 μm CMOS for EDGE. The

proposed architecture transmits baseband components well and meets system requirements, with relaxed time alignment, good linearity, high efficiency and low noise.

ACKNOWLEDGMENTS

This work is supported by the National Natural Science Foundation of China (No. 61306037) and Basic Research Foundation of Beijing Institute of Technology (No. 20130542009).

REFERENCES

[1] J. Lopez, et al, "Design of highly efficient wideband RF polar transmitters using the envelope-tracking technique," *Solid-State Circuits*, *IEEE Journal of*, Vol.44, No.9, pp.2276-2294, Sept., 2009.

[2] J. Mehta, et al, "An efficient linearization scheme for a digital polar EDGE transmitter," *Circuits and Systems II, IEEE Transactions on*, Vol.57, No.3, pp.193-197, Mar., 2010.

[3] P. Nuyts, et al,"A fully digital delay line based GHz range multimode transmitter front-end in 65-nm CMOS," *Solid-State Circuits*, *IEEE Journal of*, Vol.47, No.7, pp.1681-1692, July, 2012.

[4] J. Chen, et al, "The design of all-digital polar transmitter based on ADPLL and phase synchronized ΔΣ modulator," *Solid-State Circuits*, *IEEE Journal of*, Vol.47, No.5, pp.1154-1164, May, 2012.

[5] M.H. Perrott, et al, "A 27-mW CMOS fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation," *Solid-State Circuits*, *IEEE Journal of*, Vol.32, No.12, pp.2048-2060, Dec., 1997.

[6] M. Youssef, A. Zolfaghari, et al, "A low-power GSM/EDGE/WCDMA polar transmitter in 65-nm CMOS," *Solid-State Circuits*, *IEEE Journal of*, Vol.46, No.12, pp.3061-3074, Dec., 2011.

[7] P.Y. Wu, and P.K.T. Mok, "A two-phase switching hybrid supply modulator for RF power amplifiers with 9% efficiency improvement," *Solid-State Circuits*, *IEEE Journal of*, Vol.45, No.12, pp.2543-2556, Dec., 2010.

[8] P.J. Nagle, et al, "A wideband linear amplitude modulator for polar transmitters based on the concept of interleaving delta modulation," *Solid-State Circuits Conference, 2002. ISSCC 2002. Digest of Technical Papers. IEEE International*, 7-7, pp. 234-235, Feb., 2002.

[9] W.-Y. Kim, "1-bit and multi-bit envelope delta-sigma modulators for CDMA polar transmitters," *Microwave Conference, 2008, APMC 2008, Asia-Pacific*, 16-20, pp.1-4, Dec., 2008.

[10] S. Zheng, and H.C. Luong, "A CMOS WCDMA/WLAN digital polar transmitter with AM replica feedback linearization," *Solid-State Circuits*, *IEEE Journal of*, Vol.48, No.7, pp.1701-1709, July, 2013.

[11] M. Hassan, P.M. Asbeck, and L.E. Larson, "A CMOS dual-switching power-supply modulator with 8% efficiency improvement for 20MHz LTE envelope tracking RF power amplifiers," *Solid-State Circuits Conference, 2013. ISSCC 2013. Digest of Technical Papers. IEEE International*, 17-21, pp. 366-367, Feb., 2013.

[12] F. You, B. Zhang, et al, "Analysis of a broadband high-efficiency switch-mode ΔΣ supply modulator based on a class-E amplifier and a class-E rectifier," *Microwave Theory and Techniques, IEEE Transactions on*, Vol.61, No.8, pp.2934-2948, Aug., 2013.

[13] K.M. Nitin Babu, and K.K. Vinaymurthi, "GSM-EDGE modulators for 2.5G system, an efficient parallel implementation on FPGA," *Signal Processing, Communications and Computing, 2011, ICSPCC 2011, IEEE International Conference on*, 14-16, pp.1-5, Sept., 2011.

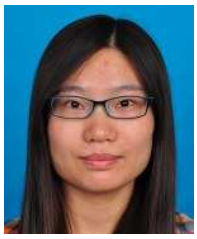
[14] A. Chen, and S. Yang, "Reduced complexity CORDIC demodulator implementation for D-AMPS and digital IF-sampled receiver," *Global Telecommunications Conference, GLOBECOM 1998*, 8-12, pp.1491-1496, Nov., 1998.

[15] M.H. Perrott, M.D. Trott, and C.G. Sodini, "A modeling approach for Σ-Δ fractional-N frequency synthesizer allowing straightforward noise analysis," *Solid-State Circuits*, *IEEE Journal of*, Vol.37, No.8, pp.1028-1038, Aug., 2002.

[16] C. Mayer, et al, "A robust GSM/EDGE transmitter using polar modulation techniques," *Wireless Technology, 2005, ECWT 2005, The European Conference on*, 3-4, pp.93-96, Oct., 2005.

[17] M. Albulet, *RF power amplifiers*, Atlanta, USA: Nobel Publishing Corporation, 2011.

Bo Zhou received the B.S. degree from Hunan University, Changsha, China, in 2002, and the M.S. degree in Shanghai Jiaotong University, Shanghai, China, in 2005, and the Ph.D. degree in Tsinghua University, Beijing, China, in 2012, respectively. In 2005, he joined STMicroelectronics Co. Ltd., Shanghai, China, and worked on car-body electronic power design. In 2007, he joined Agere System Co. Ltd., Shanghai, China, and worked on magnetic head read-write channel design. In 2012, he joined the faculty of the School of Information and Electronics at Beijing Institute of Technology. His research interests cover delta-sigma PLLs, fully-digital transmitter, polar transmitter and frequency-modulated ultra-wideband transceivers.



Shuli Liu received the B.S. degree in Electronic Information Science and Technology from China Agricultural University, Beijing, China, in 2013. She is currently working toward the M.S. degree at the School of Information and Electronics, Beijing Institute of Technology, Beijing, China. Her current research interests are analog and RF integrated circuits.