Epilayer Optimization of NPN SiGe HBT with n+ Buried Layer Compatible With Fully Depleted SOI CMOS Technology

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Abstract— **In this paper, the epi layer of npn SOI HBT with n+ buried layer has been studied through Sentaurus process and device simulator. The doping value of the deposited epi layer has been varied for the npn HBT to achieve improved f_tBV_{CEO} product (397 GHzV). As the BV_{CEO} value is higher for low value of epi layer doping, higher supply voltage can be used to increase the f_t value of the HBT. At 1.8 V V_{CE}, the f_tBV_{CEO} product of HBT is 465.5 GHzV. Further, the film thickness of the epi layer of the SOI HBT has been scaled for better performance (426.8 GHzV f_tBV_{CEO} product at 1.2 V V_{CE}). The addition of this HBT module to fully depleted SOI CMOS technology would provide better solution for realizing wireless circuits and systems for 60 GHz short range communication and 77 GHz automotive radar applications. This SOI HBT together with SOI CMOS has potential for future high performance SOI BiCMOS technology.**

Index Terms— **Fully depleted, sentaurus, SiGe HBT, SOI**

I. INTRODUCTION

The SiGe heterojunction bipolar transistors have been popular choice for high speed analog and RF circuit applications [1]. The working principle of HBTs and the review work are given in detail in [1-5]. Several works have been reported on BiCMOS technology on bulk substrate that can be found from the literature [6-8]. Although BiCMOS technology on bulk substrate offers devices with promising performance, the process complexity, isolation among devices and power consumption have been the main issues in deep submicron lithography nodes. The emergence of SOI as an excellent platform for short channel MOSFETs has motivated researchers to design and optimize HBTs on thin film SOI. The detailed discussion on integration of SiGe HBT with CMOS on SOI can be found in [9, 10]. The advantages of this integration on SOI platform are also discussed in [11, 12].

A novel vertical bipolar transistor compatible with SOI CMOS was demonstrated in [13]. Recently, researchers have been trying to integrate the HBT with SOI CMOS to offer SOI BiCMOS technology [14-17]. The SOI CMOS technology has been of interest in the industry due to its scalability and reduced short channel effects. The HBTs that are compatible with the fully depleted SOI CMOS technology have poor performance in terms of speed due to the high value of collector resistance. Therefore, it is of interest to improve the performance of the SOI HBT. Recently, simulation study of SOI HBT with buried layer has been performed [18] and a high performance SOI HBT compatible with 130 nm SOI CMOS technology is proposed. Though SiGe HBT with buried silicide layer has been discussed in [19], the HBT is not compatible with advanced fully depleted SOI CMOS technology. A fully self aligned Si/SiGeC HBT with boron in-situ doped polybase, phosphorus doped emitter and nickel silicide has been reported in [20].

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Using different device design approach researchers have explored performance improvement in HBT [18-21].

In this paper, 2D numerical simulation studies have been performed on SOI HBT compatible with fully depleted SOI CMOS which is in a way an extension of our previous work [18]. The SOI HBT is optimized for 65 nm technology node. The epilayer is optimized to achieve higher f_tBV_{CEO} product. The fabrication procedure and the operating principle of the HBT are discussed in section II. The dc and ac characteristics of SOI HBT have been discussed by varying the doping value of the epi layer. The optimal doping value obtained from the simulations is reported in section III. Section IV describes the scaling of epi layer thickness to obtain better performance. Finally the conclusion is given in section V.

II. NPN SOI HBT WITH BURIED LAYER

The proposed SOI HBT with n+ buried layer of 0.15 μm^2 area is shown in Fig. 1. The fabrication of the device is given as follows. An SOI substrate is taken with 20 nm film thickness. By applying the rule of ETSOI ($T_{si} = L_G/3$) [22], this substrate is fully depleted and is optimal for SOI CMOS technology with 65 nm node. The SOI film is doped with $1x10^{20}$ cm^{-3} in the area where the HBT is to be fabricated. To achieve this doping value, a dose of $8x10^{14}$ cm^{-2} is used at 30 KeV. A 100 nm n-type epi layer is deposited on the n+ buried layer. The rest of the fabrication procedure can be followed from [23] to fabricate the proposed npn SOI HBT. In the process simulations, phosphorus has been used for the n-type collector and the polysilicon emitter. The experimental HBTs use arsenic doped emitter [23, 24]. Boron is used in the base. After the epitaxial growth of SiGe base layer, 12 nm of silicon cap layer has been used for the emitter diffusion. The process steps reported for the experimental device [23] has been applied in Sentaurus process simulator [25]. From the process simulations the doping values and germanium concentration of the HBT are obtained. The doping profiles are plotted with two different epi layer doping as shown in Fig. 2. The device parameters obtained from the process simulations are tabulated in Table 1. The SOI HBT simulation results have been validated with the high speed experimental device [23] and the simulation results agree closely with the experimental findings. The experimental HBT uses SiGeC in the base layer. In our simulations, SiGe base layer has been used. The beta value of the experimental

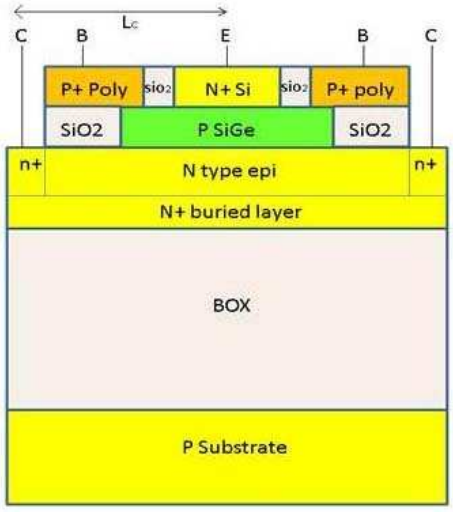

Fig. 1. Schematic of npn SOI HBT with n+ buried layer.

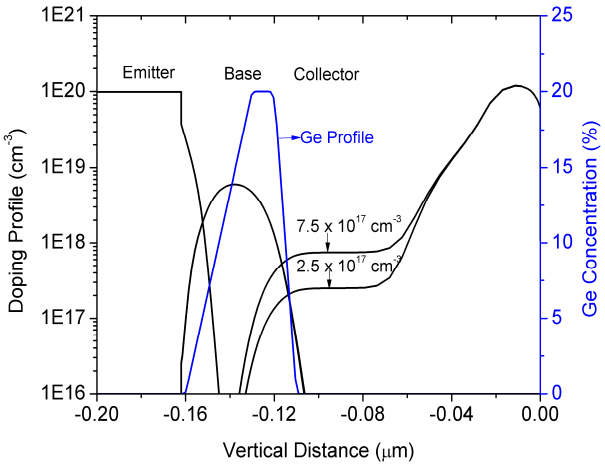

Fig. 2. Doping Profile and Ge profile of npn SOI HBT (epilayer thickness = 100 nm and buried layer thickness = 20 nm).

Table 1. SiGe HBT parameters

Parameter	Values	units
Emitter thickness	100	nm
Emitter Width	150	nm
Base thickness	30	nm
Buried layer	20	nm
Deposited epi layer	100	nm
BOX thickness	100	nm
Emitter doping	$1x\ 10^{20}$	cm^{-3}
Base doping	$1x\ 10^{19}$	cm^{-3}
Epi layer doping	$7.5x\ 10^{17}$	cm^{-3}
Buried layer doping	$1x\ 10^{20}$	cm^{-3}
Substrate doping	$1x\ 10^{15}$	cm^{-3}

device is nearly 1000. For our simulated device, the beta value is nearly 850. The peak f_t and BV_{CEO} values of the experimental device are 102 GHz and 1.8 V respectively. The peak f_t and BV_{CEO} values of the simulated HBT are 113 GHz and 1.78 V respectively. For this work, the collector profile has been engineered with a n+ buried layer and a deposited epi layer. For obtaining better f_t value a modified trapezoid Ge profile (0 % - 20 %) has been used. The slow grading of this profile minimizes the base-emitter capacitance compared to the device with steeper Ge grading profile. The 2D numerical simulations have been performed in the Sentaurus device simulator [26] to obtain the current density of npn SOI HBT. The models and the model parameters that have been used in the simulation are discussed in [18] and are as follows. The hydrodynamic model has been used in the simulation. The Slotboom bandgap narrowing model [27] is used to estimate the carrier density. Philips unified mobility model [28] has been chosen. In the recombination, Shockley-Read-Hall and Auger recombination model is used. The Okuto-Crowell model [29] is used to incorporate the impact ionization.

III. Optimization of Epi Layer Doping in SOI HBT

In the npn SOI HBT simulation study, a 1.2 V of V_{CE} is used and V_{BE} is varied from 0 V to 1.2 V. From Table 1, the epi layer doping value is varied and the other parameters are kept constant. This parameter is chosen to change the base collector space charge region inside the device. In the simulation the biasing scheme is forced-V_{BE}. From the simulations, the base and collector currents have been obtained. The beta values are extracted as shown in Fig. 3. The small signal ac analysis has been performed to obtain the Y parameters. From the Y parameters the ac voltage gain (Y_{21}/Y_{22}) is evaluated. The results are reported in Fig. 4. At low value of epi layer doping, the collector base space charge region is entirely towards collector side. Also the SOI HBT with low value of epi layer doping, the effective base layer thickness increases (in Fig. 2) which is the cause of improved output impedance. At low and moderate injection, the ac voltage gain increases by decreasing the epi layer doping. This is due to dominant contribution of R_C in the $r_0 \parallel R_C$ value. At low and moderate injection,

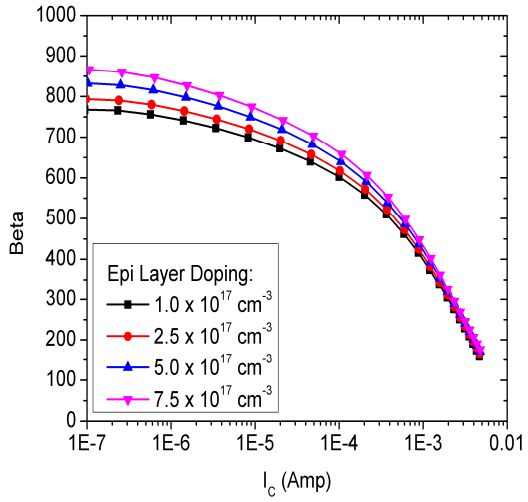

Fig. 3. Beta of npn SOI HBT with different epi layer doping.

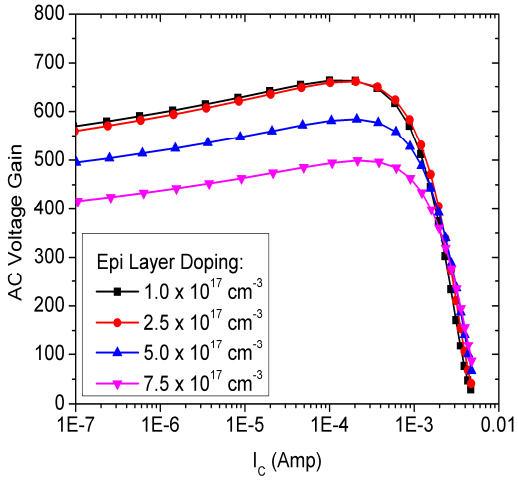

Fig. 4. AC Voltage gain of npn SOI HBT with different epi layer doping.

the r_0 value is much higher than the R_C. However, at high injection, the r_0 value is a dominant factor in the ac voltage gain. Therefore, at (I_C > 1 mA), the HBT with high value of epi layer doping has high ac voltage gain.

Fig. 5 shows the unity current gain frequency of HBT. The HBT with high epi layer doping offers better f_t value. This is due to delayed saturation of collector current. The base-collector space charge region expands towards collector side vertically because the depletion width towards collector side is approximately 60 nm for the HBT with 7.5×10^{17} cm^{-3}. In the calculation 1.2 V of reverse bias was used. The actual deposited epi layer thickness is 100 nm. But due to the diffusion buried layer, the effective epi layer thickness has become nearly 70 nm. When epi layer doping value decreases, the space charge region expands

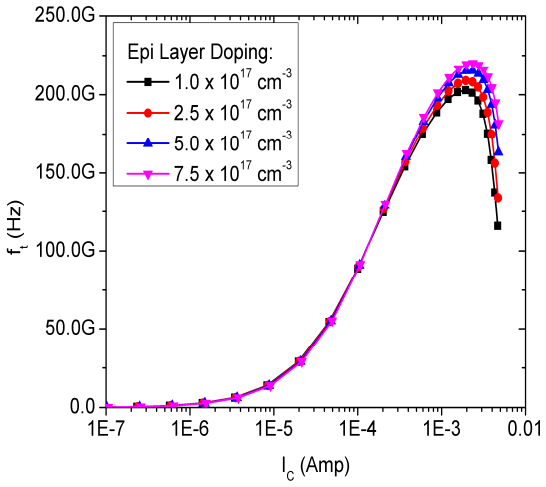

Fig. 5. f_t of npn SOI HBT with different epi layer doping.

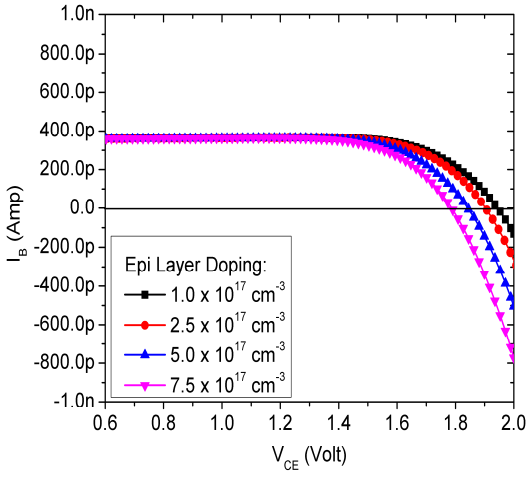

Fig. 6. BV_{CEO} of npn SOI HBT with different epi layer doping.

Table 2. Performance comparison of SOI HBT with different epi layer doping values

Epi Layer Doping (cm^{-3})	Peak f_t (GHz)	BV_{CEO} (Volt)	f_tBV_{CEO} Product (GHzV)
1.0 x 10^{17}	202.9	1.94	393.6
2.5 x 10^{17}	208.9	1.90	397.0
5.0 x 10^{17}	215.3	1.84	396.1
7.5 x 10^{17}	220.1	1.78	391.7

laterally towards collector contacts.

The base current reversal effect in bipolar transistor is discussed in [30]. In the simulation, the breakdown voltage is obtained from the base current reversal point for V_{BE} = 0.7 V. The results are reported in Fig. 6. From Table 2, it has been observed that the f_t value decreases and the BV_{CEO} value increases by decreasing the epi layer doping. The increase in BV_{CEO} value is due to the lateral expansion of space charge region. The trade off suggests that there is an optimal doping value that would be necessary to maximize the f_tBV_{CEO} product. As shown in [31, 32], there is a tradeoff between f_t and BV_{CEO} in the bipolar transistor design. In our simulation we analyzed the tradeoff and the f_tBV_{CEO} product. The f_tBV_{CEO} product has been obtained for different doping levels of the epi layer. From the results reported in Table 2, it has been observed that the SOI HBT with 2.5x10^{17} cm^{-3} epi layer doping has highest f_tBV_{CEO} product (397 GHzV). The f_tBV_{CEO} tradeoff suggests that the device performance can be improved in two ways. In the first approach, the supply voltage could be increased to achieve the high f_t value and in the second approach, the film thickness could be scaled to achieve similar improvement.

In both approaches, the Kirk current of the SOI HBT is improved. The details are discussed in the subsequent section. In both ways, power consumption of the HBT would increase as discussed below. The f_t value has been obtained by raising the supply voltage as shown in Fig. 7. At high supply voltage (V_{CE}=1.8 V), the collector base reverse bias of the HBT increases. With increased reverse bias, the depletion width of collector-base diode is increasing to compensate the reduced amount of charges. Therefore, the reverse biased collector-base capacitance value decreases by applying high supply voltage. At peak f_t (V_{BE} = 1.032 V), the (C_{BE}+C_{BC}) of the SOI HBT is 12.23 fF for 1.2 V of V_{CE}. Due to the aforementioned reason, this capacitance value decreases to 11.1 fF by applying 1.8 V of V_{CE}. Additionally, the peak f_t value of the SOI HBT (V_{CE} =1.8 V) is obtained at high collector current compared to the HBT with 1.2 V of V_{CE}. This is because the increase in the trans-conductance value is significant compared to the increase in the capacitance value at V_{BE} = 1.032 V (corresponding to peak f_t) and hence the peak f_t value is obtained at the collector current of 3.58 mA. This delays the onset of the Kirk effect of the transistor. As can be seen from the Fig. 7, a maximum of 245 GHz of f_t value can be obtained by using 1.8 V of V_{CE} with an epi layer doping of 2.5 x 10^{17} cm^{-3}. The Kirk current of the HBT [33] can be written as given in Eq. (1).

$$\text{IC, Kirk} = qA_E v_{sat} N_C \left(1 + \frac{2\mathcal{E}(V_{CB} + \emptyset_{bi})}{qN_C W_C^2}\right) \quad (1)$$

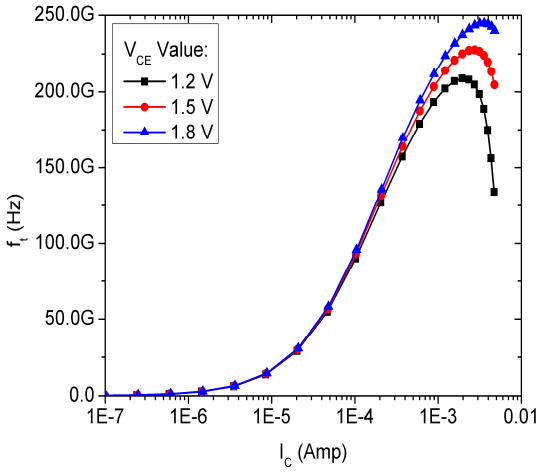

Fig. 7. f_t of npn SOI HBT with epi layer doping of $2.5x10^{17}$ cm^{-3}.

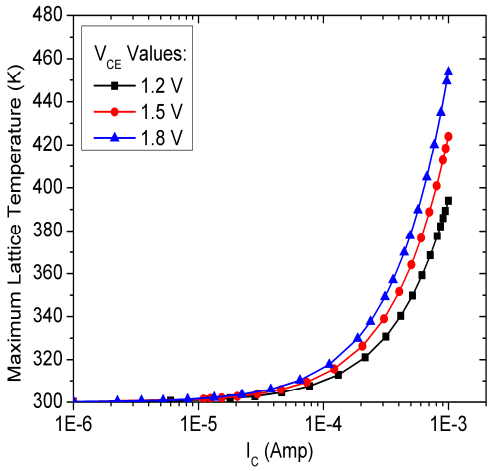

Fig. 8. Maximum lattice temperature of HBT with different V_{CE}.

where N_C is the the doping value of the deposited epi layer and W_C is the thickness of the layer. V_{CB} is the applied reverse bias voltage to the collector-base diode. The onset of Kirk current can be increased by increasing the epi layer doping, supply voltage and reducing the thickness of the epi layer. By increasing the Kirk current value, the charging time component of the transistor can be reduced. For the epi layer doping of 2.5 x 10^{17} cm^{-3}, the BV_{CEO} of the SOI HBT is 1.9 V. This results in 465.5 GHzV of f_tBV_{CEO} product. The improved performance of the SOI HBT with n+ buried layer is obtained at the cost of power consumption. At peak f_t, the power consumption of this HBT with 1.2 V and 1.8 V V_{CE} are 2.33 mW and 6.4 mW respectively. At higher supply the HBT consumes more power and hence the self heating of the transistor is of major concern. Due to this, 100 nm BOX thickness has been used in this design so that thin BOX will compensate for the thermal performance due to high supply voltage. The research efforts are on towards thin BOX devices [34, 35] that would improve the self heating performance.

The detailed study of the electro thermal behavior of the HBT has been studied in (V_{CE}, I_C) plane [36]. In this simulation collector-emitter voltage is varied. Thermal resistances of three SOI HBTs with different geometries are reported in [37] with values 4430, 5850 and 6680 K/W. The results reported [37] suggests that the thermal performance can be made better for properly choosing the device geometry. 3D TCAD simulation with lattice temperature will be required for finding the optimal device geometry and heat flow mechanism inside the device. In the 2D simulation study the geometry is limited by device width. Therefore, using 2D simulation, the geometry optimization cannot be done for finding the device structure for better thermal performance. A thermal resistance of $4x10^{-5}$ Kcm^2/W has been used between the SOI HBT and the heat sink for the simulation. Heat equations have been solved by coupling the temperature. The model parameters for analyzing the self heating effect are discussed in [18]. In this work the same parameters have been used to estimate the maximum lattice temperature of the SOI HBT. The maximum lattice temperature of SOI HBT is shown in Fig. 8 with different voltages. A maximum of 408 K temperature is observed in the HBT with 1.8 V of supply voltage and 1 mA of collector current. This value is 42 K higher compared to the HBT with 1.2 V of V_{CE} at 1 mA of collector current.

IV. Scaling of Epi Layer Thickness of SOI HBT

As the f_tBV_{CEO} product of the HBT is better with an epi layer doping value of $2.5x10^{17}$ cm^{-3}, this value has been used and the epi layer thickness has been scaled to study the HBT performance. The V_{CE} value is kept 1.2 V and V_{BE} is varied from 0 V to 1.2 V. The small signal analysis of the SOI HBT has been performed to obtain the ac voltage gain with different epi layer thicknesses. The voltage gains are compared and plotted as shown in Fig. 9. The results show that the voltage gain decreases as the epi layer thickness of the HBT decreases. This

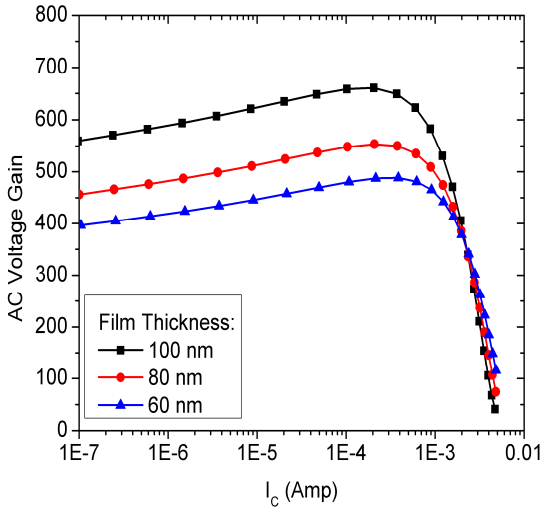

Fig. 9. AC Voltage gain of HBT.
Epi Layer doping=2.5x10^{17} cm^{-3} and the epi layer thickness is varied

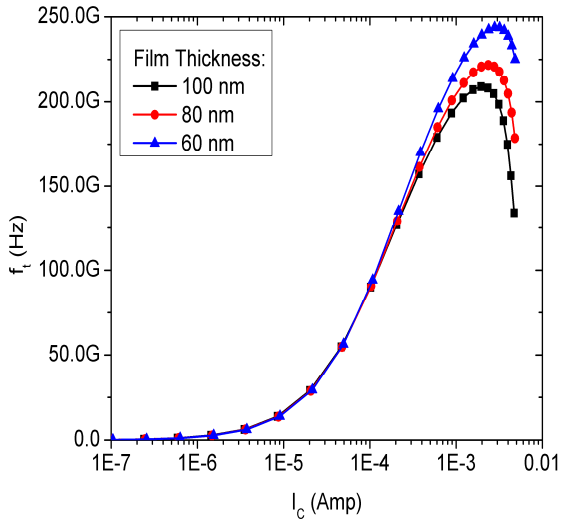

Fig. 10. f_t of SOI HBT.
Epi Layer doping=2.5x10^{17} cm^{-3} and the epi layer thickness is varied

reduction in voltage gain is due to the reduction in the output impedance resulting from the reduction in base-collector space charge region and the diffusion of dopants from the buried layer towards base side. The f_t values are plotted in Fig. 10 with different epi layer thickness values. The diffusion of dopants from the buried layer shows that the epi layer thickness can be scaled upto 60 nm. The onset of the Kirk current increases with the scaling of the epi layer thickness as discussed in the Eq. (1). Thus the device performance can be improved in terms of speed by scaling the epi

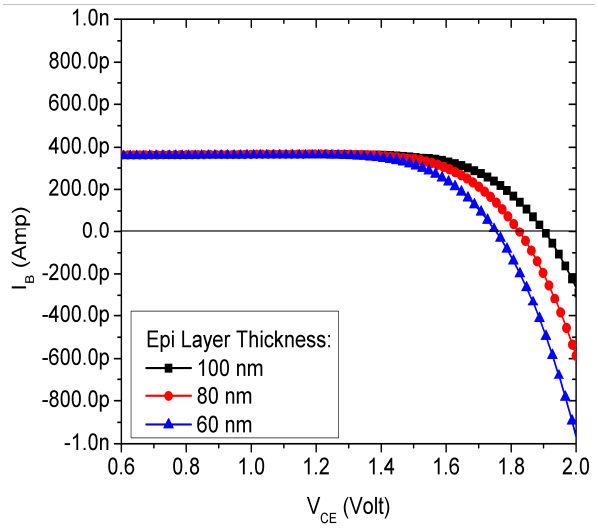

Fig. 11. BV_{CEO} of HBT.
Epi Layer doping=2.5x10^{17} cm^{-3} and the epi layer thickness is varied

Table 3. Performance comparison of HBT by varying epi layer thickness

Epi Layer Thickness (nm)	Peak f_t (GHz)	BV_{CEO} (Volt)	f_tBV_{CEO} Product (GHzV)	Power (mW)
100	208.9	1.975	358.4	2.33
80	221.7	1.842	367.3	2.84
60	243.9	1.75	426.8	3.35

layer thickness. The breakdown voltage of SOI HBT has been measured from base current reversal point at V_{BE}=0.7 V with different epi layer thicknesses. The results are plotted as shown in Fig. 11. As can be seen the high f_t value can be obtained at the cost of the breakdown voltage of the device. However, the breakdown volatge of 1.75 V is nominal for the transistor to be operated with 1.2 V of V_{CE}. The summary of the performance is given in Table 3.

By scaling the epi layer thickness of the HBT, high f_tBV_{CEO} product can be obtained. From the results it can be found that the HBT with 20 nm buried layer and 60 nm epi layer has a maximum of 243.9 GHz f_t value and 1.75 V of BV_{CEO} value resulting in 426.8 GHzV f_tBV_{CEO} product. This performance has been achieved at 3.35 mW of power consumption. The power consumption can be minimized by lowering the collector current instead of operating the HBT at its peak f_t value.

The simulation results suggest that the HBT with low epi layer thickness value would provide low power solution with reasonable performance. The f_tBV_{CEO}

product can be improved by increasing the base current in SiGe HBTs with a SiGe spike inside the emitter [38]. This technique would provide low current gain value as discussed in the paper. The physical and electrical performance limits of the HBT have been predicted in [39, 40]. In this work, process and device cosimulations have been performed so that high performance SOI BiCMOS technology could materialize. The HBT with thick buried layer would provide better performance. However, compatibility with fully depleted SOI CMOS will be a challenge because in advanced fully depleted SOI CMOS technology, the film thickness is very low. The addition of this HBT to fully depleted SOI CMOS technology would provide high performance SOI BiCMOS technology.

Also, the HBT with buried nickel silicide layer is investigated. The simulation studies show that the HBT with nickel silicide buried layer has less diffusion towards the epi layer. Due to this, the film thickness could be scaled upto 40 nm to reduce the collector transit time. In this case, the effective epi layer thickness is around 20 nm due to the diffusion from the buried silicide layer. Using 40 nm epi layer and 20 nm buried layer the f_t value of the HBT is 273 GHz. Although the performance is better in case of HBT with buried silicide layer, integrating the SOI HBT with buried silicide layer to the fully depleted SOI CMOS would be a challenge. There are process issues while integrating with SOI CMOS.

The benefits of designing analog/RF systems with HBTs and digital systems with CMOS are discussed in [41]. Similar benefits can be found using this technology particularly for highly integrated mixed signal chips. Thus, RF circuits and systems can be designed for 60 GHz short range communication and 77 GHz automotive radar applications [42] with better performance and low noise figure.

V. CONCLUSION

The simulation study of npn SOI HBT with buried layer has been performed with trapezoidal Ge profile. The epi layer doping is varied to vary the base collector space charge region inside the device and the tradeoff in the HBT performance is studied in terms of DC current gain, AC voltage gain, unity current gain frequency and breakdown voltage. From the results it is observed that a maximum of 397 GHzV f_tBV_{CEO} product can be obtained with $2.5x10^{17}$ cm^{-3} epi layer doping using V_{CE} of 1.2 V. As the breakdown voltage is higher at low value of epi layer doping, the supply voltage can be raised upto 1.8 V so that the f_tBV_{CEO} product can be improved to 465 GHzV. The lattice temperature of the HBT has been studied at different supply voltages. At 1 mA collector current, the maximum lattice temperature of the HBT is 42 K higher while applying V_{CE} of 1.8 V in comparison to the HBT at the V_{CE} of 1.2 V. The epi layer fim thickness is scaled to obtain the DC and AC characteristics of the npn SOI HBT. The f_tBV_{CEO} product of the HBT has been evaluated. With 60 nm epi layer thickness and 20 nm buried layer, the f_tBV_{CEO} product of the SOI HBT is 426 GHzV using 1.2 V of V_{CE}. This HBT can be used in high performance RF circuits and systems at 60 GHz and 77 GHz applications.

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