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NPN 트랜지스터의 에미터 면적이 에미터 전류 이득에 미치는 영향

(Effect of forward common emitter current gain on emitter area in NPN transistors)

이 정 환[1)]
(Jung-Hwan Lee)

요 약 본 논문에서는 대부분의 선형 집적회로와 집적 주입 논리 회로에 넓게 사용되고 있는 NPN 트랜지스터의 에미터 면적의 크기에 대한 순방향 전류 이득의 영향에 대해 연구하였다. 순방향 전류이득과 에미터 면적 사이의 관계를 실험과 시뮬레이션을 통해 확인하였다. 같은 에미터 길이에서 에미터 접합 깊이가 증가할수록 에미터 전류 이득은 감소하였다. 측면 면적에 비해 에미터 바닥 면적 비율이 증가할수록 에미터 전류이득은 증가하였다. 이론과 시뮬레이션의 결과는 실험결과와 함께 아주 잘 일치하였다.

핵심주제어 : 전류이득, 에미터 길이, 접합 깊이

Abstract In this paper, we present the effect of forward current gain on emitter area in NPN transistors are used widely in the almost linear integrated circuits and integrated injection logic. Relations between forward current gain and emitter area were conformed with the simulation with examined calculation and experiments. At the same emitter length, as junction depth is increased, common emitter current gain is decreased. Ratio of Emitter bottom area comparing to side area increases, the emitter current gain is increased. The theory and simulation results were fitted in with the experimental data very well.

Key Words : Current Gain, Emitter Length, Junction Depth

1. Introduction

NPN transistor is the very basic electrical device in the solid state electronics and electrical engineering. So, NPN transistors are used widely in the almost linear integrated circuits and integrated injection logic and their dc and ac characteristics have been studied by many authors[1]~[5]. Typically in the IC fabrication, NPN transistors are fabricated with some kinds of process and their characteristics are mainly affected by the thermal process, doping profile and junction depth, etc. Particularly, common emitter current gain is the function of the base and collector currents.

Recently, we find a effect of the forward common emitter current gain due to change of emitter size of NPN transistor. As the emitter size of NPN transistor is increased, the forward common

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emitter current gain is also increased. I found that the change in current gain causes a significant change in the characteristics of the device. So, I investigated the effect of the current gain due to the emitter size on the device design.[6][7]

In this paper, we proved this phenomena through the experiment and simulation through examined theory. Two kinds of NPN transistors that have different emitter diffusion length were fabricated and confirmed the characteristics of h_{FE}-Ic,. The experimental and simulation results were examined theoretically results very well.

2. Theory[8]

Basically, current components of NPN transistor are base and collector currents. Collector current of NPN transistor is given in equation (1), where

$$I_c = \frac{qAD_n n_b(0)}{W_b} \tag{1}$$

A is emitter size, D_n is diffusion coefficient of electron, $n_b(0)$ is carrier distribution in the base region which is given in equation (2), W_b is base width.

$$n_b(0) = n_{b0}\exp\left[\frac{V_{BE}}{V_t}\right] \tag{2}$$

where n_{b0} is initial carrier concentration of the base region, V_{BE} is base-emitter potential barrier height, V_t is thermal voltage.

Base currents are consisted of four components. The bulk recombination current in the neutral base(I_{B1}) is given in the equation (3), where p_{nE} is excess hole concentration at the base edge of the emitter space-charge layer, V_B is effective volume of the base, τ_p is bulk recombination life time, q is charge constant.

$$I_{B1} = \frac{qp_{nE}V_B}{\tau_p} \tag{3}$$

The recombination current in the neutral emitter(I_{B2}) is given in the equation (4), where ni is intrinsic carrier cocentration, A_E is effective emitter area, Q_E is total number of acceptors per unit area of emitter.

$$I_{B2} = qn_i^2 A_E \frac{D_{nE}}{Q_E}\left[\exp(qV_{EB}/kT) - 1\right] \tag{4}$$

The recombination current in the emitter-base junction space charged region(I_{B3}) is given in equation (5), where τ_{n0} and τ_{p0} are the electron and hole lifetime in the space-charge layer, $f(V_{EB})$ is a function of forward bias and the parameters characterizing the recombination center, W_0 is the space-charge layer width at zero bias.

$$I_{B3} = \frac{qn_i}{2\sqrt{\tau_{n0}\tau_{p0}}} A_E W_0 f(V_{EB}) \tag{5}$$

The Recombination current through surface states at oxide-silicon interface(I_{B4}) is given in equation (6).

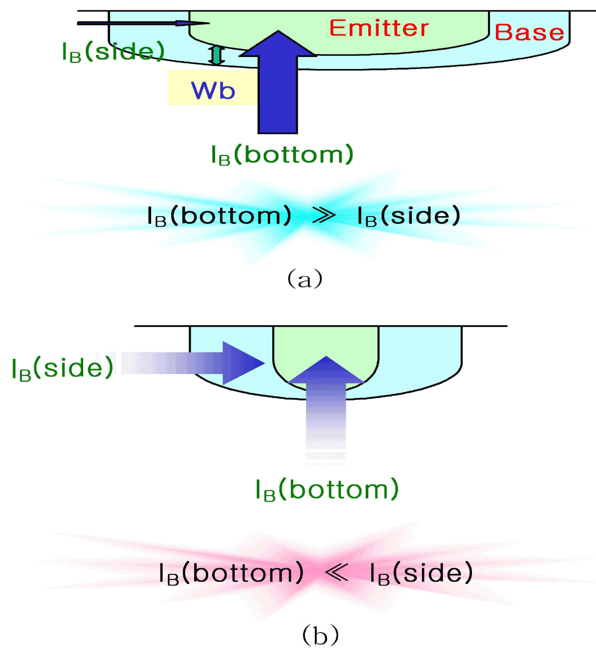
$$I_{B4} = \frac{1}{2} q s_0 \left[n_i l_E W_0 f_s(V_{EB}) + A_{BS}\frac{n_i^2}{N_D}(\exp(qV_{EB}/kT) - 1)\right] \tag{6}$$

where l_E is emitter perimeter, s_0 is surface recombination velocity, $f_s(V_{EB})$ is identical to the function $f(V_{EB})$ defined in (5), A_{BS} is the oxide-covered surface area over the neutral base. The total current is sum of four base current components given in equation (7)[9].

$$I_{B(tot)} = \sum_i I_{Bi} \tag{7}$$

The bottom and side-wall of emitter current components in the base region are shown in the <Fig. 1> Large and small emitter area cases are shown in the <Fig. 1>(a) and (b), respectively. When the emitter area is very large, almost collector and base currents are flow through the bottom region of emitter. Therefore side-wall components can be neglected. So, the forward common emitter current gain is given in equation (8).

$$\beta_0 = \frac{I_c}{I_{B(tot)}} = \frac{I_c}{\sum_i I_{Bi}} = \frac{AB \times J_c}{AB \times J_{B(tot)}} = \frac{J_c}{J_{B(tot)}} \quad (8)$$



<그림 1> 에미터 면적이 크고(a) 작은(b) NPN 트랜지스터의 전류 흐름 도해

<Fig. 1> Current flow schematics of NPN transistors with(a) large (b) small emitter area.

But as the emitter area is more and more decreased, the side-wall area is increased comparing to bottom area. Total emitter area is composed five components(①-⑤). They are given in the equation (9). Side - wall components are ①,②,③, bottom component is ④ and surface recombination component between oxide and silicon is ⑤.

$$① : (2\pi X_{je} \times A) \times \frac{1}{4} \times 2 = \pi X_{je} A$$

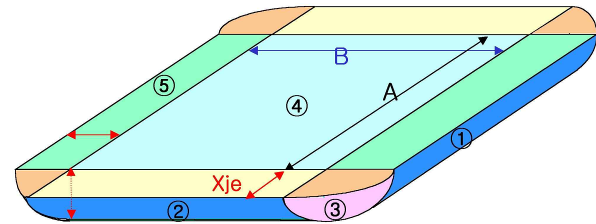
$$② : (2\pi X_{je} \times B) \times \frac{1}{4} \times 2 = \pi X_{je} B$$

$$③ : (4\pi X_{je}^2) \times \frac{4}{8} = 2\pi X_{je}^2 B$$

$$④ : AB$$

$$⑤ : X_{fs} \quad (9)$$

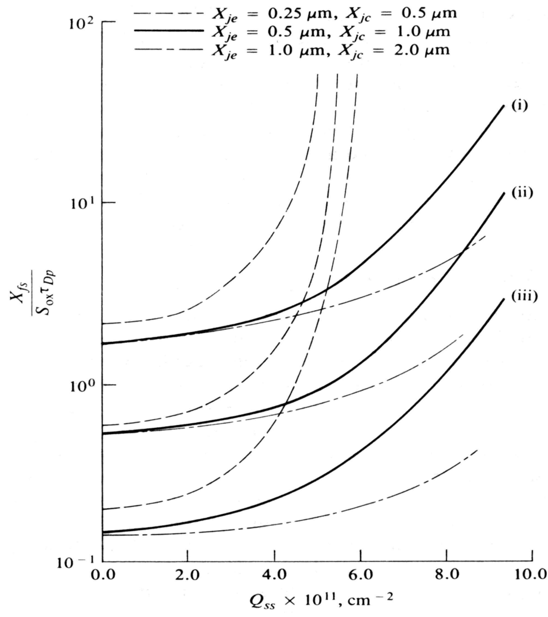
<Fig. 2> shows the three-dimensional nature of the emitter region. where A and B are width and length of emitter, X_{je} is emitter junction depth, X_{fs} is surface recombination parameter. The value of X_{fs} may be determined numerically if the relevant recombination data is known,



<그림 2> 에미터 영역의 3차원 개략도

<Fig. 2> The three-dimensional nature of the emitter region.

<Fig. 3> gives results normalized with respect to surface oxide recombination velocity S_{ox} and bulk hole lifetime τ_{DP} [10]. In general case, almost X_{fs} is limited between 0.1 to 100, and it is very wide range.



<그림 3> 정규화한 표면 재결합 변수

<Fig. 3> Normalized surface recombination parameter [10].

The total emitter area is given equation in (10), In the small emitter area case, the side-wall area current components can't be neglected due to the increasing of side-wall base current comparing to the bottom currents.

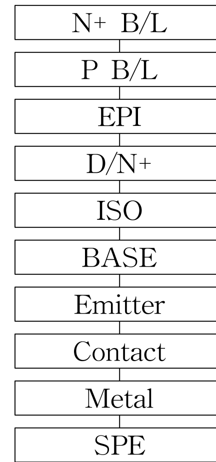
$$AB_{tot} = AB + \pi X_{je}(A+B) + 2\pi X_{je}^2 + X_{fs} \qquad (10)$$

In this case, But side-wall collector current is not increased comparing to the large area case. Forward common emitter current gain is proved in equation (11) and related with large area case with decreasing factor of AB/AB_{tot}. Therefore, in the small area case, forward common emitter current gain is more affected by the emitter area, particularly emitter junction depth.

$$\beta = \frac{I_c}{I_{B(tot)}} \qquad (11)$$
$$= \frac{I_C}{\sum_i I_{Bi}}$$
$$= \frac{AB \times J_C}{\left[AB + \pi X_{je}(A+B) + 2\pi X_{je}^2 + X_{fs}\right] \times J_{B(tot)}}$$
$$= \frac{AB}{AB + \pi X_{je}(A+B) + 2\pi X_{je}^2 + X_{fs}} \times \frac{J_C}{J_{B(tot)}}$$
$$= \frac{AB}{AB + \pi X_{je}(A+B) + 2\pi X_{je}^2 + X_{fs}} \times \beta_0$$

3. Experiment

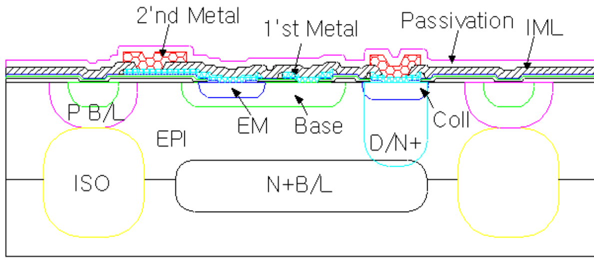
<Fig. 4> is a fabrication process, which is conventional process of NPN transistor. In this experiments, we proceeded two kinds of processes which have different emitter junction depth. One is about 2.5㎛(process A) and another is about 0.5㎛ (process B) of emitter junction depth. The thickness and resistivity of epi-layer are 9-13㎛, 1.5-4.0Ω·㎝ (process A), and 6㎛, 1.25Ω·㎝(process B), respectively. Each step of fabrication process is mask name. B/L is buried layer, EPI is epitaxial, D/N+ is Deep N+, ISO is isolation, SPE is the surface passivation etch.



<그림 4> NPN 트랜지스터의 제작공정 흐름

<Fig. 4> Fabrication process flow of NPN transistor.

The schematic description of the NPN transistor is shown in the <Fig. 5>



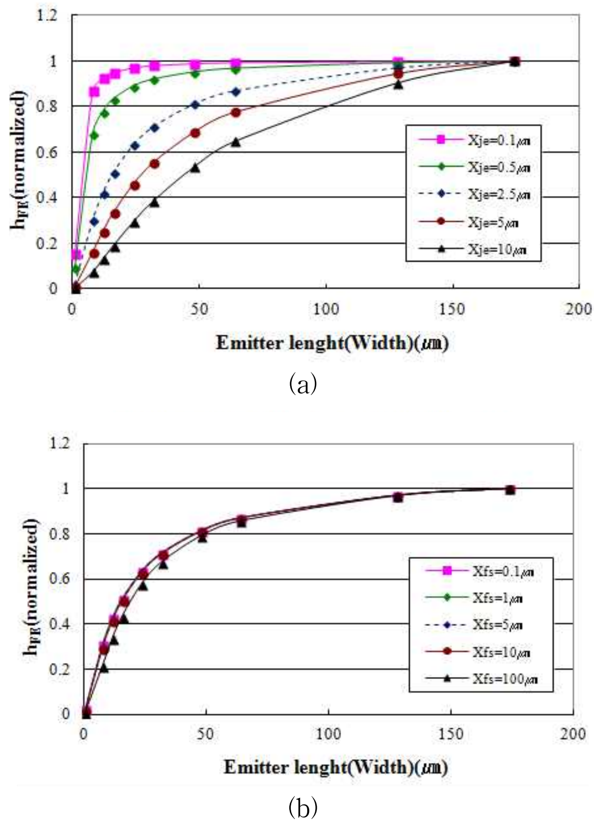
<그림 5> 제작된 NPN 트랜지스터의 단면도

<Fig. 5> Cross-sectional view of fabricated NPN transistor.

4. Results and discussion

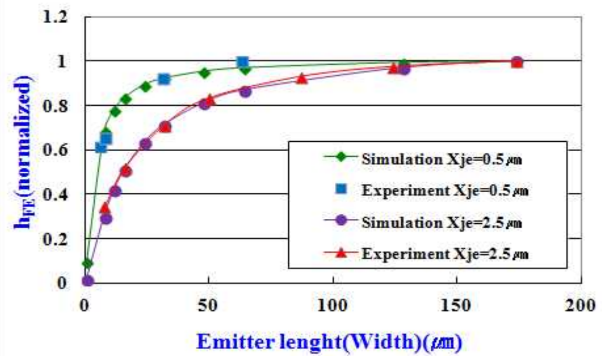
In this paper, to demonstrate the effect of forward common emitter current gain on the emitter area of NPN transistor, we simulated dependence of the current gain on the emitter size of NPN transistor using equation of (11). <Fig. 6> is the results of the simulation.

Changing the emitter size, normalized common emitter current gain is depends on the emitter junction depth. At the same emitter length, as junction depth is increased, common emitter current gain is decreased. Particularly, when the emitter length is 25㎛, as the emitter junction depth is increased from 0.2㎛ to 0.5㎛, the normalized current gain is decreased from 0.9 to about 0.5. seeing in the <Fig..6> On the other hand, the emitter length is more larger over than 150㎛, all characteristics are converged to 1. So, the emitter size and junction depth is more smaller, the common emitter current gain is more affected. But X_{fs} is not affected in the normalized common emitter current gain at the same X_{je} of 2.5㎛. seeing <Fig. 6>(b), Even if, the X_{fs} is varied between 0.1 to 100, all the characteristics have similar values.



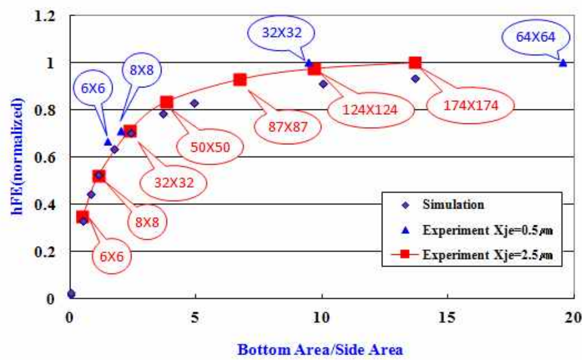
<그림 6> (a) X_{fs}가 5㎛ (b)X_{je}가 2.5㎛의 시뮬레이션 결과

<Fig. 6> Simulation results. (a)X_{fs} is 5㎛ (b) X_{je} is 2.5㎛.



<그림 7> NPN 트랜지스터의 에미터 길이와 정규화된 공통에미터 전류이득의 시뮬레이션 및 실험 결과

<Fig. 7> Emitter length vs. normalized common emitter current gain of the simulation results and experimental data of NPN transistor.



<그림 8> NPN 트랜지스터의 에미터 바닥과 측면 면적 비율에 대한 시뮬레이션 결과 및 실험값의 정규화된 공통에미터 전류이득

<Fig. 8> Ratio of emitter bottom area and side-wall area vs. normalized common emitter current gain of simulation results and experimental data of NPN trnasistor.

Emitter length vs. normalized common emitter current gain of simulation results and experimental data are seen in <Fig. 7> Both case of process A and B are well fitted with simulation results. The ratio of emitter bottom area and side-wall area vs. normalized common emitter current gain of simulation results and experimental data are seen in <Fig. 8> At the same ratio, as the emitter junction depth is larger, emitter area is also more larger. And as emitter junction depth is larger, the current gain is sensitive to the emitter area.

5. Conclusion

In this paper, the dependence of the emitter area and junction depth on the forward common emitter current gain was proved through the experiments and simulation, and it was examined theoretically. As the emitter junction depth is smaller the normalized common emitter current gain is increased. And as the emitter length is larger, the normalized common emitter current gain is increased. And Ratio of Emitter bottom area comparing to side area is increased, the emitter current gain is increased.

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