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High Quality Vertical Silicon Channel by Laser-Induced Epitaxial Growth for Nanoscale Memory Integration

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***Abstract*—As a versatile processing method for nanoscale memory integration, laser-induced epitaxial growth is proposed for the fabrication of vertical Si channel (VSC) transistor. The fabricated VSC transistor with 80 nm gate length and 130 nm pillar diameter exhibited field effect mobility of 300 cm^2/Vs, which guarantees "device quality". In addition, we have shown that this VSC transistor provides memory operations with a memory window of 700 mV, and moreover, the memory window further increases by employing charge trap dielectrics in our VSC transistor. Our proposed processing method and device structure would provide a promising route for the further scaling of state-of-the-art memory technology.**

***Index Terms*—Vertical silicon channel, laser-induced epitaixal growth, 1T DRAM, floating body effect**

I. INTRODUCTION

Recently, integration of memory cells such as flash or dynamic random access memory (DRAM) confronts serious scaling issues [1]. In case of DRAM, as an alternative technology with relaxed scaling constraints, capacitor-less one-transistor (1T) DRAM cells have been investigated by several research groups [2, 3]. Impact ionization or gate induced drain leakage generates excess majority carriers in floating body, which switches the channel conductance of metal-oxide-semiconductor field effect transistor (MOSFET) from a low conductance state to a high conductance state [2, 3]. The drain current between two states can then be sensed in the linear operation regime of MOSFET, allowing us to determine memory states. 1T DRAM can be scalable to the minimum unit cell area of 4F^2 (F: minimum feature size) in vertical device architecture [3], which provides larger scale integration at the same technology node. Vertical integration of memory cells is also important in recent flash memory development [4], where the effective unite cell size can be reduced below 4F^2 by three dimensional stacked integration. These indicate that the formation of high quality vertical Si channel (VSC) is essential in nanoscale memory integration. In channel-first-gate-last scheme, VSC can be readily formed by etching Si wafers [5] via conventional semiconductor manufacturing processes, but several integration difficulties can be addressed in this scheme: e.g., forming gate electrodes with accurate vertical lengths and controlling sidewall profile or its surface roughness by dry etching [6]. In gate-first-channel-last scheme, high quality VSC can be attained without using Si wafers, which requires selective epitaxial growth techniques on pre-patterned vertical holes as VSC molds. Among selective epitaxial growth techniques [7], laser-induced epitaxial growth (LEG) has been proved to give high quality as Si wafers at low processing temperatures [8]. In this work, we have

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fabricated VSC transistors using the gate-first-channel-last scheme using LEG to prove that LEG is an essential element in nanoscale memory integration. In addition, 1T DRAM cell with an ultimate scalability of $4F^2$ will be demonstrated using the fabricated VSC transistor, whose promising aspect in scaling will also be discussed.

Table 1 show the process sequence and detailed process parameters to fabricate the VSC transistors on a bulk-silicon substrate. Fig. 1 illustrates the sequence of gate replacement process, where single crystalline silicon channel is obtained by LEG process. After the conventional shallow trench isolation process, ion implantations (P^+, 20 keV, 8×10^{12} cm^{-2}) were performed to form bottom source and drain junctions. In addition, silicon nitride/silicon oxide/silicon nitride ($SiN/SiO_2/SiN$) layers were deposited by low pressure chemical vapor deposition (LPCVD); where the top and bottom SiN layers were used as the isolation layer, and the sandwiched SiO_2 was used for the dummy gate. The holes for transistor channels were patterned by ArF-based photolithography and dry etching. Subsequently, 50 nm-thick amorphous silicon thin film was deposited by LPCVD and then chemical-mechanical polishing process was employed to remove the amorphous silicon on top of the SiN layer. Afterward, in order to perform an epitaxial growth of amorphous silicon in the channel hole area, an Nd:YAG laser beam was irradiated with a wavelength of 532 nm and a pulse duration of 150 ns [9], where the energy density of irradiated laser beam was adjusted to optimize the epitaxial growth. The vertical channel region was doped by B^+ (3×10^{13} cm^{-2}, 27 keV) implantation to control short channel effect, and top source/drain junction was formed by ion-implanting P^+ (10^{13} cm^{-2}, 10 keV) and As^+ (10^{15} cm^{-2}, 10 keV) followed by a rapid thermal annealing at 1000°C for dopant activation. We have used two different types of gate dielectric (SiO_2 and $SiO_2/SiN/SiO_2$) prior to the gate material deposition for a comparative study of 1T DRAM devices. The single dielectric layer SiO_2 of 4 nm is formed by thermal oxidation followed by NH_3 anneal at 900°C, and the multilayered dielectric $SiO_2/SiN/SiO_2$ (4 nm/6 nm/6 nm) is fabricated by additional thin film deposition of SiN and SiO_2 using an LPCVD on the 4nm-thick thermal oxide. Finally, we have used doped polycrystalline Si as the gate electrode, followed by the contact formation and metallization using a conventional silicon process technology.

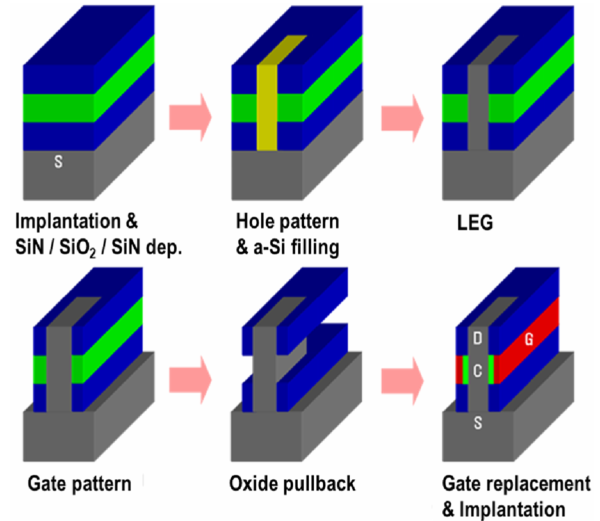

Fig. 1. Schematic process sequence of gate replacement process.

Table 1. Details of critical process parameters in the fabrication of VSC, and their process sequence.

Parameters	Conditions	Process sequence
Pillar height	150 nm	• Shallow trench isolation
Pillar	130 nm	• SiN/SiO_2 layer deposition
Gate oxide	SiO_2, ONO	• Channel hole etch
Channel Si	a-Si, poly-Si, c-Si	• Channel Si formation (a-Si dep. & crystallization by LEG)
Gate material	Doped Poly-Si	• Gate replacement process (oxide etchback, oxidation, poly-Si dep.)
Gate length	80 nm	• Contact formation • Metallization

Fig. 2 shows schematic diagrams and electron microscopy images of VSC transistor, where Fig. 2(a) displays the layout of the VSC transistor with the gate all around structure and the unit cell area of $4F^2$. The planar scanning electron microscopy (SEM) image in Fig. 2(b) depicts the contact hole with a diameter of 90 nm. Fig. 2(c) illustrates three dimensional schematic representing the unit cell area of 4F2 with stacked word line (WL), bit line (BL), self-aligned contact (SAC) to the active Si, and direct contact (DC) to SAC shifted by 0.5F. In Fig. 2(d), a cross-sectional transmission electron microscopy image of the fabricated VSC transistor is shown, where single crystalline VSC is formed by LEG.

The crystallinity of VSC plays a crucial role in the device performance. The polycrystalline and epitaxial single crystalline silicon channels are prepared by changing the energy density of the incident laser beam

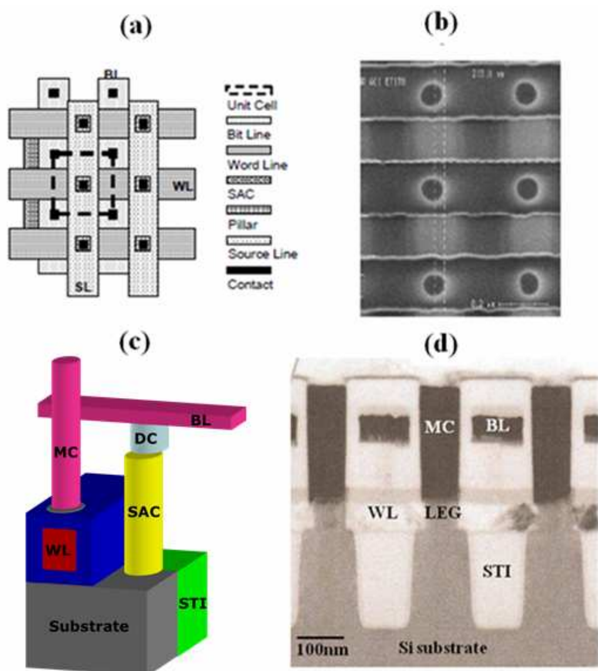

Fig. 2. Schematic diagrams and electronic microscopy images of VSC transistors (a) planar layout, (b) planar SEM image, (c) three dimensional illustration, (d) cross sectional TEM image.

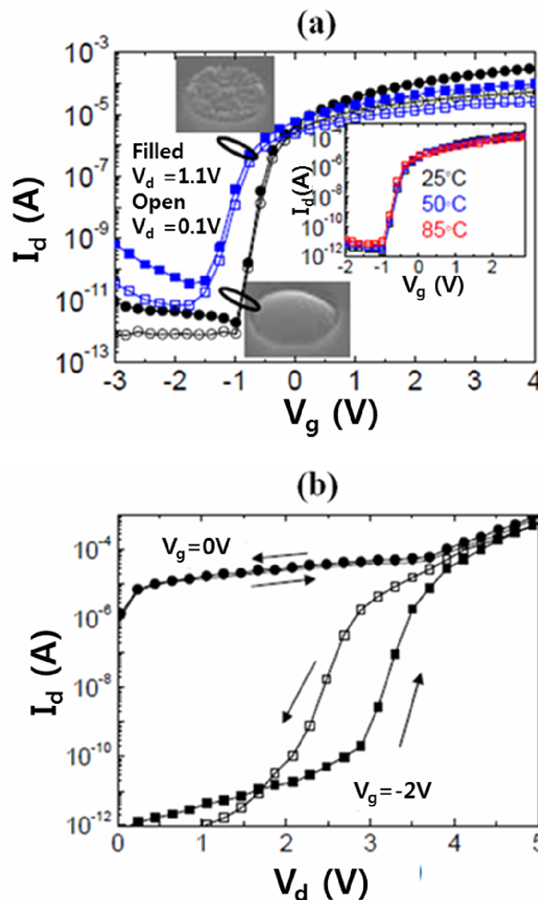

Fig. 3. (a) Transfer curves of the VSC transistors with polycrystalline (upper curves) and single crystalline (lower curves) VSC. Inset shows the planar SEM images of surface morphologies of poly crystalline (upper image) and single crystalline LEG Si (lower image). Right inset shows temperature dependent transfer curves of VSC transistor with single crystalline Si channel, (b) The output characteristics (semi-logarithmic current versus voltage) of VSC transistor with hysteresis measurement.

ranging from 700 mJ/cm^2 to 1000 mJ/cm^2 during the LEG process [9-12]. Fig. 3(a) shows the transfer characteristics of the vertical pillar transistor with polycrystalline (900 mJ/cm^2) and single crystalline (1000 mJ/cm^2) LEG silicon. For the fabricated transistor with the single crystalline LEG silicon, the electrical characteristics can be summarized as follows: field effect mobility of 300 cm^2/Vs, threshold voltage of 0.2 V, and sub-threshold slope of 100mV/decade. While the transistor with poly-crystalline silicon shows field effect mobility of 80 cm^2/Vs, threshold voltage of -0.3 V and sub-threshold slope of 145 mV/decade. In addition, the inset SEM images in Fig. 3(a) indicate different surface morphologies of polycrystaline and single-crystalline Si depending on the energy density of the incident laser beam. Moreover, negligible temperature dependence in leakage currents of VSC transistor with LEG Si indicates high quality crystalline nature (inset graph of Fig. 3(a)) [13, 14].

The drain current of VSC transistor is a function of the potential of VSC, and the potential at VSC is variable according to the charge density in VSC. That is, due to the floating body effect [2, 3], the VSC transistor can be used as 1T DRAM. Drain voltage hysteresis demonstrates the floating body effect as shown in Fig. 3(a). Considering that the measurement time of hysteresis sweep was estimated to be around 100 ms, the memory window determined from this drain voltage implies the memory window for the 100ms retention time. As shown in Fig. 3(a), the memory window is 0 V at the gate bias of 0 V, while memory window of 0.7 V is observed with the gate bias of -2 V. This implies that an additional negative gate bias is required for sensing with refresh time around 100 ms in our VSC 1T DRAM. Applying a negative bias of -2 V on the gate provides a deeper potential well for the storage of excess holes inside the vertical silicon channel, which increases the memory window and retention time [2, 3].

Electron trapping at the gate insulator is an alternative strategy for the enhancement of the memory window instead of the negative gate bias. To prove this concept, two types of gate dielectrics, i.e., SiO_2 and SiO_2/SiN/SiO_2 (ONO), were compared to observe the further enhancement of memory window. The former is almost trap-free dielectric, and the latter has a trap-rich SiN layer between trap-free SiO_2 layers. Prior to applying drain bias for the hyeteresis measurement, charging bias (V_{charge}) was applied to trap electrons in the gate dielectrics. In an ONO gate dielectric, electrons are charged in nitride layer by tunneling through the bottom oxide, which is a well-known mechanism in charge trap flash memories [15]. The negative charges in the gate dielectric enhance the junction barrier between the channel and source/drain. As shown in Fig. 4(a), electron trapping at ONO gate dielectric enhances memory window, and this enhancement increases with more electron trapping by increasing V_{charge}. Charge retention of ONO can be larger than 10 years [15], and thus, V_{charge} is necessary only during the memory production. This approach based on charge trapping gives more promising options in the application VTC 1T DRAM since negative voltages are not required for device operations.

In scaling VTC 1T DRAM, the diameter of the pillar is the key parameter in determining the cell size. Fig. 4(b) shows simulated cell size of VTC 1T DRAM versus design rule, where several pillar diameters are used and the width of WL is set twice of the design rule. It is seen that VTC 1T DRAM can provide a solution for high density DRAM with the cell area of about $4F^2$ when structure parameters are optimized, that is, smaller pillar diameter is crucial. To attain ultimate scalability in VTC 1T DRAM, development of patterning and dry etching technologies for nano-sized holes would be important; and further investigation on the performance of LEG in nano-sized pillars is also required.

In summary, we have demonstrated that LEG is a promising process method for nanoscale memory integration by demonstrating high performance VSC transistors with field effect mobility around 300 cm^2/Vs. In addition, we have demonstrated a VSC 1T DRAM by employing charge trap gate dielectric, which exhibited enhanced memory window as the amount of charge trapping increased. We believe that high quality VSC by LEG is a promising elements in future nanoscale memory integration, and in particular, VSC 1T DRAM harnessing charge trap dielectric will provide a solution for scaled DRAM below 20 nm.

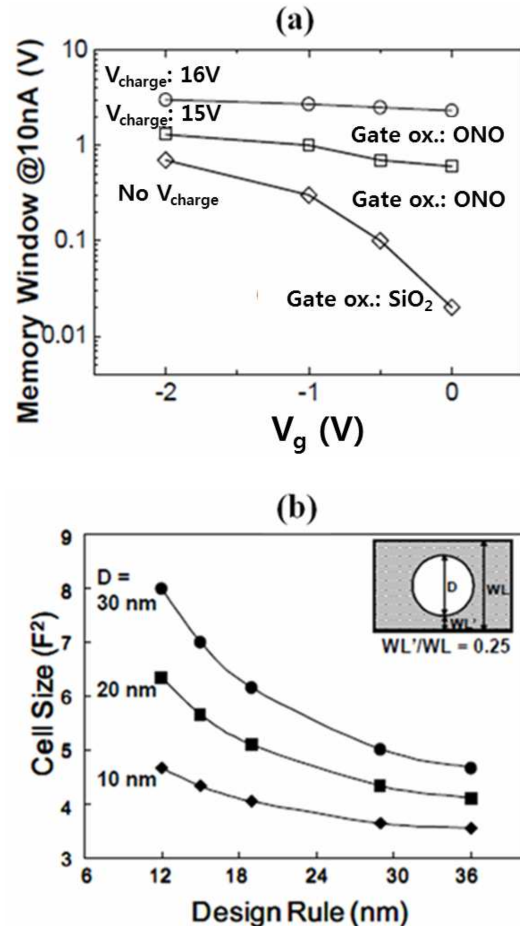

Fig. 4. (a) Memory window versus applied gate bias at various charging conditions, (b) Simulated cell size (the unit is the square of the minimum feature size F) of VSC transistor versus design rule, where three pillar diameters are applied.

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