Preparation and Properties of $ZnSe/Zn_3P_2$ Heterojunction Formed by Surface Selenization of Zn_3P_2 Film Deposited on ZnTe Layer

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ABSTRACT: $ZnSe/Zn_3P_2$ heterojunctions with a substrate configuration were fabricated using a series of cost-effective processes. Thin films of ZnTe and Zn_3P_2 were successively grown by close-spaced sublimation onto Mo-coated glass substrates. ZnSe layers thinner than 100nm were formed by annealing the Zn_3P_2 films in selenium vapor. Surface selenization generated a high density of micro-cracks which, along with voids, provided shunt paths and severely deteriorated the diode characteristics. Annealing the Zn_3P_2 film at 300°C in a $ZnCl_2$ atmosphere before surface selenization produced a dense microstructure and prevented micro-crack generation. The mechanism of micro-crack generation by the selenization was described and the suppression effect of $ZnCl_2$ treatment on the micro-crack generation was explained. $ZnSe/Zn_3P_2$ heterojunctions with low leakage current (J_0 < 1 μA/cm^2) were obtained using an optimized surface selenization process with $ZnCl_2$ treatment. However, the series resistance was very high due to the presence of an electrical barrier between the ZnTe and Zn_3P_2 layers.

Key words: Zn_3P_2, heterojunction, selenization, ZnSe, ZnTe

1. Introduction

Low cost, earth abundant materials of solar absorbers will be required for large scale deployment of photovoltaics. Zn_3P_2 has been identified as a material with low extraction cost[1]. The light absorption coefficient is greater than 10^4/cm and the band gap is 1.5eV, which is in the optimum range for efficient photo-energy conversion[2,3]. These properties, in addition to the abundance of elemental zinc and phosphorus, are promising for scalable thin-film photovoltaic applications.

Because of the difficulties in preparing n-type Zn_3P_2, device fabrication with a Zn_3P_2 absorber has focused on Schottky barrier solar cells. Schottky structures have demonstrated solar energy-conversion efficiencies of 6% for devices fabricated on Zn_3P_2 wafers and 4.3% for devices on Zn_3P_2 thin films deposited by close-spaced sublimation (CSS)[4,5]. However, these devices were reported to have a high concentration of interface states, which limits the open-circuit voltage (V_{oc}) to less than 0.5 V due to Fermi-level pinning[6]. Optical absorption and reflection losses at the metal-semiconductor contact also limit the attainable short-circuit current densities (J_{sc}) in Schottky barrier devices. These restrictions on the Zn_3P_2 Schottky device thus present challenges to obtaining further improvements in the conversion efficiency.

To overcome the Schottky barrier problem, Zn_3P_2 heterojunction solar cells have been fabricated using various n-type emitters such as ZnO, ITO, CdS, ZnSe, and ZnS[7-13]. The conversion efficiencies of these devices to date are less than 3%. Nevertheless, in some cases, the V_{oc} values surpass those of Zn_3P_2 Schottky barriers, which suggests that efficiency enhancements are possible through the optimization of the heterojunction design.

Pawlikowski fabricated a $ZnSe/Zn_3P_2$ solar cell using CSS for depositing ZnSe and Zn_3P_2 layer on glass substrate coated with a semitransparent Al layer. He reported a V_{oc} value of 0.84 V[9]. However, the J_{sc} was less than 1 mA/cm^2. The reason for the low value of J_{sc} was attributed to the low net electron concentration in ZnSe, which resulted in an extensive barrier and a presumed high recombination at the interface. The ZnSe in this cell was very thick (> 600 nm), probably because a thinner ZnSe layer might be completely dissolved by inter-diffusion of

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Se and phosphorus atoms during the Zn_3P_2 deposition by CSS.

Kakishita et al. also fabricated ZnSe/Zn_3P_2 solar cells on ZnSe single crystal substrates using a photo MOCVD method for depositing Zn_3P_2 and obtained a J_{sc} of 9 $\mu A/cm^2$ [12,13]. This small J_{sc} was also attributed to the high resistance of ZnSe crystals. To improve the J_{sc}, it appears necessary either to reduce the ZnSe resistance, which is difficult due to self-compensation, or to reduce the ZnSe thickness. In the case of ZnSe/CIGS solar cells, an extremely low thickness of the ZnSe buffer is needed for highly efficient devices. The reported optimum ZnSe thickness was in the range of 5-10 nm[14].

A thin ZnSe layer appears better suited to the heterojunction with a substrate configuration than that with a superstrate configuration. However, it is difficult to select a right formation method of thin ZnSe for a robust ZnSe/Zn_3P_2 heterojunction cell with a substrate configuration. Damage is a concern in the sputtering process. For ZnSe chemical bath deposition, the solution contains toxic hydrazine hydrate and the reaction of Zn_3P_2 with hot water generates toxic phosphine (PH_3) gas and causes dissolution and delamination of the film[15]. High source temperature (> 700ºC) is needed to deposit ZnSe film by CSS or thermal evaporation. Thus, we investigated a novel cost-effective method to form a thin ZnSe layer on the Zn_3P_2 absorber, i.e., selenization of the Zn_3P_2 surface (called surface selenization) by annealing the Zn_3P_2 layer in Se vapor.

For Zn_3P_2 film deposition, we used the CSS process because it is cheap and is widely used for growing various semiconductor films. During the Zn_3P_2 CSS process, the substrate temperature is raised to over 400ºC. Thus the substrate and the back contact on it should have good thermal stability. Chu, et al. reported that cracks were present in all deposited films of Zn_3P_2 on graphite, glass, ceramic, and copper substrates due to the large differences in thermal expansion coefficients[16]. However, Cimaroli et al. deposited Zn_3P_2 film with minimal micro-cracks on soda-lime glass, which has a coefficient of thermal expansion close to that of Zn_3P_2[17]. In our study, a sodium-doped ZnTe layer deposited on Mo-coated soda-lime glass was used as a substrate for depositing Zn_3P_2 film. Sodium-doped ZnTe is used for a low resistance back contact. ZnTe is a p-type semiconductor and can be highly doped with sodium[18]. Although the barrier height of a Mo contact on ZnTe is large (1.0 eV), the I-V curves do not show the blocking behavior of two back-to-back diodes and a contact resistance lower than that of Au can be obtained[19]. A Mo contact with a ZnTe interlayer has also been used in the CdTe solar cell with a substrate configuration[20].

2. Experimental

ZnSe/Zn_3P_2 heterojunctions were fabricated by a series of cost-effective processes. Sodium-doped ZnTe films were deposited as back contact interlayers by CSS onto Mo-coated glass substrates. Source material prepared by mixing 99.99% purity ZnTe powder with 10wt% of Na_2Te was placed in a graphite crucible and a Mo-coated substrate with dimensions of 25×50 mm^2 was located 10 mm above the source material. A graphite susceptor was place on top of the glass substrate. The source and substrate were inserted into a quartz tube filled with nitrogen. The source was heated with IR halogen lamps, from room temperature to 650ºC in 10 min., held for 5 min. at 650ºC, and then naturally cooled to room temperature. The temperatures were measured on the graphite crucible and susceptor with thermocouples. The substrate was not heated intentionally, but the temperature rose to 450ºC during the film deposition.

The Zn_3P_2 layers were also deposited onto the ZnTe layers by the CSS process using a 99.999% purity Zn_3P_2 powder source. The source temperature was 600ºC and the deposition time was 3min. The Zn_3P_2 layers on ZnTe were annealed in Se vapor to form thin layers of ZnSe. The temperatures of the Se (99.999% purity) source and substrate and the annealing time were varied.

After selenization of the Zn_3P_2 surface, around 50 nm-thick undoped ZnO was deposited by radio-frequency magnetron sputtering at 50 W and the bilayer Al-doped ZnO (AZO) was deposited consecutively. The bilayer AZO film was used to minimize the sputtering damage and the film resistance[21]. It consisted of 50 nm-thick AZO deposited at 50 W as a damage protection layer and 250 nm-thick AZO deposited at 200 W as a conducting layer. Finally, a front grid of Al was deposited by vacuum evaporation using resistance heating. The thickness of the Al grid was about 700 nm and the active cell area was 0.44 cm^2.

The microstructure of the samples was investigated using scanning electron microscopy (SEM). The depth profiles of the constituent elements were studied using x-ray photoelectron spectroscopy (XPS). The sputter etch rate for XPS depth profiling was ~0.4 nm/sec. The electrical resistance of the thin films was measured with four-point probes. The dark and light J-V characteristics were measured with HP4145 and Mac Science solar simulator (AM 1.5, 100 mW/cm^2), respectively.

3. Results and Discussion

Fig. 1 shows the cross-sectional morphology of the ZnSe/Zn_3P_2 heterojunction device. The interface between the Zn_3P_2 layer and the ZnTe layer is clearly seen. The thicknesses of the ZnTe and Zn_3P_2 layers are ~2 μm and ~4 μm, respectively. The grains of Zn_3P_2 apparently much well developed and close packed. From the size of grain on the surface the grain size is estimated as 0.5-1 μm.

Since ZnSe layer was formed by selenization of the surface of Zn_3P_2 layer, it is a simple substitutional reaction and no clear boundary is seen between ZnO and Zn_3P_2. The surface seems fairly rough because of well faceted Zn_3P_2 grains.

Fig. 2 shows the depth profiles of Zn, Se, P, and O atomic concentrations before ZnO deposition to investigate the effect of surface selenization. The Se source temperature and specimen substrate temperature during surface selenization were 200 and 300ºC, respectively. The selenization time was 5 min. The concentration of Se at the surface is about 50 atomic percent and the tail of Se distribution extended to ~300 nm. The thickness of ZnSe was less than 100 nm and $ZnSe_{1-x}P_x$ alloy exist between 100 to 200 nm. The existence of alloy at the interface lowers band gap of light absorbing layer; this causes a negative effect on solar cell performance[22].

Fig. 3 shows the dark J-V characteristics of several ZnSe/Zn_3P_2 heterojunctions fabricated using the surface selenization process. The variation of the characteristics is very large. Only a few samples have normal diode characteristics and the others are very leaky or shorted.

To understand the shunt paths of high leakage, the surface microstructures were investigated at three different process steps (Fig. 4). After Zn_3P_2 deposition (Fig. 4(a)), the surface shows some voids between the grains, but cracks were not found. However, after selenization, micro-cracks, marked with white arrow in Fig. 4(b), were easily observed. It is not easy to understand the mechanism of micro-crack generation because

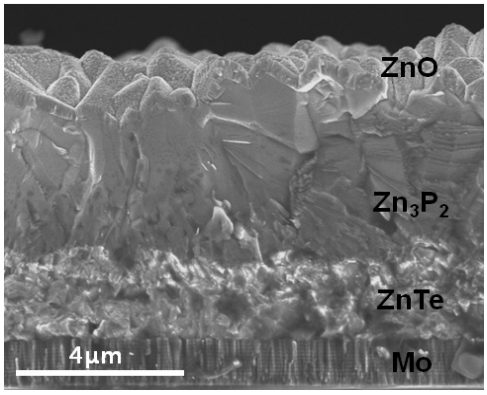

Fig. 1. Cross-sectional SEM image of the ZnSe/Zn_3P_2 heterojunction device

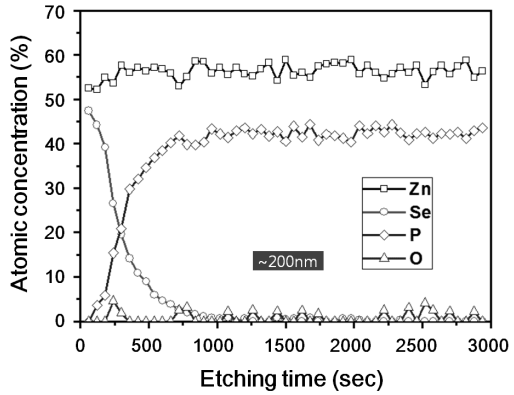

Fig. 2. XPS depth profiles of Zn, Se, P and O atomic concentration after surface selenization. Se source and specimen temperatures for the surface selenization were 200 and 300ºC, respectively

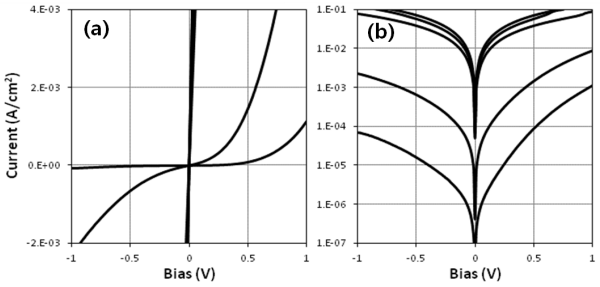

Fig. 3. Dark J-V characteristics of several ZnSe/Zn_3P_2 heterojunctions fabricated using the surface selenization process: (a) Linear J-V and (b) Log J-V

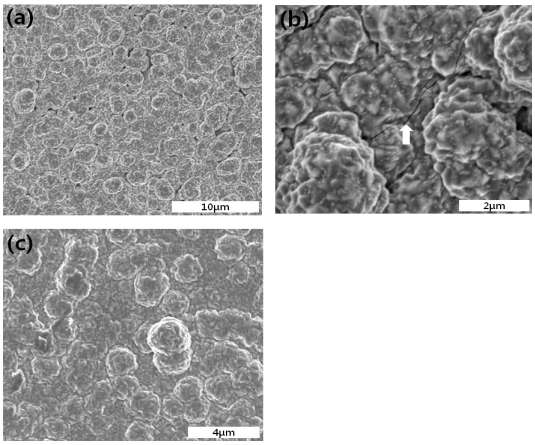

Fig. 4. Surface morphologies of Zn_3P_2 films on ZnTe layer (a) just after Zn_3P_2 film deposition, (b) after surface selenization without $ZnCl_2$ treatment, and (c) after $ZnCl_2$ treatment and surface selenization. The white arrow in (b) denotes a micro-crack

the lattice mismatch between Zn_3P_2 and ZnSe is only 1.0%[13]. The voids and micro-cracks may be the high leakage shunt paths which should be eliminated for better diode characteristics.

To remove the voids, the Zn_3P_2 films were annealed in $ZnCl_2$ vapor before surface selenization. The temperatures of the $ZnCl_2$ (99.999% purity) source and substrate were 200 and 300ºC, respectively. The surface morphology of a sample selenized after $ZnCl_2$ treatment is shown in Fig. 4(c). Neither voids nor micro-cracks are found in Fig. 4(c). The elimination of voids, i.e., densification of the microstructure can be explained by the liquid-assisted grain growth because the melting point of $ZnCl_2$ is around 300ºC[23].

It is necessary to understand the surface selenization process in detail to explain how the surface selenization generates a high density of micro-cracks and how the $ZnCl_2$ treatment suppresses the micro-crack generation in the following selenization process. To study the mechanism, a sample was selenized at 200ºC. The substrate temperature was reduced to retard the redistribution of constituent elements and phase transformation.

Fig. 5 shows the compositional profiles analyzed by XPS. By decreasing the specimen temperature from 300 to 200ºC, the Zn and P profiles were considerably changed. The Zn:Se ratio at the surface is 60:40, i.e., Zn_3Se_2 is formed instead of ZnSe, which inevitably accompanies significant volume expansion because the atomic size of Se is 15% larger than that of phosphorus[24]. It is also notable that the phosphorus concentration beneath the selenized surface region rapidly increased to over 40 atomic percent. This means that phosphorus atoms released by selenization are pushed into the Zn_3P_2 film, which also induces volume expansion. The combined effect of Zn_3Se_2 formation and phosphorus overcharge can induce sufficiently high mechanical stress to initiate and propagate the micro-cracks.

For a sample selenized at 300ºC as shown in Fig. 2, although the Zn:Se ratio in the surface region is apparently about 50:50 and the phosphorus concentration below the transition region is much lower than that shown in Fig. 5, the micro-crack generation can also be explained by the same mechanism in this case: the formation of Zn_3Se_2, buildup of excess phosphorus, and the generation of micro-cracks take place instantly; soon afterward, unstable Zn_3Se_2 transforms to stable ZnSe and the concentration of phosphorus decreases by out-diffusion. The effect of $ZnCl_2$ treatment suppressing the micro-crack generation can be explained with residual $ZnCl_2$ or excess Zn atoms, both of which can react with Se to produce a stable ZnSe phase, which, in turn, decrease the volume of Zn_3Se_2 formed by substitution of P atoms with Se atoms and reduce the amount of released phosphorus.

Several ZnSe/Zn_3P_2 heterojunction solar cells were fabricated by changing the process conditions of the surface selenization with and without the $ZnCl_2$ treatment of Zn_3P_2 layer. Fig. 6 shows the leakage currents of these samples at a 1 V reverse bias. The distribution of leakage current of the cells with the $ZnCl_2$ treatment on Zn_3P_2 layer was much narrower than that without the $ZnCl_2$ treatment. Leakage current values smaller than 10 $\mu A/cm^2$ were obtained in sample group S12 using an optimized surface selenization process. The Se source temperature and specimen temperature of S12 sample group were 250 and 400ºC, respectively. The holding time was 5 min.

Fig. 7 shows the J-V characteristics of the samples in group S12. The reverse bias saturation current, J_o, values are less than 1 $\mu A/cm^2$, but the current values in the forward bias are also very low and the series resistance values derived from dark J-V curves are ~700 $\Omega \cdot cm^2$. This high series resistance is mainly responsible for the low value of J_{sc} (< 0.1 mA/cm^2).

In order to understand the cause of high series resistance,

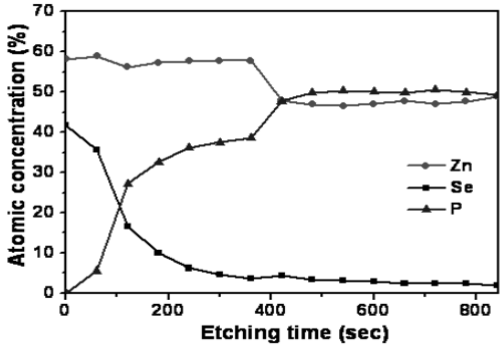

Fig. 5. XPS depth profiles of Zn, Se, and P atomic concentration after surface selenization. Both Se source and specimen temperatures for the selenization were 200ºC

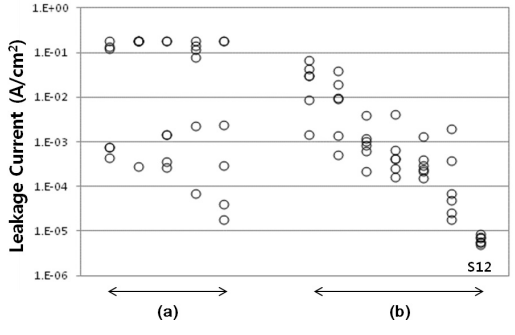

Fig. 6. Leakage currents of several ZnSe/Zn_3P_2 heterojunction solar cells at 1 V reverse bias, prepared (a) without $ZnCl_2$ treatment and (b) with $ZnCl_2$ treatment of Zn_3P_2 layer before selenization

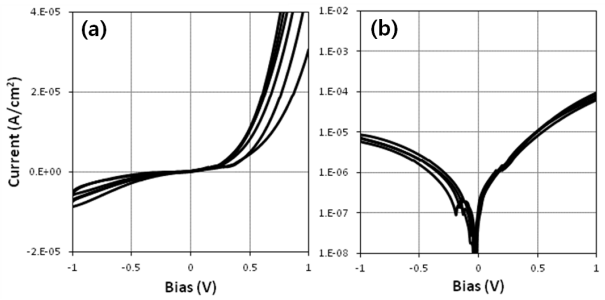

Fig. 7. Dark J-V curves of the ZnSe/Zn_3P_2 heterojunction cells in group S12 shown in Fig. 6

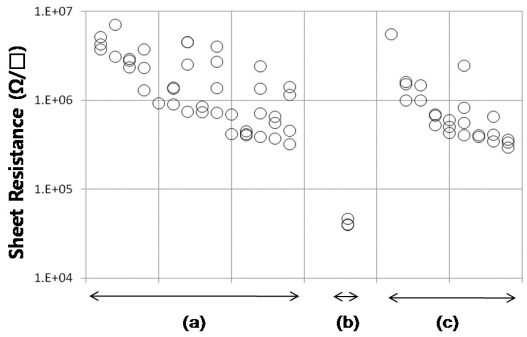

Fig. 8. Sheet resistance values of (a) Zn_3P_2 films, (b) sodium-doped ZnTe films, and (c) stacks of sodium-doped ZnTe/Zn_3P_2. All the films were deposited on soda-lime glass substrates without a Mo layer

resistance values of various parts of the heterojunction were measured. First of all, the contact resistance of sodium-doped ZnTe/Mo was measured by a 2-point probe method. A probe tip with a 0.07 cm^2 area was put into direct contact with the ZnTe surface while the other tip was placed on the Mo surface. The measured value was ~1 Ω·cm^2, which was very small compared with the series resistance of the heterojunction.

To investigate the contribution of the Zn_3P_2 film and ZnTe/Zn_3P_2 interface resistance, several types of films, Zn_3P_2, sodium-doped ZnTe, and Zn_3P_2 on sodium-doped ZnTe, were deposited on soda-lime glass substrates without a Mo layer. The deposition rate on the surface of glass is quite different from that on a Mo surface, particularly, for Zn_3P_2. The source temperature for the Zn_3P_2 films was increased to 650ºC because the deposition rate was too low on the glass substrate at 600ºC. The thickness of Zn_3P_2 films deposited on glass was ~8 μm. Zn_3P_2 films on ZnTe were formed at 600ºC and the films were ~3 μm-thick. The thickness of the ZnTe films was ~2.5 μm.

Fig. 8 shows the sheet resistance values measured with 4-point probes for (a) Zn_3P_2 film, (b) ZnTe film, and (c) stacks of Zn_3P_2/ZnTe film. The sheet resistance of Zn_3P_2 is less than 10^7 Ω/sq, the film resistivity is $<10^4$ Ω·cm, and the contribution to the series resistance is <4 Ω·cm^2, which indicates that the film resistance of Zn_3P_2 is not the main cause of the high series resistance. Especially, under light illumination, the resistivity will be well decreased due to photoconductivity. The sheet resistance of ZnTe is one order lower than that of Zn_3P_2/ZnTe stack. The sheet resistance of ZnTe and Zn_3P_2/ZnTe stack supposed to be similar because of the low resistance of ZnTe layer. The high sheet resistance of the Zn_3P_2/ZnTe stack is possible only when an insulator or a strong barrier is present between the Zn_3P_2 and ZnTe layer. In the case ZnTe should be eliminated.

Recently, Bosco et al. described the experimental results of band alignment measurements on hetero-interfaces composed of n-type II-VI semiconductors grown on a Zn_3P_2 surface[11]. The band offset value of ZnTe/Zn_3P_2 was not reported, but it can be readily calculated because the relative band edge positions of various II-VI compounds are nearly fixed due to self-compensation[25-27]. The energy position of the valence-band maximum of ZnTe is 0.4-0.5 eV lower than that of Zn_3P_2; this makes hole transport from Zn_3P_2 to Mo through the ZnTe layer more difficult. This problem of band alignment may be another cause of low J_{sc}. If this is true, our selection of p+ contact might be not a proper selection.

Further studies are needed to improve the solar cell performance by eliminating p-type ZnTe layer. Our results suggested that it is crucial to reduce the series resistance by making a low resistance back contact. High doping of the Zn_3P_2 layer, at least in the vicinity of the back contact, or use of higher work function contact material might be useful for further improvement.

4. Summary

Thin films of ZnTe and Zn_3P_2 have been successively grown by close-spaced sublimation onto Mo-coated glass substrates. ZnSe layers thinner than 100nm were formed on the surface of Zn_3P_2 films by annealing in Se vapor. Micro-cracks were observed after surface selenization of Zn_3P_2. These micro-cracks and voids provide shunt paths which severely deteriorate the diode characteristics. Annealing the Zn_3P_2 films in a $ZnCl_2$ atmosphere before surface selenization eliminated the voids and prevented the generation of micro-cracks. The mechanism of

micro-crack generation by selenization was described and the suppression effect of $ZnCl_2$ treatment on the micro-crack generation was explained. Using the $ZnCl_2$ treatment and the surface selenization process, ZnSe/Zn_3P_2 heterojunctions with low leakage current ($J_0 < 1\mu A/cm^2$) were fabricated. However, the series resistance was very high due to the presence of an electrical barrier between the ZnTe and Zn_3P_2 layers. To improve the solar cell performance, the series resistance must be reduced by making a low resistance back contact without any hole barrier.

Acknowledgments

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