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Crystallization of Amorphous Silicon Films Using Joule Heating

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Abstract

Joule heat is generated by applying an electric filed to a conductive layer located beneath or above the amorphous silicon film, and is used to raise the temperature of the silicon film to crystallization temperature. An electric field was applied to an indium tin oxide (ITO) conductive layer to induce Joule heating in order to carry out the crystallization of amorphous silicon. Polycrystalline silicon was produced within the range of a millisecond. To investigate the kinetics of Joule-heating induced crystallization (JIC) solid phase crystallization was conducted using amorphous silicon films deposited by plasma enhanced chemical vapor deposition and using tube furnace in nitrogen ambient. Microscopic and macroscopic uniformity of crystallinity of JIC poly-Si was measured to have better uniformity compared to that of poly-Si produced by other methods such as metal induced crystallization and Excimer laser crystallization.

Keywords : Crystallization, Poly-Si, AMOLED, Joule heating

1. Introduction

Active matrix organic light emitting diode (AMOLED) has recently come into the spotlight for its applicability to the next-generation flat panel displays. Since the device operates in a current-driven mode uniform source/drain current is critical for uniform picture quality. Low temperature polycrystalline silicon is thus preferred to a-Si for the thin-film-transistor backplanes. A crystallization technology should produce poly-Si having a uniform grain size over the whole panel especially for AMOLED application. The methods of forming polycrystalline silicon at a low temperature include solid phase crystallization (SPC)[1], metal induced crystallization (MIC)[2], metal induced lateral crystallization (MILC)[3], and Excimer laser crystallization (ELC)[4].

Several attempts have been made to anneal silicon films by applying an electric field during the crystallization of amorphous silicon films. By applying an electric field during MILC, Jun *et al.* attempted to fabricate polycrystalline silicon thin film transistors using field-aided lateral crystallization[5]. Electric field enhanced silicide mediated crystallization has also been reported for low temperature crystallization[6,7]. In such methods, an electric field is applied to an a-Si film which has an ultrathin Ni layer during the crystallization process. Sameshima *et al.* proposed a crystallization method with pulsed electrical current-induced heating of silicon films. In coincidence with the voltage pulse, samples were irradiated with a 28-ns pulsed XeCl excimer laser. The authors reported that the melt duration time of the silicon thin films could be controlled using electrical current intensity in order to obtain large crystalline grain growth[8,9]. They also reported the rapid crystallization of silicon films using Joule heating of metal films[10]. Rapid Joule heating at an intensity of about 1.0 MW/cm^2 was demonstrated by allowing current to flow in chromium metal strips located above a-Si films. This particular method involved the achievement of crystallization by melting silicon films.

We previously reported a crystallization method named as Joule heating induced crystallization (JIC)[11]. In this technique, Joule heat is generated by applying an electric filed to a conductive layer located beneath or above the amorphous silicon film, and is used to raise the temperature of the silicon film to crystallization

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temperature. For the crystallization of a-Si films to occur, the Joule heat generated must be used mainly in raising the temperature of the film to its crystallization temperature. Thus, an electric field should be applied to the conductive layer for a very short time in order to generate intense pulses of energy which are conducted to the film, therefore minimizing the heating of glass substrate. As the Joule heat is generated uniformly throughout the conductive layer, the temperature of the film can be regarded as being more uniform than that achieved using other conventional heating methods. Crystallization is accomplished within the range of a millisecond. In this work we investigated crystallization kinetics of JIC and crystalline uniformity of JIC poly-Si.

2. Experimental Procedure

Schematic diagram for the JIC process is shown in Fig. 1, where an electric pulse is imposed on the specimen with ammeter and voltmeter for in-situ measurements. Fig. 1 shows an instance in which a conductive layer is located beneath the amorphous silicon films. A conductive layer such as Mo, Cr, or indium tin oxide (ITO) and a SiO_2 dielectric layer are successively formed on the dielectric layer produced on the glass substrate, which is then followed by the formation of an amorphous silicon thin film thereon.

Using the plasma enhanced chemical vapor deposition (PECVD) method, a SiO_2 layer (first dielectric layer) with a thickness of 300 nm was formed on a 0.7 mm-thick glass substrate. An ITO thin film (conductive layer) having a thickness of 70 nm was deposited on the first dielectric layer by sputtering, and then a SiO_2 layer (second dielectric layer) having a thickness

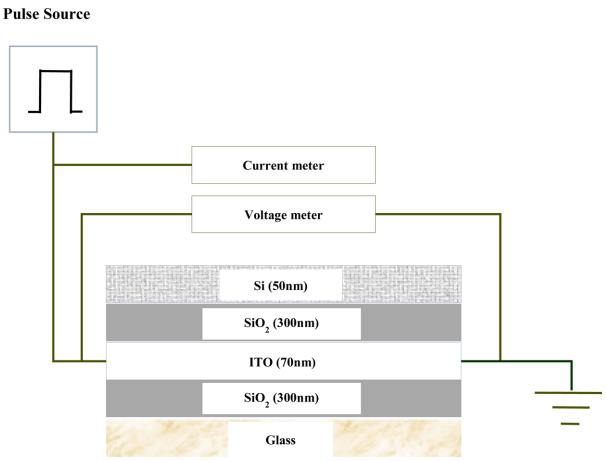


Fig. 1. Schematic diagram of experimental setup for Joule-heating induced crystallization.

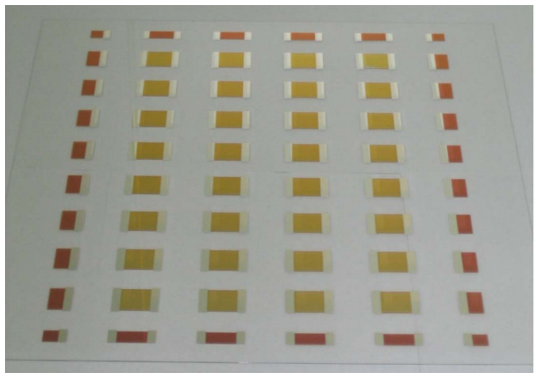


Fig. 2. Small-sized (20 mm × 20 mm) JIC crystallized samples on the 2nd generation glass substrate.

of 500 nm was deposited thereon using the PECVD method. The PECVD method also resulted in an amorphous silicon thin film having a thickness of 50 nm being deposited on the second dielectric layer. Thus, an array, including the amorphous silicon thin film shown in Fig. 1, was prepared. Fig. 2 shows small-sized crystallized samples using JIC method on the 2nd generation glass substrate (Corning Eagle 2000[12]). Overall dimensional size of each specimen was 20×30 mm^2, where the crystallization window and each electrode at both sides were 20×20 mm^2 and 5×20 mm^2, respectively.

The sheet resistance of the ITO conductive layer was measured to be 30 Ω/□. An electric field was applied to an ITO film within the range of a millisecond for crystallization. The microstructure of crystallized films was determined by transmission electron microscopy (TEM). Macroscopic uniformity of crystallinity of JIC poly-Si samples was measured using Raman spectroscopy and was compared to that of poly-Si produced by the methods of MIC and ELC, respectively. A Jasco-NR110 Raman system was used at room temperature with the 514.5 nm line from an Ar ion laser. Raman shift was measured between 350 cm^{-1} and 650 cm^{-1}. Broad peak of a-Si was observed at 480 cm^{-1} while crystalline Si exhibited a sharp peak at 520 cm^{-1}.

3. Results and Discussion

Two main factors whether crystallization occurs or not using a JIC process are power density (W/cm^2) and pulsing time, respectively. Power density affects the heating rate during the period of electrical pulsing. Raman spectroscopy was employed to check if crystallization occurred according to processing conditions of power density and pulsing time. When an electric

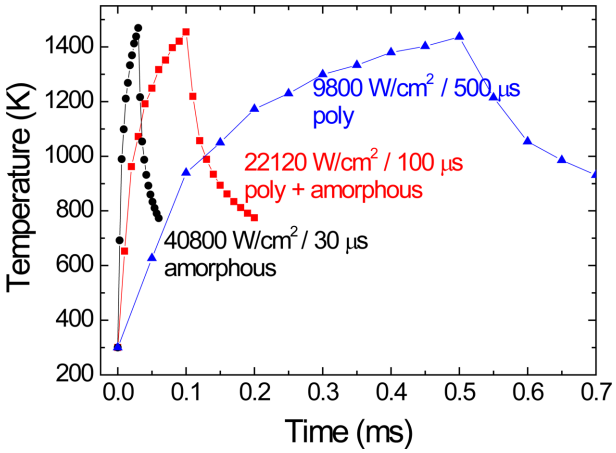


Fig. 3. The simulated temperature profile according to the processing conditions of the power density and the pulsing time.

field was applied with the power density of 40800 W/cm^2 for 30 μs, crystallization was not observed to occur. The 100 μs pulse with the power density of 22120 W/cm^2 resulted in partial crystallization. Meanwhile, complete crystallization was observed with the power density of 9800 W/cm^2 for 500 μs. Fig. 3 indicates the simulated temperature profile under these three different processing conditions. Each thin film in the specimen had no patterned features and Joule heat was assumed to be generated uniformly in the ITO thin film. Furthermore, the major process time was about tens or hundreds of microseconds. Thus the convective and radiation heat transfer was assumed to be negligible. Based on this approximation, the temperature of the film could be estimated by the one-dimensional heat conduction model, given by

$$\frac{\partial \rho C T}{\partial t} = \frac{\partial}{\partial x}\left(K\frac{\partial T}{\partial x}\right) + S \quad (1)$$

$$S = I\,V / A h_{ITO} \quad (2)$$

Where ρ, C, K are density, specific heat, and thermal conductivity, respectively, for each layer and S denotes volumetric Joule heat generation rate only in the ITO film. Here, a time-dependent input pulse of current, I, and voltage, V, was imposed on the specimen of process window area, A, and ITO film of thickness, h_{ITO}. The finite difference form of the heat conduction equation was solved by the Crank-Nicolson method. As the power density increases the heating rate increases as demonstrated in Fig. 3. Joule heating under each three condition causes almost the same peak temperature of the film to rise above 1400 K. However, the duration above a critical temperature during the period of heating (during electrical pulsing) and cooling (after electrical pulsing) is different according to processing parameters, which affects the crystallization kinetics.

In order to investigate the temperature dependence of the crystallization kinetics, we conducted SPC experiments using silicon wafers that had the structure of a 50 nm-thick PECVD a-Si / 500 nm-thick SiO_2 / silicon wafer. Solid phase crystallization was conducted using a tube furnace in nitrogen ambient at temperatures ranging from 600°C to 1000°C. Crystallization kinetics was checked as a function of annealing temperature and time using Raman spectroscopy. While the crystallization process was completed in 20 hrs at 600°C,

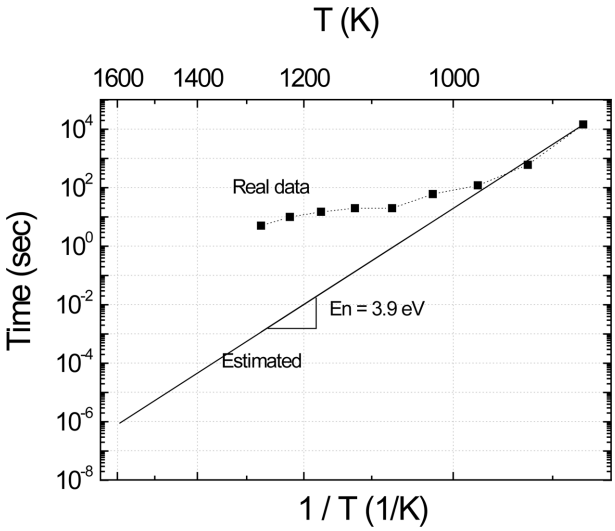
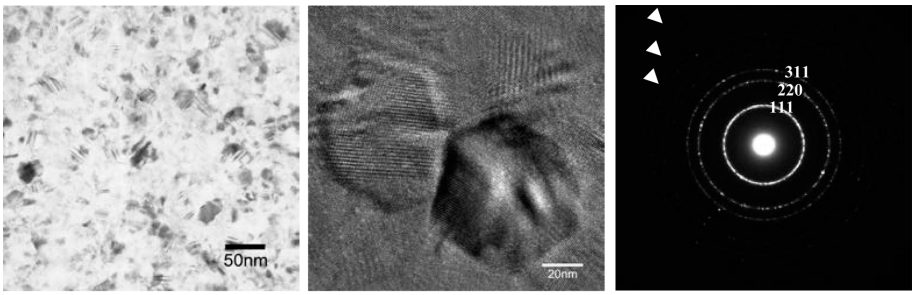


Fig. 4. Arrhenius plot of the measured incubation time. Notice that the measured data does not fit to straight line. The estimated straight line was obtained using the measured data at low temperatures and using the value of nucleation activation energy of 3.9 eV.

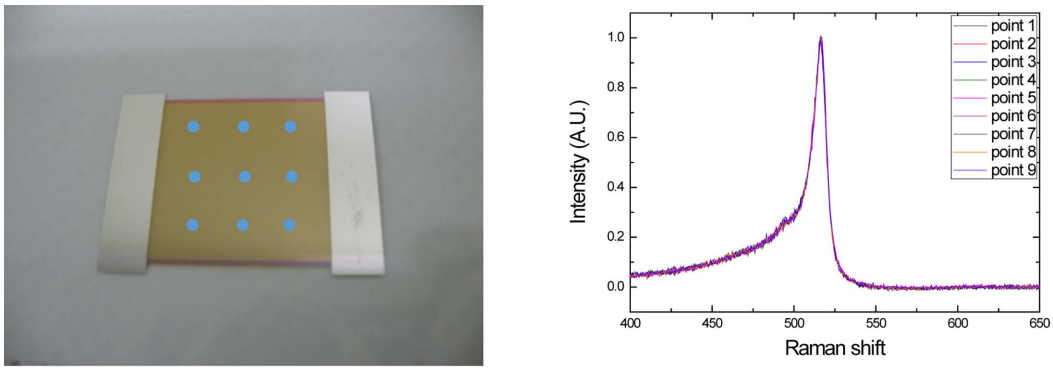
Table 1. Measured and estimated incubation time vs. crystallization temperatures

	Measured incubation time	Estimated incubation time
600°C	~ 4 hrs	4 hrs
700°C	< 2 min	1.16 min
800°C	< 20 sec	912 ms
900°C	< 15 sec	25.01 ms
1000°C	< 5 sec	1.2 ms
1050°C	N/A	314.5 μs
1100°C	N/A	90.5 μs
1150°C	N/A	28.4 μs
1200°C	N/A	9.64 μs
1250°C	N/A	3.52 μs
1300°C	N/A	1.37 μs



(a) (b) (c)

Fig. 5. (a) Bright filed TEM bright-field micrograph, (b) high resolution TEM micrograph, and (c) TED pattern of the JIC poly-Si crystallized at room temperature in an electric field of 800 V/cm for 320 μs.



(a) (b)

Fig. 6. (a) JIC poly-Si sample (20 mm × 20 mm) showing 9 spots where Raman spectroscopy was conducted, (b) Raman spectra of JIC poly-Si analyzed from 9 different locations.

it was over in 25 s at 1000°C. Since SPC kinetics is controlled by the nucleation rate, and the activation energy needed to nucleate silicon crystals has a high value of 3.9 eV[13], the crystallization rate is significantly increased when the crystallization temperature is raised. Moreover, in the case of furnace annealing, the sample was found to be unable to reach the setting temperature of 1000°C within 25 s. Fig. 4 indicates an Arrhenius plot of an incubation time. The dotted line represents the measured data while the solid straight line denotes the estimated data using the nucleation activation energy of 3.9 eV with the measured data under 600°C. The measured and estimated incubation time are summarized in Table 1 at crystallization temperatures ranging from 600°C to 1300°C. It can be seen that the estimated incubation time indeed becomes less than 1 ms at temperatures above 1000°C. As indicated in Fig. 4 the incubation time at 1400 K is estimated to be around 36 μs, which may explain the experimental results as shown in Fig. 3.

Fig. 5(a) and Fig. 5(b) show a TEM bright field micrograph and high resolution TEM micrograph, and Fig. 5(c) shows the transmission electron diffraction (TED) pattern of the JIC poly-Si. The a-Si film is fully crystallized at room temperature in an electric field of 800 V/cm for 320 μs. The radii of the TED patterns shown in Fig. 5(c) for the JIC poly-Si have been indexed and found to correspond to the interplanar spacing of silicon. The grains are preferentially oriented with the (111), (220) and (311) directions according to the TED patterns. The microstructure of the poly-crystalline silicon thin film exhibits a nano-crystalline phase. The polycrystalline silicon produced has a very small grain size of ~30 nm and exhibits grains of equiaxed morphology uniformly distributed in terms of the grain size as can be seen in Fig. 5(b). Such a microstructure cannot be obtained by solid state trans-formation using conventional heat-treatment methods since crystallization is completed during the period of heating-up. In order to check the macroscopic crystalline-uniformity Raman spectroscopy[14] was conducted on the 9 spots in the JIC poly-Si sample having dimension of 20 × 20 mm^2 as demonstrated in Fig. 6(a). Fig. 6(b) shows Raman spectra measured at 9 different locations.

Crystalline non-uniformity of JIC poly-Si was measured to be ~1.1% while ELC poly-Si was measured to have crystalline non-uniformity of ~2.3% and ~7.2% for MIC poly-Si. Thus, the macroscopic uniformity of the grain size of the JIC poly-Si was found to be excellent in addition to the microscopic one.

4. Conclusions

This study demonstrated the possibility of achieving the microsecond crystallization of amorphous Si thin film via Joule heating. Such a process does not make use of any metallic element for preferential nucleation, and is completed within a millisecond at room temperature. Poly-Si films featuring nano-crystalline sized grains were obtained by the present crystallization method. Crystalline non-uniformity of JIC poly-Si was measured to be ~1.1% while ELC poly-Si was measured to have crystalline non-uniformity of ~2.3% and ~7.2% for MIC poly-Si. As microscopic and the macroscopic uniformity of the grain size of the JIC poly-Si film is excellent, this process is expected to find its applications, especially with regards to AMOLED. In order to apply JIC method in mass production line where large-sized glass substrate is used thickness uniformity of a conductive layer should be improved.

Acknowledgments

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References

1. A. T. Voutsas, M. K. Hatalis, J. Electrochem. Soc., 139 (1992) 2659.
2. R. S. Wagner, W. C. Ellis, Appl. Phys. Lett., 4 (1964) 89.
3. S.-W. Lee, S.-K. Joo, IEEE Electron Dev. Lett., 17 (1996) 160.
4. J. S. Im, H. J. Kim, M. O. Thompson, Appl. Phys. Lett., 63 (1993) 2969.
5. S.-I Jun, Y.-H. Yang, J.-B. Lee, D.-K. Choi, Appl. Phys. Lett., 75 (1999) 2235.
6. J. Jang, J. Y. Oh, S. K. Kim, Y. J. Choi, S. Y. Yoon, C. O. Kim, Nature, 395 (1998) 481.
7. S. Y. Yoon, J. Y. Oh, C. O. Kim, J. Jang, J. Appl. Phys., 84 (1998) 6463.
8. T. Sameshima, K. Ozaki, N. Andoh, Appl. Phys., A 71 (2000) 1.
9. T. Sameshima, N. Andoh, H. Takahashi, J. Appl. Phys., 89 (2001) 5362.
10. T. Sameshima, Y. Kaneko, N. Andoh, Appl. Phys., A 73 (2001) 419.
11. J.-S. Ro, W.-E. Hong, SID Digest of Technical Papers (2006) 1280.
12. Samsung Corning Precision Glass Inc., www.samsungscp.co.kr.
13. I.-W. Wu, A. Chiang, M. Fuse, L. Öveçoglu, T. Y. Huang, J. Apply. Phys., 65 (1989) 4036.
14. W.-E. Hong, J.-S. Ro, J. Appl. Phys., 114 (2013) 073511.