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High Efficiency Buck-Converter with Short Circuit Protection

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** Short Paper*

** Invited Paper: None*

** Review Paper: This paper reviews the recent progress possibly including previous works in a particular research topic, and has been accepted by the editorial board through the regular reviewing process.*

** Extended from a Conference: Preliminary results of this paper were presented at the IEEE VTC Fall 2012. This present paper has been accepted by the editorial board through the regular reviewing process that confirms the original contribution.*

***Abstract*:** This paper proposes a DC-DC Buck-Converter with DT-CMOS (Dynamic Threshold-voltage MOSFET) Switch. The proposed circuit was evaluated and compared with a CMOS switch by both the circuit and device simulations. The DT-CMOS switch reduced the output ripple and the conduction loss through a low on-resistance. Overall, the proposed circuit showed excellent performance efficiency compared to the converter with conventional CMOS switch. The proposed circuit has switching frequency of 1.2MHz, 3.3V input voltage, 2.5V output voltage, and maximum current of 100mA. In addition, this paper proposes a SCP (Short Circuit Protection) circuit to ensure reliability.

***Keywords*:** DT-CMOS, DC-DC, SCP, Buck-converter, PMIC

1. Introduction

These days, the importance of power management IC(PMIC) has been emphasized for battery-powered portable electronics, such as tablets and mobile phones. For miniaturization and high efficiency, the power supply of these devices is replaced with Linear-type with SMPS-type. SMPS (Switching Mode Power Supply) can increase the switching frequency to reduce the size of the energy storage element. On the other hand, the switching operation at high frequency causes switching losses, inductor losses and conduction losses.

2. Dynamic Threshold-Voltage CMOS

Switching loss is a fixed cause, but conduction loss by the on-resistance of a switch increased with increasing output current. When the output current was increased, the conduction loss increased more than the switching loss in high output current, as shown in Fig. 1.

Dynamic Threshold voltage MOSFET (DT-CMOS) was designed using a SOI wafer, as shown in Fig. 2 [1, 2].

When the switch was ON after connecting the gate and p-substrate, a heighten body voltage occurred, which reduced the threshold voltage. When the switch was OFF, the body was connected to the ground, which increased the threshold voltage.

Fig. 3 shows the DT-CMOS proposed in this paper. When the proposed DT-CMOS switch was turned-on, the threshold voltage was lowered by the NMOS connected to the diode. Therefore, when the proposed switch was turned on, it has a lower threshold voltage than the standard switch. When the switch was OFF, the body of the PMOS and NMOS was connected to the power supply and the ground, respectively. Therefore, the limitation of power supply voltage by the leakage current is overcome by minimizing the body leakage current, which is a

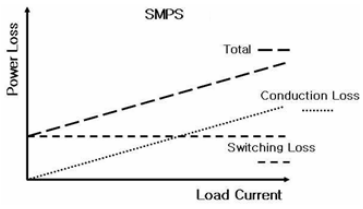

Fig. 1. Power loss analysis SMPS.

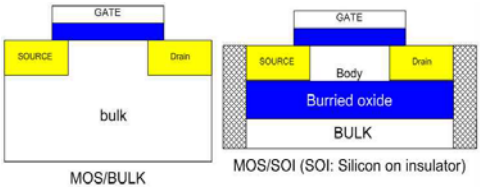

Fig. 2. CMOS & DT-CMOS.

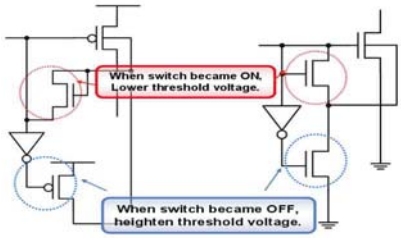

Fig. 3. Proposed DT-CMOS.

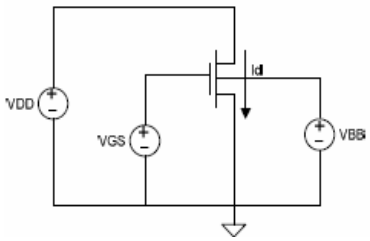

Fig. 4. Switching characteristic simulation circuit.

conventional DT-CMOS fault when deciding the supply and the ground [3, 4].

Fig. 4 shows the switching characteristic simulation circuit. This circuit simulates the DT-CMOS and CMOS switching characteristics.

Figs. 5 and 6 present the switching characteristics. In this paper, the threshold voltage and I-V characteristics of DT-CMOS with CMOS are compared. When the VDD was a 3.3V input voltage, the threshold voltage simulation was performed by increasing the VGS. The simulation was performed to compare the I-V characteristics using the CMOS and DT-CMOS with the same W/L ratio. As shown in Fig. 5, DT-CMOS has a lower threshold voltage than CMOS. Fig. 6 presents the I-V characteristics as a function of Vds.

In this study, the DT-CMOS was designed with Deep-Nwell isolation from the substrate and body to a conventional silicon wafer, as shown in Fig. 7. One-chip of the switching device and PWM control circuit were designed using this technique.

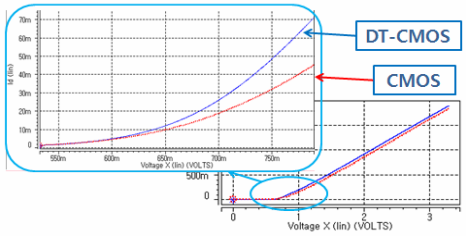

Fig. 5. Comparison of the threshold-voltage.

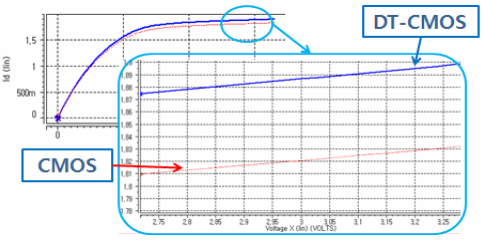

Fig. 6. Comparison of the I-V characteristics.

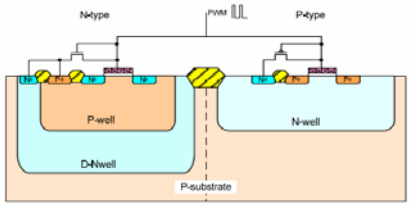

Fig. 7. Cross section of the proposed DT-CMOS.

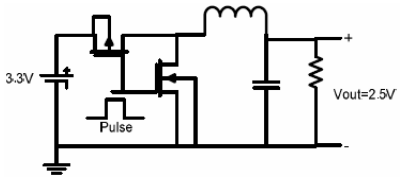

Fig. 8. DT-CMOS & CMOS circuit for efficiency.

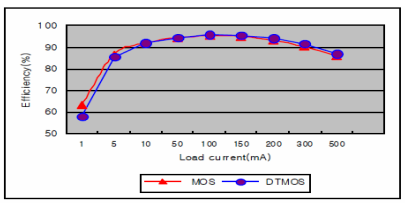

Fig. 9. DT-CMOS & CMOS efficiency as a function of the load current.

DT-CMOS was compared with CMOS in a simulation. Fig. 8 showed the designed simulation circuit.

The load current was changed and the efficiency for DT-CMOS and CMOS was compared. When the load current was changed from a minimum 0.1mA to a maximum 300mA, the efficiency of CMOS was higher until 10mA. In contrast, the efficiency of DT-CMOS was higher from 50mA as shown in Fig. 9.

When the output current of the DC-DC converter was based on 100mA, the efficiency of CMOS was 96.25%,

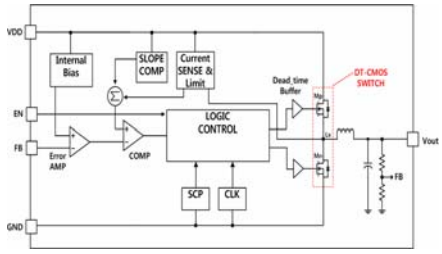

Fig. 10. Function Block diagram.

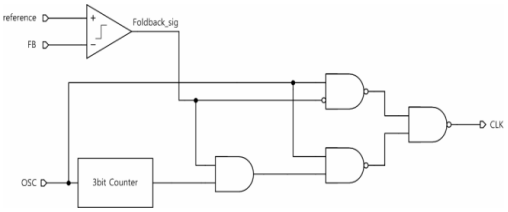

Fig. 11. SCP(Short Circuit Protection) circuit.

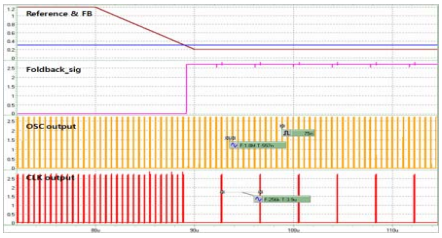

Fig. 12. Result of the SCP circuit simulation.

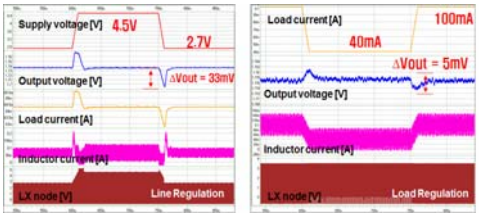

Fig. 13. Result of line / load transient response.

but the efficiency of DT-CMOS was 97%. If the efficiency of CMOS is 97%, the size of CMOS will double.

3. The Design of Proposed DC-DC Converter

Fig. 10 presents a function block diagram of the proposed buck-converter. The proposed converter operates in PWM mode. The PWM waveform was applied to the gate of the DT-CMOS switch, and the ON-OFF of switch was determined. Therefore, the output voltage is formed. The feedback voltage formed by the voltage divider was compared to a reference voltage using an error amplifier. The comparator generates a pulse by comparing the saw tooth wave and error factor. The pulses generated by the comparator generate a pulse, which is applied to the NMOS switch and PMOS switch via the logic controller. [5-7].

4. SCP(Short Circuit Protection)

Fig. 11 shows a block diagram of the SCP (Short circuit protection). When the clock signal is applied to the terminals of the OSC in the SCP, CLK terminal is maintained or the frequency of the conventional clock frequency through SCP decreases according to the output (Foldback_sig) obtained from a comparison of the feedback voltage and the reference voltage of the converter output. If the output terminals of the Foldback_sig are low, an output short circuit does not occur. Therefore, the waveform of the OSC terminal appears intact in the output terminals CLK. In contrast, when the feedback voltage applied to the fb terminals, if fb is lower than the reference voltage, it detecting the output short circuit phenomenon. At that time, the output from the 3-bit counter in the OSC terminal to CLK terminal appear to reduce the clock frequency. To prevent this phenomenon, If the output voltage falls below the set voltage, which decreases the frequency of the clock. As a result, it is possible to prevent the phenomenon of the inductor current runway and reduce the power consumption.

5. Simulation Result

Fig. 12 presents the simulation results of SCP. The feedback voltage was compared with a reference voltage of 0.3V to determine the operation SCP. The feedback voltage will have the same value as that of the bandgap reference voltage of 1.2V due to the virtual short circuit phenomenon between the bandgap reference and feedback voltage.

During normal operation, the feedback voltage has a greater voltage than the reference voltage of 0.3V. Then, Foldback_sig has a low voltage. As a result, the OSC generated by ring oscillator circuit appears on the CLK port.

In contrast, when the feedback voltage is lower than the reference voltage of 0.3V. Then, Foldback_sig has a high voltage. As a result, the SCP output frequency(CLK) is reduced by a 3-bit counter in the SCP**.**

The clock frequency by the SCP is approximately 256kHz, and width is the same at 75ns.

Fig. 13 presents the results of line / load transient response simulation. For line transient response, when input voltage is changed from 2.7V to 4.5V, the output has a ripple voltage of 33mV. For the load transient response, when the load current is changed from 100mA to 40mA, The output has a ripple voltage of 6mV.

Low side switch is ON after the high side switches OFF and then low side switch is OFF before the high side switch ON for stable operation. This is illustrated in Fig. 14.

The PWM DC-DC converter (Fig. 150 was designed using the PWM control circuit designed previously. The performance of the DC-DC converter is a 3.3V input voltage, a 1.4V output voltage, maximum output current

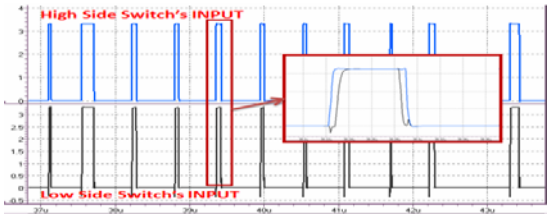

Fig. 14. Simulation result of switch's input wave.

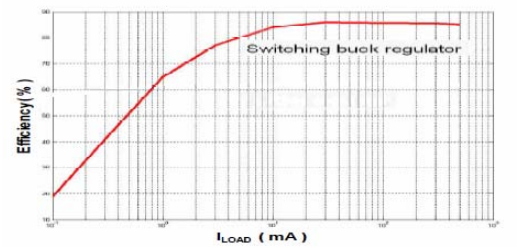

Fig. 15. Efficiency of SMPS.

100mA, a 1.2MHz switching frequency, maximum efficiency of 95%, and a 12mV ripple voltage. The efficiency of DT-CMOS was improved 0.5% compared to CMOS in the simulation result.

6. Conclusion

The DC-DC Converter with DT-CMOS switch. DT-CMOS switch reduces the output ripple and the conduction loss through a low on-resistance. Therefore, the proposed Buck-converter has excellent performance efficiency compared to the converter with a conventional CMOS switch. In addition, the proposed IC was protected from short circuits using a SCP.

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