A Scan-Based On-Line Aging Monitoring Scheme

Hyunbean Yi[1], Tomokazu Yoneda[2], and Michiko Inoue[2]

Abstract—**In highly reliable and durable systems, failures due to aging might result in catastrophes. Aging monitoring techniques to prevent catastrophes by predicting such a failure are required. This paper presents a scan-based on-line aging monitoring scheme which monitors aging during normal operation and gives an alarm if aging is detected so that the system users take action before a failure occurs. We illustrate our modified scan chain architecture and aging monitoring control method. Experimental results show our simulation results to verify the functions of the proposed scheme.**

Index Terms—**Aging monitor, scan test, delay test, on-line test, system-on-chip (SoC)**

I. INTRODUCTION

Transistor aging has been a major concern. It is well known that, with time, transistor performance degrades due to failure mechanisms such as negative/positive Bias temperature instability (NBTI/PBTI), Hot Carrier Injection (HCI), and Time Dependent Dielectric Breakdown (TDDB). In the latest CMOS process technology, most dominant failure mechanism is NBTI which causes slow delay degradation and finally a failure can occur [1-4]. In applications requiring high field reliability such as medical equipment, satellites, aircrafts, and power plants, performance degradation and a failure can trigger life-threatening disasters. In order to prevent a disaster, aging monitoring techniques have been presented [5-12]. They give a warning to the system user or conduct self-repair before a failure occurs. As a way to monitor performance degradation, delay test techniques can be used. However, a conventional at-speed delay test may not be used because performance degradation must be sensed before a failure occurs. Besides, the delay test operation must be performed in field over system lifetime. Therefore, an on-line self-delay-test scheme using a faster clock than the functional clock is required.

In this paper, we propose a scan-based on-line aging monitoring scheme which can monitor aging during normal operation. We propose a modified scan-chain architecture using a duty cycle adjustable clock generator. Section II illustrates our proposed aging monitoring scheme and Section III shows experimental results. In Section IV, we conclude the paper.

II. RELATED WORKS

As an on-line self-test architecture, Y. Li et al. [5] introduced the concurrent autonomous chip self-test using stored test patterns (CASP) which performs on-line testing using the test patterns pre-stored in a non-volatile memory in the system. Y. Sato et al. [6] presented a circuit failure prediction mechanism named DART which stands for *D*egrade factor, *A*ccuracy, *R*eport, and *T*est Coverage. They also use pre-stored test patterns and refer to the measured voltage and temperature, which are uncontrollable in field but affect delay variation, to improve the delay measurement accuracy. The architectures utilize core idle time or power-on/-off time as test mode and apply scan-based delay test with faster-than-at-speed clocks. In case where an SoC has to

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continuously work without stopping (power-off), a core test scheduling method which selects a core to be tested is needed because all cores cannot be in test mode. A simple static round-robin scheduling method cannot give cores many chances of test because the scheduler simply waits until the next core becomes idle. Therefore, H. Inoue et al. [7] and Y. Li et al. [8] respectively applied Virtualization-Assisted concurrent autonomous Self-Test (VAST) and CASP-aware OS scheduling which are higher-level on-line scheduling support techniques. They took the unavailability of cores into consideration, thereby attempting to test each core as often as they can as well as minimizing the impact on application performance. H. Yi et al. [9] presented a degree-of-aging-based weighted test scheduling scheme. By testing the more aged cores more often, they reduce the possibility to miss a system failure. However, the on-line test scheduling schemes cannot help resulting in performance loss because schedulers has to schedule normal and test operations at the same time and interface with the processors or OS to have cores enter test mode and recovered. Furthermore, some cores such as processor cores may not be in idle state during normal operation and cannot be tested even during power-on/-off time if power-on/-off time is not long enough.

In order to predict timing errors on actual data paths during normal operation, D. Ernst et al. (Razor flip-flop) [10], T. Sato and Y. Kunitake (Canary flip-flop) [11], M. Agarwal et al. (Aging Sensor flip-flop) [12], T. Nakura et al. (delay prediction flip-flop, DPFF) [13], and J. Park and J. A. Abraham (Aging Aware FF) [14] proposed modified flip-flops. Each of them uses two flip-flops (or a flip-flop and a latch), one to capture the normal data and the other one to capture the delayed data, and checks if timing constraints are met. In order to capture the delayed data, Razor flip-flop [10] and Aging Aware FF [14] use a delayed clock and the others [11-13] put a delay element. Therefore, the area overhead due to the delayed clock circuits or the delay elements is very high.

III. Proposed Scan-Based On-Line Aging Monitoring Scheme

The existing aging monitoring techniques designed their own clock generator or adopted an on-chip test clock generator to perform a faster-than-at-speed delay test. In order to decide the frequency of a faster test clock, guard-band interval is used. The guard-band interval, as shown in Fig. 2, is the timing guard-band given to account for expected performance loss over device lifetime. Traditionally, 10-20% frequency guard-bands have been used. For example, devices that operate at 3 GHz during testing may come out to the market as devices operating at 2.7 GHz [15].

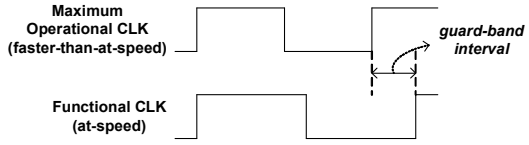

Fig. 1. Guard-band interval.

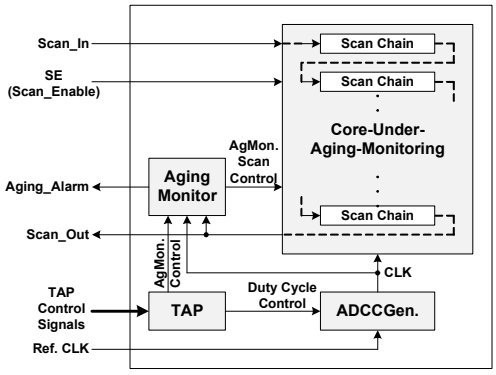

Fig. 2. A simple device with a core and aging monitoring circuits.

1. Overview

Fig. 2 shows the overall architecture of a device with a core and aging monitoring circuits. The core has a scan chain and operates at the core functional clock (CLK) generated from the Adjustable Duty Cycle Clock Generator (ADCCG) [16, 17]. The Aging Monitor periodically checks aging and when an aging is detected, it gives out the alarm signal, Aging_Alarm. Through the TAP, the duty cycle and the Aging Monitor (AgMon.) control information are set. The control information may be fixed before the device goes to the market or may be reset on board in the system where the device is installed. Our main goal is to perform this aging monitoring during normal operation without stopping the core. The basic idea for the goal is to insert another scan chain which captures functional data within a given guard-band interval during normal operation and to compare the

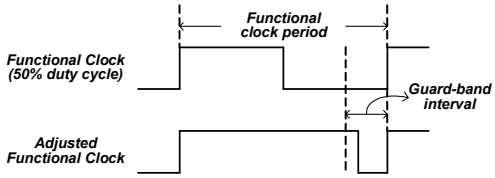

Fig. 3. Adjusted functional clock.

early captured data in the additional scan chain with the normally loaded data in the original scan chain. Then, the next problem is how to generate the early capture clock while keeping the normal operating speed of the core. If using a separate clock for the early capture operation is allowed, it would be functionally easy to implement.

However, it will make physical implementation much more difficult because the early capture clock faster than the functional clock may create clock and scan control signal skew problems. Therefore, in order to embody our idea without inserting another clock, assuming that the core-under-aging-monitoring is rising edge triggered, we i) adjust the duty cycle of the functional clock so that the falling edge can be located within the guard-band interval and ii) modify the scan architecture so that the additional scan chain captures the functional data at the falling edge.

Fig. 3 shows the adjusted functional clock to be used in our aging monitoring scheme. The duty cycle of the adjusted functional clock has to be determined so that the falling edge occurs within the given guard-band interval. The guard-band interval and the duty cycle are decided considering the aging prediction model used in the device manufacturing process and variations of environmental conditions such as voltage and temperature [9].

2. Modified Scan Chain Architecture

The detailed architecture of the proposed scan chain including the early scan cell architecture is shown in Fig. 4. There are two scan chains which are the normal scan chain consisting of the series of scan cells (SCs) and the early capture scan chain consisting of the series of the early capture scan cells (ECSCs). When the core runs, the input data (DI) is continuously captured in the early capture flip-flop (ECFF) at falling edges and loaded in the data flip-flop (DFF) at rising edges. The two values in the DFF and the ECFF are compared using the XOR

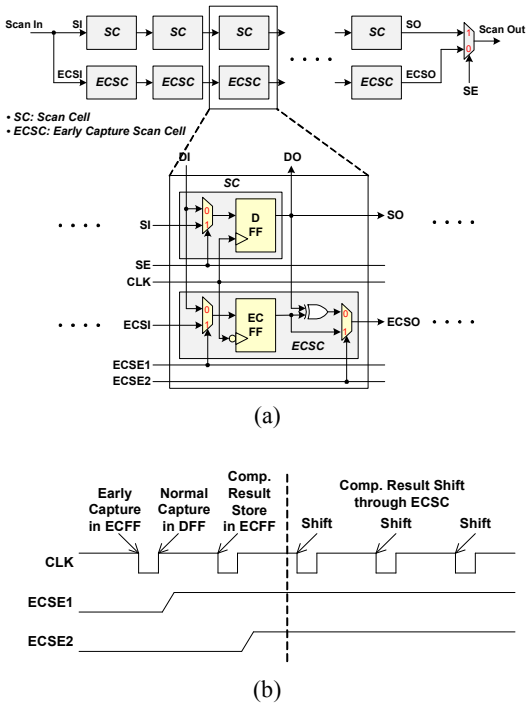

Fig. 4. Modified Scan Chain Architecture (a) Early capture scan chain and cell, (b) Timing diagram of ECSC operation.

gate. There are two early capture scan enable signals, ECSE1 and ECSE2. When the ECSE1 goes to '1' after a rising edge, the comparison result is captured at the following falling edge in the next ECFF. And then, if the ECSE2 goes to '1' after the falling edge, the captured comparison results are shifted out. The Aging Monitor checks the shifted values. If '1' is observed during the shift operation in the early capture scan chain, it gives the aging warning signal, Aging_Alarm. In this way, without stopping cores, the aging monitoring operations can be concurrently performed during normal operation.

3. Aging Monitor

When an aging monitoring session starts, the Aging Monitor controls the early capture scan chain to capture functional data earlier and observe the comparison results. When the early-capture-scan-shift operation is over, the observation is finished and an aging monitoring session ends. Fig. 5(a) shows the block diagram of our Aging Monitor. Through TAP, a time interval between sessions is programmed. Fig. 5(b) show state diagram for the EC/AG. Once the Programmable Interval Timer (PIT) reaches the programmed interval time, the ECS Controller/Alarm

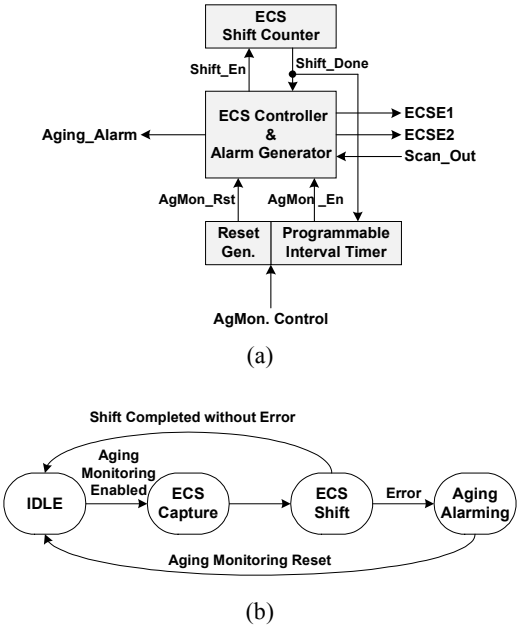

Fig. 5. Aging Monitor Architecture (a) Block Diagram of Aging Monitor, (b) State Diagram for ECS Controller/Alarm Generator.

Generator (EC/AG) is enabled (AgMon_En = '1' for one clock cycle). Then, the EC/AG timely generates the signals, ECSE1 at the "ECS Capture" state and ECSE2 at the "ECS Shift" state, enables the ESC Shift Counter, and observes if there is an error coming out through the Scan_Out until the Counter is over (Shift_Done = '1'). If no error was observed during ECS shift operation the "ECS Shift" state, the EC/AG does not alarm and waits for the next session at the "IDLE" state. But, if an error once was observed (Scan_Out = '1'), the aging warning signal is given out (Aging_Alarm = '1') at the "Aging Alarming"

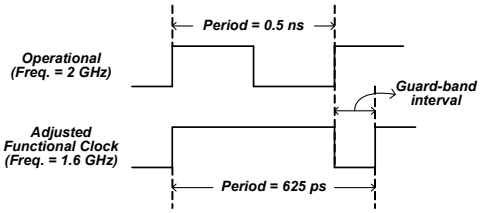

Fig. 6. Adjusted functional clock for simulation.

state.

When an aging is detected, the system users must take immediate action. If there is a backup system or device available, even though it is very costly, it could be the best way to replace it as soon as possible. Otherwise, they may be able to prolong the device life time by running a self-repair mechanism or strengthen the monitoring by increasing the clock duty cycle and reducing the session period (the interval time in the PIT). How to take action against the aging alarming is out of the scope of this paper.

VI. EXPERIMENTAL RESULTS

In order to conduct simulations, we designed an 8-bit scan chain and the proposed early capture scan chain and generated the 8-bit data coming into the scan chain (output of a combinational logic). We assumed that a device operates at 2 GHz during testing and the 20% frequency guard-band is used. Then the functional clock frequency becomes 1.6 GHz and the adjusted functional clock is generated as shown in Fig. 6. Fig. 7 shows our simulation result. In order to verify the functions of the

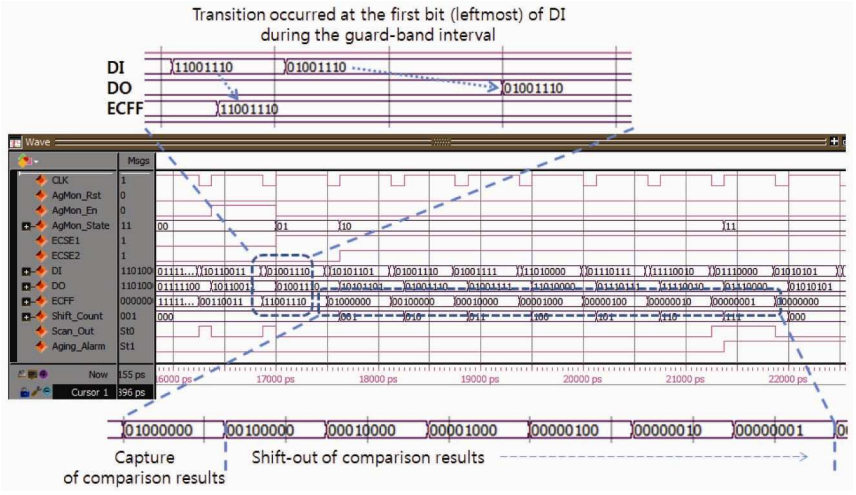

Fig. 7. Simulation result of a case where aging occurs on a data path.

proposed ECSC, we present the case where there is aging on a data path. We added delay on the first (leftmost) data input signal as if aging occurred. As shown in the left dotted box, the first bit is transited (11001110 => 01001110) during the guard-band interval, "11001110" is captured in the ECSC at the falling edge of the adjusted functional clock, and "01001110" is captured in the scan chain (DO) at the rising edge of the adjusted functional clock. When ECSE1 = 1 and ECSE = 1, the comparison results are captured in the next early capture cells and shifted. Therefore, the first 8 bits in the right dotted box became "01000000" which means aging is detected on the first data input signal. As a result, '1' is shifted out and the Aging Monitor asserted the Aging_Alarm signal.

Table 1 shows a comparison of cells in terms of additional logic and area. In order to compare the existing cells with our proposed ECSC, we assumed that scan chain is inserted and figured out the additional parts except for the basic scan cell (= 1 MUX and 1 FF). All of the cells basically include a flip-flop (or latch) and an XOR gate as shown in the Additional Logic column. In order to capture delayed data, Canary FF [11], Aging Sensor FF [12], and DPFF [13] put a delay element on the data path, but Razor FF [10] and Aging Aware FF [14] used a delayed clock instead of generating delay on data path which create a relatively large area for additional clock tree or clock delay circuit. Although the proposed ECSC has 2 MUXs and uses a duty cycle adjustable clock, it has relatively less overhead in a large design because no data/clock delay circuit and additional clock tree are needed.

Table 1. Comparison with Existing Cells

Modified FFs	Additional Logic	Timing Control	Relative Overhead
Razor FF [10]	1 Latch, 1 XOR	Delayed Clock	Additional clock tree
Canary FF [11]	1 Latch, 1 XOR, DDE[a]	Delayed Data	DDE logic
Aging Sensor FF [12]	1 FF, 1 XOR, DDE	Delayed Data	DDE logic
DPFF [13]	1 FF, 1 XOR, 2 MUXs, DDE	Delayed Data	2 MUXs DDE logic
Aging Aware FF [14]	1 Latch, 1 XOR, CDE[b]	Delayed clock	CDE logic
Proposed ECSC	1 FF, 1 XOR, 2 MUXs	Duty Cycle Adjusted Clock	2 MUXs, Clock duty cycle adjusting logic

[a]DDE: Data Delay Element, [b]CDE: Clock Delay Element

With regard to power consumption, although all the methods including our proposed ECSC do not create additional switching activities in combinational logic, it is obvious that the more scan cells a circuit has, the more power it consumes. However, since the proposed ECSC operates on the opposite clock edge and does not create additional switching activities in combinational logic, it will consume less power than the previous methods which use delay elements or additional clock tree.

It is natural that the total area and power consumption will increase with the increase of the number of scan cells because the size of an ECSC is bigger than that of a scan cell. However, aging monitoring techniques are targeted to electronic life-support systems or relatively large and high-end systems. In such systems, some increase in chip size and power consumption is acceptable if reliability and stability of the systems are guaranteed.

V. CONCLUSIONS

A failure during system operations in highly reliable systems such as medical equipment, satellites, aircrafts, or power plants might result in a disaster. Such a failure can occur because of transistor aging. In order to predict a failure and avoid disasters, we proposed a scan-based on-line aging monitoring scheme which observes aging by capturing functional data at different timing within the functional clock period and comparing the captured data. We added an early capture scan chain which captures the functional data earlier than the original scan chain. Guard-band interval is used to decide the early capture timing. The early capture scan chain is designed so as to capture functional data at the falling edges of the functional clock. We used an adjustable duty cycle clock generator to shift the falling edges within a guard-band interval. Since all the aging monitoring operations are performed during system operation, there is no performance impact.

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