Highly Linear Wideband LNA Design Using Inductive Shunt Feedback

Nam Hwi Jeong[1], Choon Sik Cho[1], and Seungwook Min[2]

Abstract—**Low noise amplifier (LNA) is an integral component of RF receiver and frequently required to operate at wide frequency bands for various wireless system applications. For wideband operation, important performance metrics such as voltage gain, return loss, noise figure and linearity have been carefully investigated and characterized for the proposed LNA. An inductive shunt feedback configuration is successfully employed in the input stage of the proposed LNA which incorporates cascaded networks with a peaking inductor in the buffer stage. Design equations for obtaining low and high impedance-matching frequencies are easily derived, leading to a relatively simple method for circuit implementation. Careful theoretical analysis explains that input impedance can be described in the form of second-order frequency response, where poles and zeros are characterized and utilized for realizing the wideband response. Linearity is significantly improved because the inductor located between the gate and the drain decreases the third-order harmonics at the output. Fabricated in 0.18 μm CMOS process, the chip area of this wideband LNA is 0.202 mm^2, including pads. Measurement results illustrate that the input return loss shows less than -7 dB, voltage gain greater than 8 dB, and a little high noise figure around 6-8 dB over 1.5 - 13 GHz. In addition, good linearity (IIP3) of 2.5 dBm is achieved at 8 GHz and 14 mA of current is consumed from a 1.8 V supply.**

Index Terms—**Low noise amplifier, wideband, inductive shunt feedback, high linearity, RF CMOS**

I. INTRODUCTION

For transmitting large amounts of data at a high-data rate through wireless systems, wideband LNA is required on the receiver side. The design approaches for wideband LNAs can be categorized into many methods. Resistive feedback amplifiers [1-4] create a wideband input impedance match, but gain decreases at high frequencies. Capacitive feedback or active feedback can be utilized to compensate for the gain decrease in resistive feedback amplifiers [5, 6]. Conventionally inductive peaking or capacitive peaking has been employed to obtain a bandwidth extension [7-10]. However, analytic expressions for return loss or input impedance have not been fully derived for this topology using inductive peaking. Resistive feedback is frequently combined with inductive peaking [11, 12], and an inductor coupled resonator is sometimes utilized in the feedback loop [13]. The wideband input matching network can also be designed using a high-pass filter [14], where an input-matching network is devised separately with the cascode amplifier, but the parasitics can lead to a fluctuation of input-matching characteristics. The common-gate configuration can be easily used for wide input impedance matching [15].

The present work proposes an inductive shunt feedback circuit between drain and gate of the first stage

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transistor for simultaneously achieving wideband characteristic and high linearity. The equation for input impedance is deduced analytically to obtain the low and high input impedance-matching frequencies of the pass-band of interest. The parasitic capacitance between gate and source of transistor in the input stage is easily integrated into these design equations. The inductive gate peaking is utilized in the buffer stage for extending the bandwidth of voltage gain. The linearity has been improved substantially because the shunt inductor located in the feedback loop suppresses the third-order harmonics at the output port. In this work, the design philosophy is explained and derived in Section II, and a wideband LNA using the proposed configuration is implemented in Section III. Simulations and measurement results are presented in detail in Section IV, and finally conclusion is made in Section V.

II. DESIGN PHILOSOPHY

The shunt feedback is commonly utilized for extending the bandwidth of amplifiers. LNAs employing resistive shunt feedback (sometimes along with active buffer in the feedback path) provide bandwidth extension compared with simple common-source amplifiers. However, gate inductive peaking is frequently needed for a greater extension of bandwidth. Unfortunately, the analytical derivation for the input impedance of LNAs using gate inductive feedback is quite complicated [4]. Moreover, NF and input impedance matching are in general traded off. The present work proposes an inductive shunt feedback topology for realizing wideband input impedance matching, where a resistor is inserted at the drain output and an external capacitor is added at the gate input, as shown in Fig. 1. The equivalent circuit model is illustrated in Fig. 2. The input impedance of this proposed circuit is calculated without difficulty, as derived in (1), where C_L represents the total load capacitance of the following stage and C_{gs} refers to the external capacitance C_g plus the inherent parasitic capacitance C'_{gs}. This input impedance should be equal to the characteristic impedance (Z_0) for ideal matching, as expressed in (3). Taking the real and imaginary parts of (2) separately, two equations can be derived, as expressed in (3) and (4). Once we can obtain more than two frequencies (actually two frequencies in this work) for

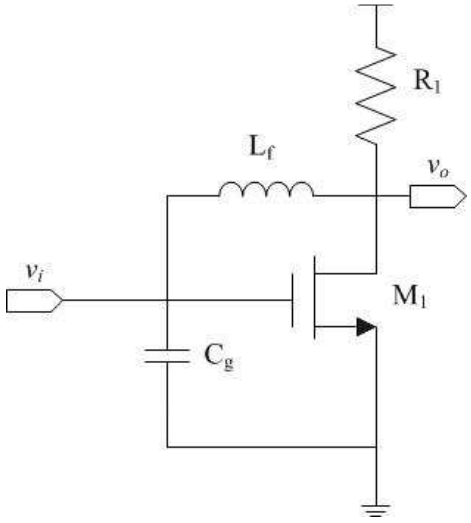

Fig. 1. The proposed wideband circuit using an inductive feedback network.

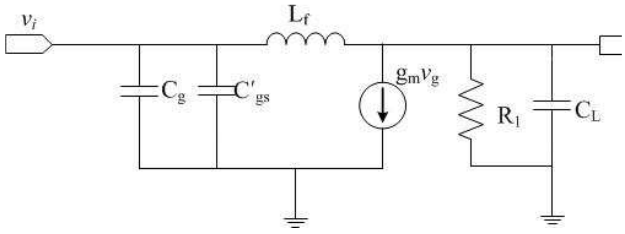

Fig. 2. Small-signal equivalent model of Fig. 1.

satisfying these two equations simultaneously, wideband input impedance- matching can be achieved plainly at these frequencies.

$$Z_{in} = \frac{1}{sC_{gs}} \frac{1}{1+\dfrac{\dfrac{1}{sC_{gs}+\dfrac{g_m R_1}{1+sR_1C_L}}}{sL_f + R_1 \| \dfrac{1}{sC_L}}}$$

$$= \frac{R_1 + sL_f + s^2 R_1 L_f C_L}{1 + g_m R_1 + sR_1(C_{gs}+C_L) + s^2 C_{gs} L_f + s^3 R_1 L_f C_L C_{gs}} \quad (1)$$

$$Z_0 = \frac{R_1(1-\omega^2 C_L L_f) + j\omega L_f}{1 + g_m R_1 - \omega^2 C_{gs} L_f + j\omega R_1(C_L + C_{gs}) - j\omega^3 C_{gs} L_f R_1 C_L}$$

$$Z_0(1 + g_m R_1 - \omega^2 C_{gs} L_f) + j\omega Z_0[R_1(C_L + C_{gs}) - \omega^2 C_{gs} L_f R_1 C_L] = R_1(1-\omega^2 C_L L_f) + j\omega L_f \quad (2)$$

$$Z_0(1 + g_m R_1) - R_1 = \omega^2 (Z_0 C_{gs} L_f - R_1 C_L L_f) \quad (3)$$

Since the reactive elements do not contribute to input impedance at *dc*, (3) can be reduced to (5). As expected,

the input impedance can be represented by a parallel combination of the load resistance and transconductance of M_1. By proper selection of R_1 and the transconductance of M_1, the input impedance can be matched to Z_0 at *dc* without difficulty, which means the very low frequency around *dc* can be used for the low input impedance-matching frequency. The high (=second) input impedance-matching frequency is derived by solving (3) and (4) simultaneously, as seen in (6). (6) can be solved in terms of Z_0 as shown in (7) where Z_0 can be obtained using g_m, R_1, L_F, C_{gs} and C_L. Since R_1 and g_m are chosen from (5), L_f, C_{gs} and C_L need to be determined for specific Z_0. It is possible to achieve wideband input impedance matching by assigning two frequencies, indicating the lowest return loss at *dc* and ω_{o2} expressed in (6).

$$L_f = Z_0[R_1(C_L + C_{gs} - \omega^2 C_{gs} L_f R_1 C_L)] \tag{4}$$

$$Z_0 = \frac{R_1}{1 + g_m R_1} = R_1 \,\|\, \frac{1}{g_m} \tag{5}$$

$$\omega_{o2}^2 = \frac{Z_0(1 + g_m R_1) - R_1}{Z_0 C_{gs} L_f - R_1 C_L L_f} = \frac{Z_0 R_1 (C_{gs} + C_L) - L_f}{Z_0 R_1 L_f C_{gs} C_L} \tag{6}$$

$$Z_0 = \frac{-L_f(R_1^2 C_L^2 + L_f C_{gs}) \pm \sqrt{L_f^2(R_1^2 C_L^2 + L_f C_{gs})^2 + 4R_1^2 L_f^2 C_{gs} C_L (g_m R_1 C_L - C_{gs})}}{2R_1 L_f C_{gs}(g_m R_1 C_L - C_{gs})} \tag{7}$$

Meanwhile, the voltage gain for Fig. 1 can be easily computed using the equivalent circuit model shown in Fig. 2, as represented in (8). This exhibits the maximum gain at the resonant frequency of resonator composed of feedback inductor and load capacitor.

$$A_v = \frac{v_o}{v_{gs}} = \frac{R_L(1 - j\omega g_m L_f)}{R_L(1 - \omega^2 L_f C_L) + j\omega L_f} \tag{8}$$

Since $v_o = i_o(R_L \,\|\, \frac{1}{sC_L})$, the equivalent transconductance (G_m) for this inductive shunt feedback circuit can be expressed as (9):

$$G_m = \frac{i_o}{v_{gs}} = \frac{(1 - j\omega g_m L_f)(1 + j\omega R_L C_L)}{R_L(1 - \omega^2 L_f C_L) + j\omega L_f}. \tag{9}$$

(9) reveals that G_m reaches its highest value around the resonant frequency of resonator composed of feedback inductor and load capacitor, as does the voltage gain.

Besides, the input referred noise voltage and current can be represented as (10) and (11).

$$\overline{v_{n,i}^2} = \frac{\overline{i_{n,d}^2}}{G_m^2} = \frac{4kT\gamma g_m \Delta f[R_L^2(1 - \omega^2 L_f C_L)^2 + \omega^2 L_f^2]}{(1 + \omega^2 g_m^2 L_f^2)(1 + \omega^2 R_L^2 C_L^2)} \tag{10}$$

$$\overline{i_{n,i}^2} = \frac{\overline{i_{n,d}^2}}{G_m^2 Z_{in}^2} = \frac{4kT\gamma g_m \Delta f[R_L^2(1 - \omega^2 L_f C_L)^2 + \omega^2 L_f^2]}{(1 + \omega^2 g_m^2 L_f^2)(1 + \omega^2 R_L^2 C_L^2) Z_{in}^2} \tag{11}$$

where k is the Boltzmann's constant, T is the absolute temperature, Z_{in} is input impedance, Δf is the noise bandwidth, and γ is the thermal excess noise factor, which is about 2/3 in a long channel device. Here, (10) and (11) reveal that the input-referred noise voltage and current decrease as the frequency approaches the resonant frequency of resonator composed of feedback inductor and load capacitor, as given in the voltage gain and the equivalent transconductance.

As expressed in (11), the input referred noise current is inversely proportional to transconductance and input impedance. Increasing the number of fingers and/or bias voltage of gate-to-source (V_{GS}) leads to increase of transconductance (g_m), where V_{GS} is determined automatically by the bias voltage at drain of M_1. Therefore, it is not quite easy to optimize V_{GS} of M_1 for low noise in this circuit. Increasing the number of fingers of M_1 gives rise to increase of C_{gs}, and then increase of C_{gs} provides decrease of input impedance (Z_{in}). Due to this kind of conflict in design stage, very careful selection of bias voltage at gate, transistor width and input capacitance is definitely required. Meanwhile, since the condition for wideband input impedance matching is also different from the optimized noise condition, we put higher priority for wideband impedance matching compared with noise optimization, which can cause little higher noise performance over whole bandwidth of interest.

Other than NF and impedance matching, distortion occurring in the LNA design has been characterized systematically in [16]. Therefore, in principle this distortion can be alleviated by suppressing even- and odd-order harmonics simultaneously. As shown in Fig. 3, the feedback current through the shunt inductor is 90° out of phase with the input current, so that this feedback current plays an important role in suppressing third-order harmonics at the output. C_{gs} is C_g plus C'_{gs} and Z_L

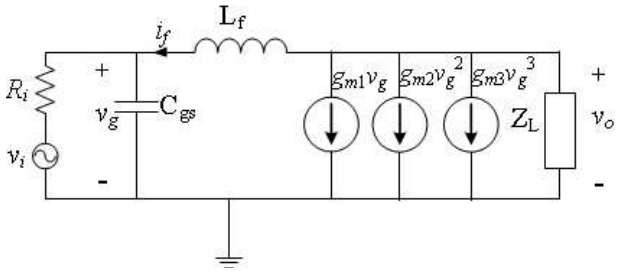

Fig. 3. Circuit diagram for exploiting distortion reduction.

represents $R_L \parallel C_L$. Due to the inherent nonlinearity of transistors, the equivalent drain current can be approximated up to third-order as $i_d=g_{m1}v_g+g_{m2}v_g^2+g_m^3v_g^3$. The voltage across C_{gs} can be expressed using the feedback current i_f as in (12) since $i_f = -(i_d+v_o/Z_L)$.

$$v_g = v_o - L\frac{di_f}{dt} = v_o + L\frac{d}{dt}(g_{m1}v_g + g_{m2}v_g^2 + g_{m3}v_g^3 + \frac{vo}{Z_L}) \tag{12}$$

Since the source resistance R_i is much smaller than the input impedance looking into the gate of transistor, v_i can be approximated as v_g. Thus, v_o can also be expressed as in (13) with constants a_1, a_2 and a_3, because v_o can be thought to be a nonlinear function of v_i.

$$v_o \simeq a_1 v_i + a_2 v_i^2 + a_3 v_i^3 \tag{13}$$

Therefore, v_g can be approximately represented by (14).

$$\begin{aligned} v_g &\simeq a_1 v_i + a_2 v_i^2 + a_3 v_i^3 \\ &+ L\frac{d}{dt}\left[g_{m1}v_g + g_{m2}v_g^2 + g_{m3}v_g^3 + \frac{a_1 vi + a_2 v_i^2 + a_3 v_i^3}{Z_L} \right] \\ &\simeq a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + L\frac{d}{dt}(b_1 v_i + b_2 v_i^2 + b_3 v_i^3) \end{aligned} \tag{14}$$

This means that gate voltage is a sum of nonlinear product of the input voltage and its differentiated (or phase leading) values. When two voltage signals spaced closely in frequency are applied to the input port as $v_i=A_1cos\omega_1 t+A_2cos\omega_2 t$, substituting v_i for (14), v_g can be expressed as a linear sum of the various frequency components, as shown in (15), with $f(x) = \cos x$. Because the third-order intermodulation product (IM3) of the output voltage contributes to nonlinearity of the overall circuit, the terms corresponding to $(2\omega_1 - \omega_2)$ can be represented as in (16). As seen in (16), each pair can be aligned out of phase, and thus eventually the IM3 product can be suppressed effectively by properly choosing the constants a_{mm} and b_{mm}. In other words, feedback inductor can be adjusted for reducing the IM3 power as desired.

$$\begin{aligned} v_g &= \sum_{m,n=0}^{3} a_{mn} f(m\omega_1 t \pm n\omega_2 t) \\ &- \sum_{m,n=0}^{3} b_{mn} f(m\omega_1 \pm n\omega_2 t + (m+n)\times 90^\circ) \end{aligned} \tag{15}$$

$$\begin{aligned} v_o\,|_{IM3} &= g_{m3}Z_L \times \\ &\{a_{21}b_{00}f(2\omega_1-\omega_2) + a_{00}b_{10}b_{20}f(2\omega_1-\omega_2+180^\circ) \\ &-a_{20}b_{01}f(2\omega_1-\omega_2+90^\circ) + b_{01}b_{10}^2 f(2\omega_1-\omega_2+270^\circ) \\ &+a_{10}^2 f(2\omega_1-\omega_2) = a_{01}b_{10}^2 f(2\omega_1-\omega_2+180^\circ)+....\} \end{aligned} \tag{16}$$

III. DESIGN OF THE WIDEBAND LNA

Using the design philosophy proposed in Section II, a wideband LNA has been implemented, as shown in Fig. 4, which includes a feedback shunt inductor in the input stage, a common source amplifier in the second stage, and a peaking inductor and another common source amplifier as the output buffer. In the input stage, the transistor M_1 constitutes the feedback topology combined with feedback inductor L_f to achieve the desired bandwidth extension. The external gate input capacitor C_g, combined with the parasitic capacitance C'_{gs} and L_f, controls the high input-matching frequency which is equal to ω_{o2} in (6). The low frequency input impedance and voltage gain are determined by R_1 and the transconductance of M_1 (g_{m1}). The second stage is a common source amplifier used to obtain sufficient voltage gain. In the buffer stage, a gate peaking inductor is employed to further extend the bandwidth. Additional inductor is placed at the output to achieve sufficient RF voltage swing.

Several combinations of R_1, C_{gs}, C_L and L_f are manipulated in theoretical computations of high input-matching frequency for the basic inductive feedback circuit, as illustrated in Fig. 1, where 18 GHz is used temporarily for calculating the desired high input-matching frequency (ω_{o2}) leading to a perfect match to 50 Ω. Good candidate values are calculated as listed in

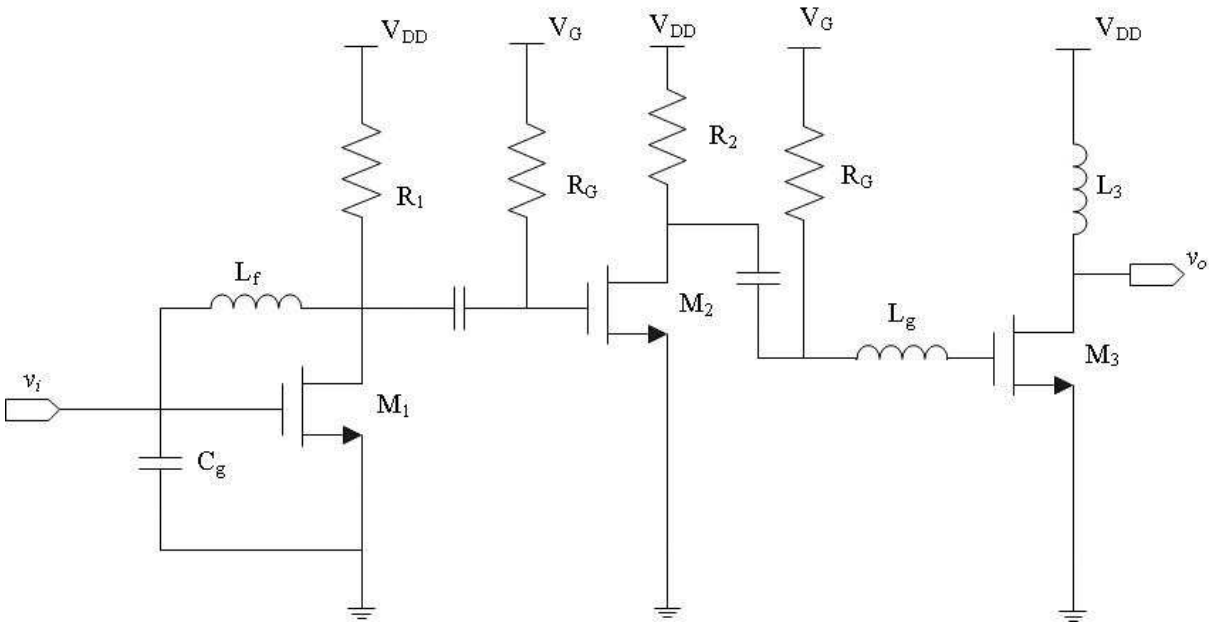

Fig. 4. Schematic of the proposed wideband LNA.

Table 1. Using the computed values in Table 1, the input return loss is calculated, as shown in Fig. 5, where an excellent input-match is achieved at *dc* and ω_{o2} frequencies. Input return losses are illustrated graphically by varying L_f and C_L while maintaining R_1 and C_{gs}, because the feedback inductance (L_f) of the input stage and input capacitance (C_L) of the second stage allow more freedom of choice to provide the desired circuit performance. As L_f decreases and C_L increases, the bandwidth is extended as desired.

Transistor dimensions play a significant role in the input stage, since the parasitic capacitance C'_{gs} can reach hundreds of fF, and g_{m1} is critical for achieving high gain and low noise. In this circuit, a gate width of 2×10μm is chosen for M_1, 65 Ω is used for R_1 to set the low input impedance-matching frequency and *dc* headroom of input stage amplifier. This results in a transconductance between 10 mS and 20 mS. The external capacitor C_g is chosen to be 230 fF, taking into account C'_{gs} of 20 fF, which is extracted from layout parasitics. While the LNA design is simplified because the input impedance is easily calculated from g_{m1} combined with R_1 to match the input impedance Z_0 at the low frequency around dc, this makes it difficult to lower the NF with the chosen g_{m1}. Since the gate biasing for M_1 cannot be determined independently, the drain biasing for it is carefully designed considering the drain current and then g_{m1}. 1.65

Table 1. Design parameters for the proposed LNA

Parameters	Computed	Pre-layout	Post-layout
R_1 (Ω)	70	65	70
C_{gs} (pF)	110	250	80
L_f (nF)	0.55	0.533	0.533
R_2 (Ω)	-	125	125
L_g (nF)	-	0.898	1.1
L_3 (nF)	-	2.072	2.11
M_1	-	(10μm/0.18μm)×2	
M_2	-	(10μm/0.18μm)×16	
M_3	-	(10μm/0.18μm)×10	
V_D at M_1	-	1.65 V	1.64 V
V_G at M_1	-	1.65 V	1.64 V
I_D at M_1	-	2.12 mA	2.13 mA
I_D for whole circuit	-	11 mA	11 mA

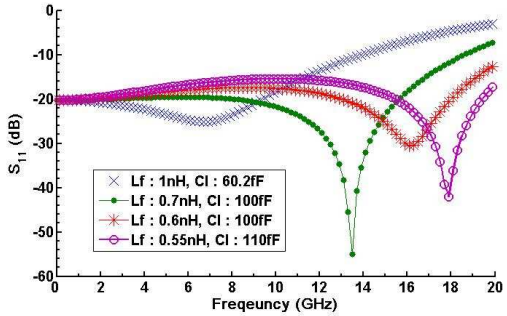

Fig. 5. Calculated return loss of the basic inductive feedback circuit.

V is chosen for the drain and gate biasing of M_1. M_2 needs to supply sufficient voltage gain to compensate any insufficient voltage amplification in the input stage due to restriction occurring from relatively low g_{m1}. The gate width of M_2 contributes to the load capacitance (C_L) of input stage affecting bandwidth extension, so that a proper value considering L_f, is chosen for the gate width of M_2. 16×10μm is chosen for this purpose. R_2 is chosen to be 125 Ω. For the gate peaking inductor (L_g), an inductance around 0.9 nH is used. A 2.072 nH inductor is chosen at the drain (L_3) to ensure sufficient *dc* voltage headroom and output impedance matching. Total drain current of 11 mA flows over this circuit. Design parameters are finally optimized after layout as listed in Table 1.

The output impedance matching is carried out based on the equivalent circuit as drawn in Fig. 6 where C_d represents the capacitance at drain of M_3, R_o the resistance between drain and source of M_3, C_c the coupling capacitance, and C_L the load capacitance that may occur on connecting to the following circuits or from pad parasitic. The output impedance Z_{out} can be calculated as expressed in (17).

$$Z_{out} = \frac{1}{sC_L} \| \left(\frac{1}{sC_c} + \frac{1}{sC_d + \frac{1}{R} + \frac{1}{sC_L}}\right) = \frac{R + sL + s^2L(C_d + C_L)R}{D} \tag{17}$$

where $D = s(C_c+C_L)R+s^2(C_c+C_L)L+s^3L(C_cC_d+C_dC_L+C_cC_c)R$. Equating Z_{out} to be 50 Ω, (17) can be realigned to (18).

$$50[-j\omega^3L(C_cC_d + C_dC_L + C_cC_L) - \omega^2(C_c + C_L)L + j\omega(C_c + C_L)R] = -\omega^2L(C_d + C_L)R + j\omega L + R \tag{18}$$

Solving (18) by separating real and imaginary parts, the impedance matching frequency can be calculated as in (19) as expected in the right side of Fig. 6 where C_c is considerably big compared with other capacitor values and can be ignored. 7.5 GHz has been used for this frequency for output impedance matching.

$$\omega_{out} \simeq \sqrt{\frac{1}{L(C_d + C_L)}} \tag{19}$$

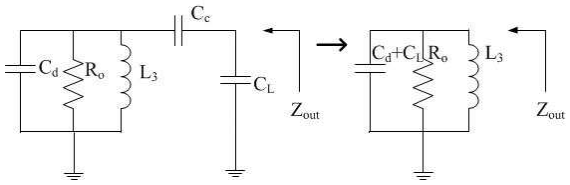

Fig. 6. Equivalent circuit for calculating output impedance.

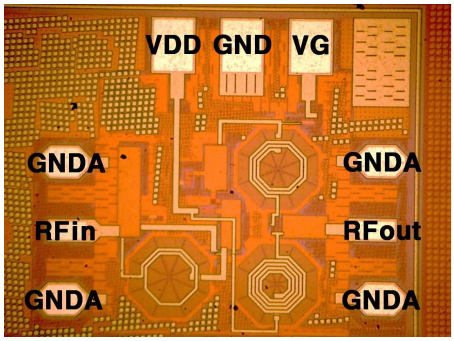

Fig. 7. Chip photograph of the proposed wideband LNA.

Since Q of parallel resonant circuit as seen in Fig. 6 is $R_o\sqrt{(C_d + C_L)/L_3}$, low Q (< 1) is required for wideband output matching, leading to need of small capacitance and large inductance. For this requirement, we optimize L_3 and (C_d + C_L) for achieving as low Q as possible and use 2.072 nH for L_3 and under 20 fF for (C_d + C_L) including parasitics.

IV. Simulation and Measurement

The proposed wideband LNA was fabricated using design parameters optimized as listed in Table 1 in a 0.18 μm RF CMOS process technology, and the chip photograph is shown in Fig. 7. The overall chip size (with pads) is 0.8 × 0.7 mm^2 and the core area is 0.45 × 0.45 mm^2. The designed wideband LNA was biased at V_{DD} = 1.8 V and V_g = 0.7V, and draws 14 mA of current. An on-wafer probe station was used for measuring the S-parameters from 0.1 to 20 GHz, and S_{11} and S_{21} are displayed in Fig. 8 along with the post-layout simulation results. The fabricated wideband LNA designed based on the design philosophy explained in Section II works from 1.5 GHz to 13 GHz and obtains a maximum small-signal voltage gain of 11 dB at 11 GHz and a minimum value of 8 dB at 13 GHz. The simulated S_{21} shows very similar results to measurement one.

S_{11} was measured less than -7 dB within this frequency

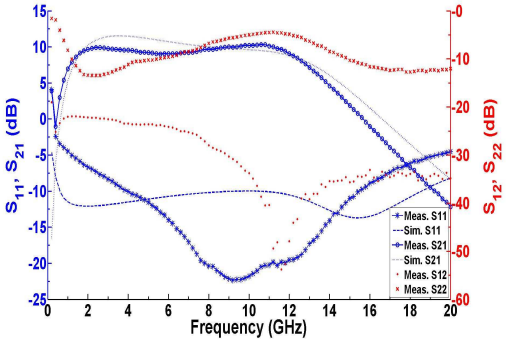

Fig. 8. Measured S-parameters.

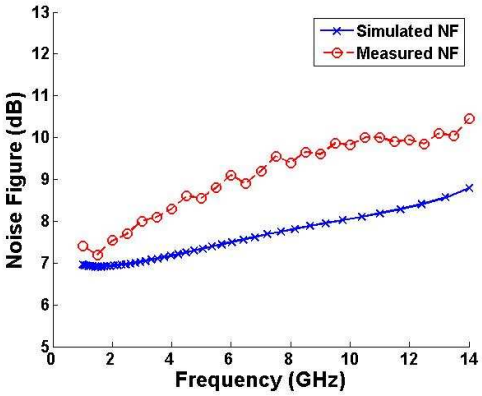

Fig. 9. Measured and simulated noise figures.

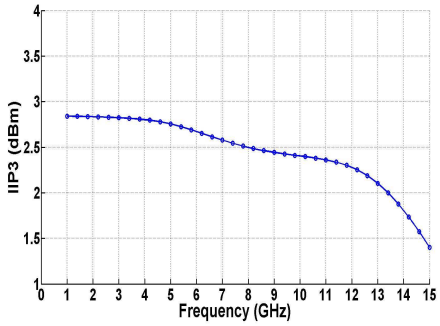

Fig. 10. Measured IIP3.

range, while post-layout simulation shows under -10 dB from 0.1 GHz to 18 GHz. The measured S_{11} shows deviated results compared with those of simulation in S_{11}. This is possibly because input impedance at the low input-matching frequency is deviated from the value as shown in (5) due to altered g_m possibly originating from unexpected parasitics. As seen in Fig. 8, S_{11} at low frequency goes higher compared with simulation result. The high input-matching frequency moves to lower band due to excessive C_{gs} originating from parasitic of input pad. S_{12} and S_{22} results are exhibited in Fig. 8, where S_{12} is kept under -20 dB and S_{22} under -6 dB from 1.5 GHz to 13 GHz.

Fig. 9 illustrates the simulated and measured NF from 1.5 GHz to 13 GHz, with values of 6 - 8 dB and 7 - 10 dB, respectively. As seen in Fig. 9, NF is measured to be 7.3 dB at 1.5 GHz. The measured NF is a little higher at 1.5 - 13 GHz in comparison with simulated results. Fig. 10 displays the measured input third-order inter-modulation (IIP3) versus frequency, with a two-tone

Table 2. Comparison with other wideband lnas operating in similar bands

	Bandwidth (GHz)	$Gain_{max}$ (dB)	NF (dB)	S_{11} (dB)	Power (mW)	IIP3 (dBm)	Area (mm^2)	Topology	Technology
[1]	3-8	15.2	4.2-8	< -8	3.77	-6.63	0.96	Resistive feedback	0.18 μm CMOS
[2]	1-10.5	16.5	3.9-5	< -10	36	-5	0.021	Resistive feedback	65 nm CMOS
[3]	1.6-28	10.7	2.92-4.4	< -10	21.6	4	0.139	Resistive feedback	90 nm CMOS
[4]	3.1-10.6	12.4	2.7-3.7	< -7.3	14.4	-3.8	0.031	Resistive feedback	0.13 μm CMOS
[5]	3.1-10.6	11	4.5-5.1	< -11	21	-12	0.46	Capacitive feedback	0.18 μm CMOS
[6]	0-22.1	10.7	4.3-6.5	< -10	8.4	-2.67	0.017	Dual feedback	90 nm CMOS
[7]	0-6.5	16.5	2-2.7	< -10	9.7	-2	0.0017	Active feedback	90 nm CMOS
[8]	5-11	19.1	1.8-2.6	< -4	9.0	-	1.078[a]	Inductive/capacitive peaking	0.12 μm SiGe
[9]	3-10.6	15	4-4.4	< -7	21.5	2.5	0.688[a]	Inductive peaking	0.18 μm CMOS
[10]	2-9.6	11	3.6-4.8	< -8.3	19	-7.2	0.05	Capacitive peaking	0.13 μm CMOS
[11]	3-20	19.1	4.2-5.2	< -4	116	-6	0.954[a]	Resistive feedback/peaking	0.18 μm SiGe
[12]	0-11.5	14.2	5-5.6	< -8	9.1	-10	0.08	Resistive feedback/peaking	0.13 μm CMOS
[13]	1.2-10.6	10.8	3.9-5.8	< -5.7	6.2	-5	1.32[a]	Inductor coupling resonator	0.18 μm CMOS
[14]	3.1-10.6	13	3.1-6	< -8	11.9	-7	1.2[a]	High-pass input filter	0.18 μm CMOS
[15]	1.5-8.1	11.7	3.6-6	< -9	2.62	14.1	0.58	Common gate	0.13 μm CMOS
This work	1.5-13	11	7.1-9.8	< -7	25.2	2.5	0.202	Inductive feedback	0.18 μm CMOS

a : include pads

spacing of 8 MHz. IIP3 is achieved from 2.8 dBm to 2.2 dBm over entire frequency band of interest, as expected theoretically. The overall performances of this fabricated LNA are compared with those of other previously published circuits, and are summarized in Table 2. Wideband performance with respect to the voltage gain, together with excellent input return loss over frequencies from under 1.5 GHz to over 13 GHz is achieved, with improved linearity, in spite of higher NF.

V. SUMMARY

A wideband LNA operating from under 1.5 GHz to over 13 GHz was designed and implemented based on design equations derived using inductive feedback topology in the input stage. The design equations developed here can easily be utilized to obtain a wideband input matching. Using two frequencies obtained for input impedance matching, input return loss can be easily computed and utilized to design an LNA circuit with wide bandwidth. The voltage gain displays flatness over the desired bandwidth while keeping S_{11} under -7 dB over this wide bandwidth. Input impedance matching is easily realized using the drain resistance and the transconductance of input stage at the low frequency, and feedback inductance and C_{gs} at the high frequency. The proposed LNA also shows good linearity performance because this feedback configuration alleviates nonlinear characteristics effectively. While the circuit offers a simple design and gain flatness over wide bandwidth, the NF still needs to be improved using specific noise cancellation methods.

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