Capacitive Readout Circuit for Tri-axes Microaccelerometer with Sub-fF Offset Calibration

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Abstract—**This paper presents a capacitive readout circuit for tri-axes microaccelerometer with sub-fF offset calibration capability. A charge sensitive amplifier (CSA) with correlated double sampling (CDS) and digital to equivalent capacitance converter (DECC) is proposed. The DECC is implemented using 10-bit DAC, charge transfer switches, and a charge-storing capacitor. The DECC circuit can realize the equivalent capacitance of sub-fF range with a smaller area and higher accuracy than previous offset cancelling circuit using series-connected capacitor arrays. The readout circuit and MEMS sensing element are integrated in a single package. The supply voltage and the current consumption of analog blocks are 3.3 V and 230 μA, respectively. The sensitivities of tri-axes are measured to be 3.87 mg/LSB, 3.87 mg/LSB and 3.90 mg/LSB, respectively. The offset calibration which is controlled by 10-bit DECC has a resolution of 12.4 LSB per step with high linearity. The noise levels of tri-axes are 349 μg/√Hz, 341 μg/√Hz and 411 μg/√Hz, respectively.**

Index Terms—**Capacitive readout circuit, micro-accelerometer, digital to equivalent capacitance converter (DECC)**

I. INTRODUCTION

The microaccelerometers have been successfully commercialized, and its applications have extended to various fields including automotive applications, mobile applications, and so on. In the mobile application, especially, the microaccelerometers have become an essential part to recognize motion and realize various functions. To satisfy the tight requirements of the recent mobile platforms, the footprint of Microelectro-mechanical System (MEMS) sensing device and its readout circuit should be small and power consumption should be lower than other applications. Thus, capacitive sensing scheme is generally used due to its strength of simple structure and low power consumption [1].

In two-chip microaccelerometers with separated MEMS sensing element and CMOS readout circuit, the analog front-end block is generally connected to the MEMS sensing element using wire-bonding. The parasitic capacitances between bonding pads are typically about 10^{-11}~10^{-12} F. As the size of sensing element gets smaller, the effect of the mismatch between these parasitic capacitances becomes more critical to the accelerometer's performance. The output signal can be easily saturated by even a little mismatch of several fF because the mechanical sensitivity with respect to the acceleration input is usually about a few fF/g.

Thus, to reduce output offset variations and obtain wide signal swing range, the calibration technique with sub-fF resolution is inevitable. An offset trimming is one of the most important issues in microaccelerometer readout circuit design. Some studies on calibration methods for minimizing the parasitic capacitance effect

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have been reported [1, 4, 5]. The minimum implementable capacitance is typically in the range of 10~20 fF on the minimum design rule. Therefore, previous researches implemented small capacitance by series-connected unit capacitance, which is area-consuming solution [4]. In addition, excessively sophisticated layout should be considered to form desired capacitance without unwanted parasitic components.

In this paper, a sub-fF trimmable readout circuit for capacitive tri-axes microaccelerometer is presented. A charge sensitive amplifier (CSA) with correlated double sampling (CDS) scheme and a precise offset calibration scheme is proposed. Instead of using series-connected capacitor arrays, the digital to equivalent capacitance converter (DECC) adopting offset calibration scheme using charge transferring [6, 7] is implemented using 10-bit DAC, charge transfer switches, and a charge-storing capacitor. The DECC circuit can realize the equivalent capacitance of sub-fF range with a small area and high accuracy. The calibration coefficients are stored to the on-chip EEPROM.

II. TOP LEVEL ARCHITECTURE

The block diagram of the top-level microsystem, consisting of the MEMS sensing element and CMOS readout circuit, is shown in Fig. 1. In the tri-axes MEMS sensing elements, the inertial force exerted by applied acceleration compels the proof mass to move, producing the capacitance changes between movable electrodes and fixed electrodes. To reduce the chip size and power consumptions, we adopted time-interleaved channel sharing scheme. A muxed CSA with CDS converts these capacitance changes to analog voltages. The CDS scheme eliminates the undesired low frequency components including 1/f noise and amplifier offset. The charge-transfer offset calibration circuit in CSA can adjust the output offset. A programmable gain amplifier (PGA) amplifies the signal to the desired target. An algorithmic ADC converts this analog input to digital data. The following digital signal processing block includes digital low pass filter (LPF) using a moving average method, additional offset and gain calibration, and motion interrupts generator. The internal register values including offset and gain calibration coefficients are stored to on-chip EEPROM. Both the SPI and I2C

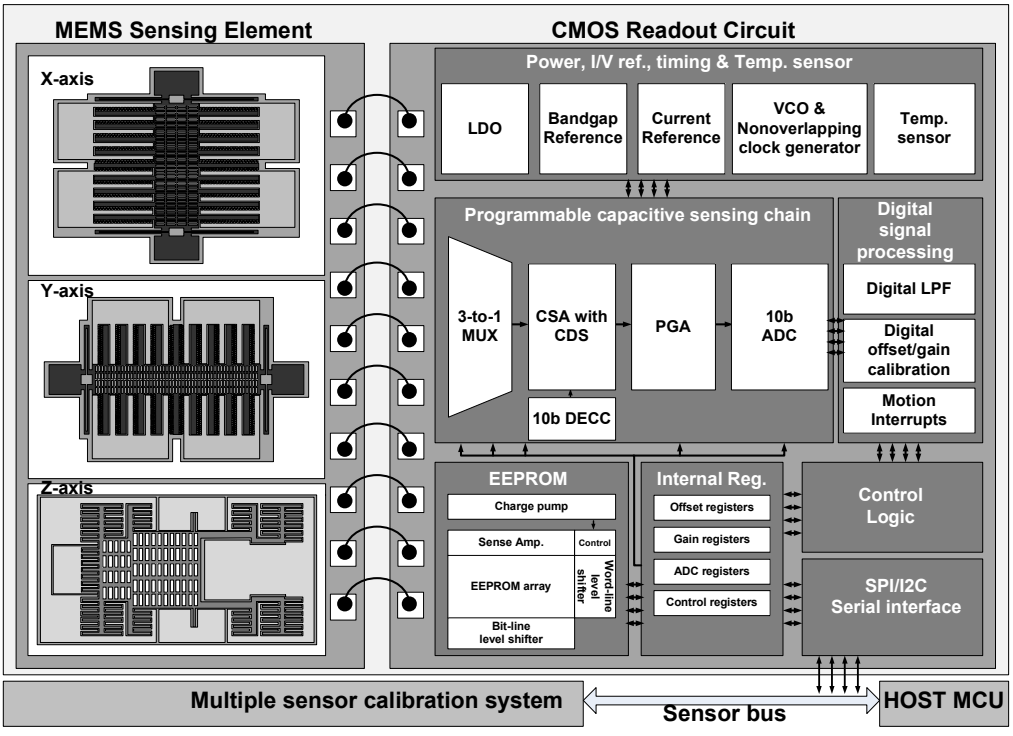


Fig. 1. Block diagram of the top-level microsystem.

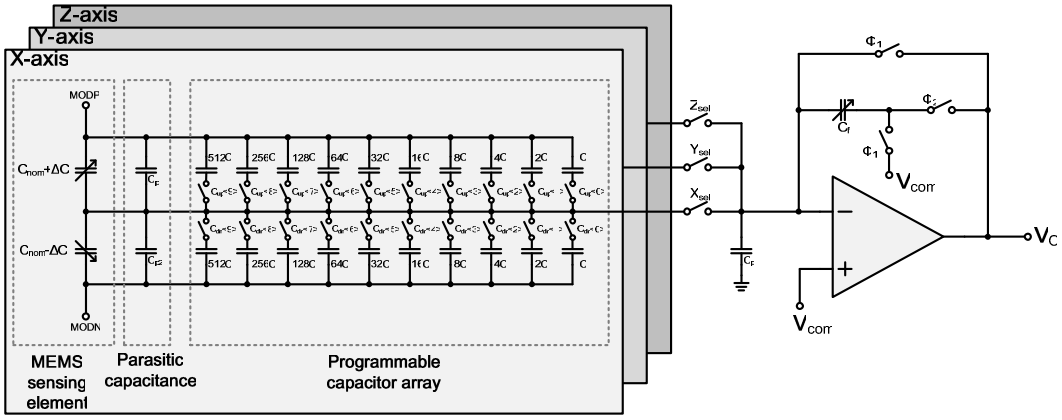
protocol are implemented to interface with various host systems and calibration systems.

III. PROGRAMMABLE CAPACITIVE SENSING CHAIN

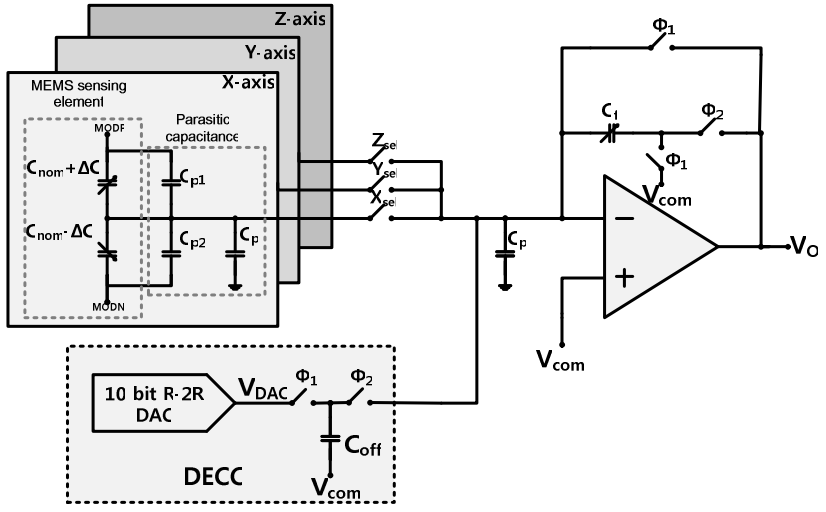
1. Proposed CSA Architecture with CDS and DECC

The schematics of the conventional CSA and the proposed CSA are shown in Fig. 2. Fig. 2(a) shows the conventional CSA with CDS and programmable capacitor arrays [5]. In conventional CSA, binary weighted capacitor arrays are generally used to compensate for output offset due to the parasitic capacitance mismatch. The binary weighted capacitor arrays, however, are not adequate approaches to implement the offset calibration circuit with sub-fF resolution and high linearity. In binary weighted capacitor array, area-consuming series-connected unit capacitances are required to implement the sub-fF capacitors, because the minimum implementable capacitance is typically in the range of 10~20 fF on the minimum design rule. Moreover, unwanted parasitic components by sophisticated interconnections degenerate the linearity of the capacitor arrays.

Since the capacitors for sub-fF calibration are difficult to be implemented, a new CSA with CDS and DECC is proposed without area-consuming capacitor arrays, as shown in Fig. 2(b). To achieve low noise characteristics, the proposed CSA adopts the CDS scheme reported in [2]. This has several advantages of speed and noise immunity compared to other CDS types reported in [3].



(a) Conventional CSA with CDS and programmable capacitor arrays



(b) Proposed CSA with CDS and DECC

Fig. 2. Conventional and proposed CSA circuit.

In this process, the capacitance density is 1 fF/μm^2, and the minimum allowed area of the capacitor in design rule is 16 μm^2 (= 4 μm × 4 μm). To implement the unit capacitance of 1 fF, 16 capacitors are connected in series, and the area consumption becomes 256 μm^2. In the conventional binary weighted capacitor array, thus, the silicon area of 262144 μm^2 (= 256 × 1024 μm^2) is required for 10 bit resolution. In the proposed DECC circuit, however, the equivalent 10 bit capacitor array can be implemented in only 12190 μm^2 (= 115 × 106 μm^2), which area is only 4.65 % of the conventional binary weighted capacitor arrays.

The offset calibration principal of the proposed CSA using DECC is as follows: In Fig. 2(b), C_{p1} and C_{p2} are parasitic capacitances. The DECC is implemented using 10-bit DAC, charge transfer switches, and a charge-storing capacitor. To compensate for an undesired charge from the mismatch between C_{p1} and C_{p2}, the DAC charges the charge-storing capacitor (C_{off}) at the reset phase of Φ_1.

The simplified schematic of the proposed CSA is shown in Fig. 3. The voltage across C_{off} is V_{DAC}-V_{COM}, where V_{DAC} is output voltage of 10 bit R-2R DAC, and V_{COM} is common mode voltage, VDD/2.

At Φ1 phase, the charges stored in the capacitors are expressed as follows.

$$Q_{u\Phi 1} = \left(V_{COM} - V_{DD}\right)\left(C_{nom} + \Delta C + C_{p1}\right) \tag{1}$$

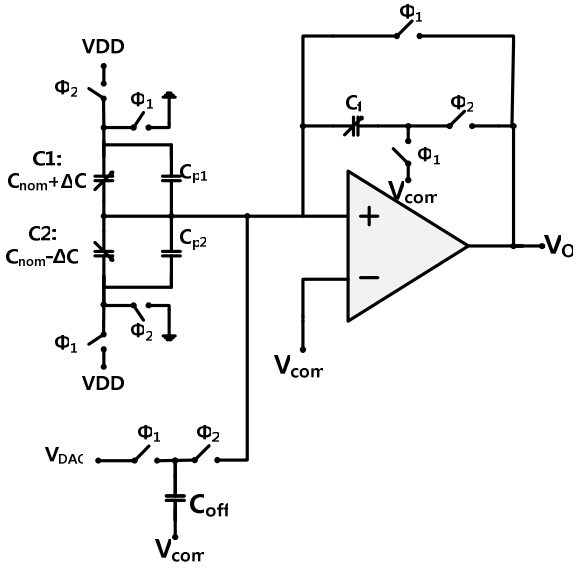


Fig. 3. Simplified schematic of proposed CSA.

$$Q_{d\Phi 1} = \left(V_{COM}\right)\left(C_{nom} - \Delta C + C_{p2}\right) \tag{2}$$

$$Q_{off\Phi 1} = \left(V_{DAC} - V_{COM}\right)C_{off} \tag{3}$$

$$Q_{total\Phi 1} = Q_{u\Phi 1} + Q_{d\Phi 1} + Q_{off\Phi 1} \tag{4}$$

Here, ΔC and Cnom are the capacitance change and the nominal capacitance of the MEMS sensing element, respectively. Also, the $Q_{u\Phi 1}$ is stored charge in C_{nom} + ΔC and C_{p1}, $Q_{d\Phi 1}$ is stored charge in C_{nom} - ΔC and C_{p2}, $Q_{off\Phi 1}$ is stored charge in C_{off}, and $Q_{total\Phi 1}$ is stored charge in the capacitors at Φ1 phase.

At the amplification phase of Φ2, the charge in C_{off} of C_{off} × (V_{DAC}-V_{COM}) and the charge in the MEMS sensing element are transferred to the left plate of a feedback capacitor (C_f), at the amplification phase of Φ_2. At Φ2 phase, the charges stored in the capacitors are expressed as follows.

$$Q_{u\Phi 2} = \left(V_{COM}\right)\left(C_{nom} + \Delta C + C_{p1}\right) \tag{5}$$

$$Q_{d\Phi 2} = \left(V_{COM} - V_{DD}\right)\left(C_{nom} - \Delta C + C_{p2}\right) \tag{6}$$

$$Q_{off\Phi 2} = \left(V_{COM} - V_{COM}\right)C_{off} = 0 \tag{7}$$

$$Q_{f\Phi 2} = \left(V_{COM} - V_o\right)C_f \tag{8}$$

$$Q_{total\Phi 2} = Q_{u\Phi 2} + Q_{d\Phi 2} + Q_{off\Phi 2} + Q_{f\Phi 2} \tag{9}$$

Here, the $Q_{u\Phi 2}$ is stored charge in C_{nom} + ΔC and C_{p1}, $Q_{d\Phi 2}$ is stored charge in C_{nom} - ΔC and C_{p2}, $Q_{off\Phi 2}$ is stored charge in C_{off}, $Q_{f\Phi 2}$ is stored charge in C_f and $Q_{total\Phi 2}$ is stored charge in the capacitors at Φ2 phase.

Therefore, the output voltage, V_o, can be expressed using charge conservation between phase Φ1 and Φ2, as follows

$$V_o = V_{COM} + \frac{V_{DD} \times \left(2\Delta C + \Delta C_p + C_{eq}\right)}{C_f} \tag{10}$$

where ΔC is capacitance change from the MEMS sensing element, ΔC_p is parasitic capacitance mismatch (C_{p1} - C_{p2}), and C_{eq} is the equivalent capacitance generated by DECC. The C_{eq} is expressed as

$$C_{eq} = \frac{\left(V_{COM} - V_{DAC}\right)}{V_{DD}} \times C_{off} \tag{11}$$

As expressed in (10) and (11), the output offset due to ΔC_p can be canceled out by programming C_{eq} using

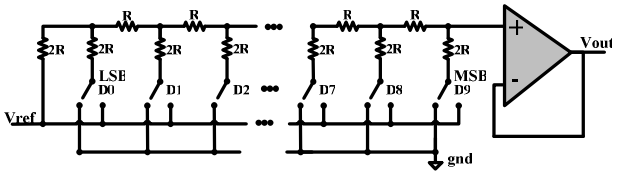


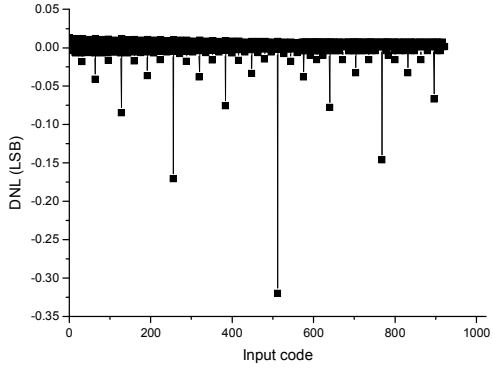
Fig. 4. 10 bit R-2R DAC in DECC.

DECC.

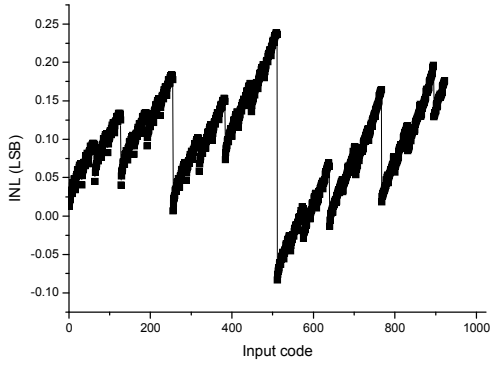
In the proposed CSA, the DAC has an output range from 0 V to VDD with 10-bit resolution. The charge-storing capacitor (C_{off}) is designed to be 512 fF. Thus, the minimum trimming step and maximum trimming range of C_{eq} are calculated to be 0.5 fF and ±256 fF, respectively. The DAC is implemented using R-2R ladder type, as shown in Fig. 4, because it has high performance with low power and does not need to have fast conversion rate.

Fig. 5 shows the simulation results of DECC. The simulated DNL and INL of the DECC are less than 0.32 LSB and 0.24 LSB, respectively, as shown in Figs. 5(a) and (b). Fig. 5(c) shows the equivalent capacitance (C_{eq}) and ΔC_{eq} (= $C_{eq}[n+1]$ - $C_{eq}[n]$) with increasing input code. The full range and programming resolution of C_{eq} are ±270 fF and 0.53 fF/code, respectively.

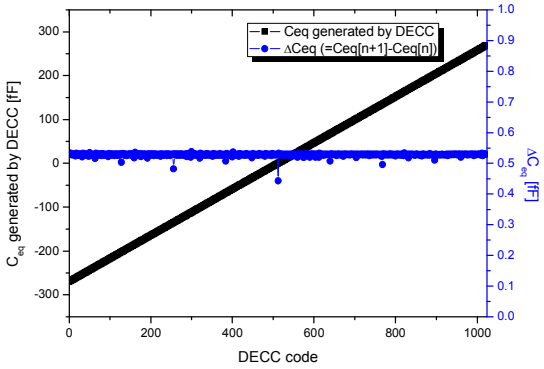
In the CSA, the modulation clock frequency is 64 kHz. The operational amplifier adopts general folded-cascode scheme. Assuming the total input capacitance of 7pF, the feedback capacitance of 576fF and a capacitive load of 180fF, the design specifications at the phase of amplification are summarized in Table 1.



(a) Simulated DNL



(b) Simulated INL



(c) Equivalent capacitance (C_{eq}) and ΔC_{eq}

Fig. 5. Simulation results of DECC.

Table 1. Specifications of CSA

Open Loop DC Gain	67 dB
Phase Margin	88°
Unity Gain Bandwidth (closed loop)	660 kHz
Current Consumption	16 uA

2. PGA with CDS

A CSA output is amplified by a programmable gain amplifier (PGA) to adjust the signal to the desired level. The designed PGA with CDS is shown in Fig. 6. The offset and 1/f noise components are removed by CDS, and the output voltage of PGA (V_{PGA}) is expressed as

$$V_{PGA} = V_{COM} + V_{CSA} \cdot \frac{C_f}{C_{in}} \quad (12)$$

The output voltage is determined with respect to the amount of the charge and the ratio of C_{in} and C_f, with the offset portion eliminated. In this circuit, the input capacitance (C_{in}) has a range from 25 fF to 180 fF with 32 steps and the feedback capacitance (C_f) is 25 fF. The simulated gain of PGA with increasing input code is shown in Fig. 7. The gain of PGA is programmable from 1 V/V to 8 V/V with 5 bit resolution.

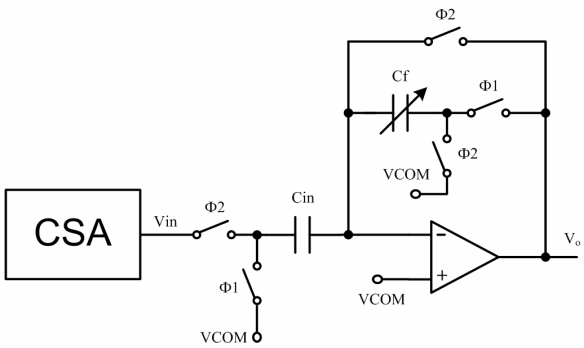


Fig. 6. PGA with CDS.

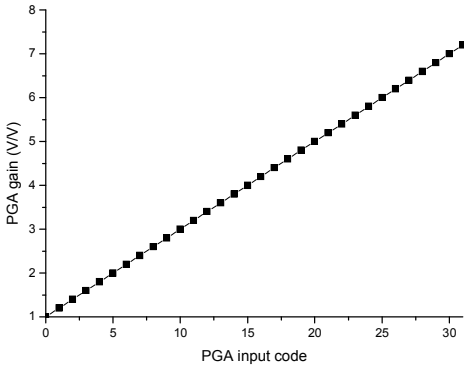
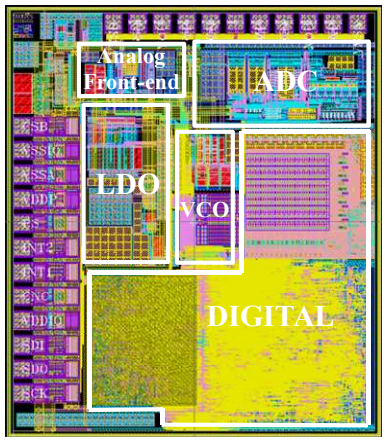


Fig. 7. Simulated gain of PGA.

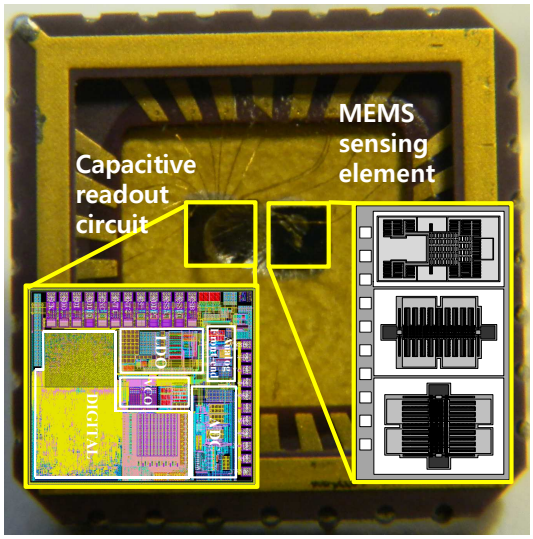
IV. Measurement Results

The readout circuit was implemented in the 0.18 μm 1P4M CMOS process with EEPROM. The die size is 1300 μm × 1500 μm and the MEMS device is 1050 μm × 1050 μm. Figs. 8(a) and (b) show the layout of the circuit and the packaged prototype of the microaccelrometer system. The supply voltage for the system is typically 3.3V, and an internal LDO generates a 1.8V supply for the analog block. Also, the supply current for analog circuits is measured to be 230 μA. In power-down mode, the supply current is measured to be less than 1 μA.

Fig. 9 shows the measurement results when the ±1 g acceleration inputs per each axis are applied. As the microaccelerometer is manually flipped along the x-, y- and z-axes, the accelerometer output is accordingly changed. The output offset and sensitivity are calibrated by using DECC and PGA. The calibration target of the output sensitivity is 512 LSB/±1 g (= 256 LSB/g = 3.906 mg/LSB). After calibration, the output sensitivities of three axes are measured to be 3.87 mg/LSB, 3.87 mg/LSB and 3.90 mg/LSB, respectively. The output



(a) layout



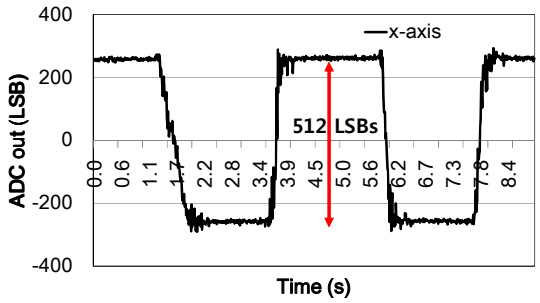
(b) two-chip implemented tri-axes microacclerometer

Fig. 8. Fabrication results.

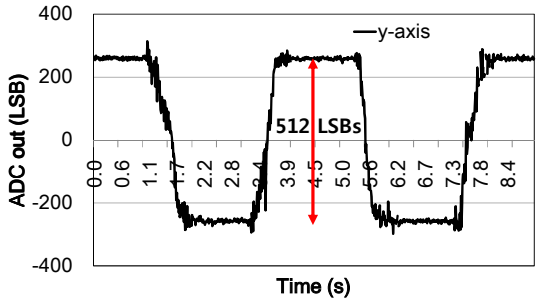
offset errors of three axes are set to be -4.8 LSB, -3.2 LSB and -4.75 LSB, respectively. The output offset with respect to the digital input of DECC is shown in Fig. 10. The DECC can calibrate the output offset with the resolution of 12.5 LSB/step.

Because the total output sensitivity is 256 LSB/g and the mechanical sensitivity of the MEMS sensing element is 6 fF/g, the capacitive sensitivity of the readout circuit is calculated to be 32 LSB/fF ((256 LSB/g) / (8 fF/g)). Therefore, the offset calibration resolution of 12.5 LSB/step is equivalent to 0.39 fF/step ((12.5 LSB/step)/ (32 LSB/fF)). This results means that the DECC can calibrate the output offset in sub-fF resolution.

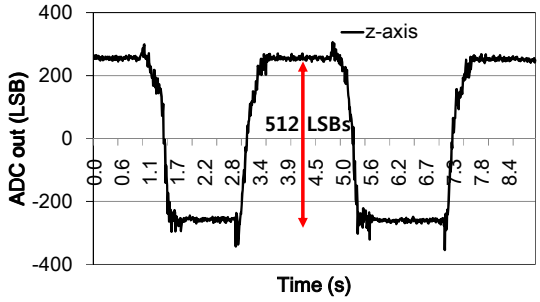
The output data rate is 2 kHz per axis. The measured



(a) x-axis output with ±1 g flip.



(b) y-axis output with ±1 g flip.



(c) z-axis output with ±1 g flip.

Fig. 9. Tri-axes accelerometer outputs at ±1g gravity acceleration input.

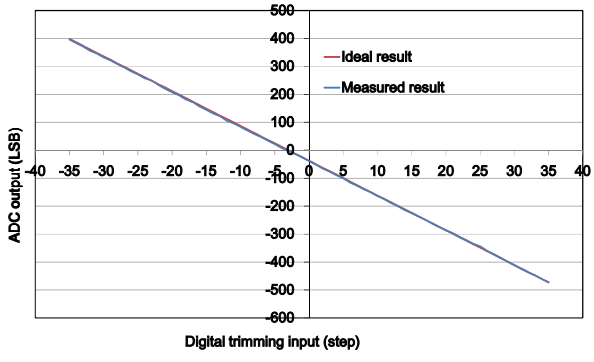


Fig. 10. Output offset with digital input of DECC.

noise levels of the x-, y- and z-axes are 349 μg/√Hz, 341 μg/√Hz and 411 μg/√Hz, respectively.

V. CONCLUSIONS

The highly precise readout circuit for capacitive tri-axes microaccelerometer is presented. The CSA with CDS and DECC can achieve both low power and high accuracy while maintaining low power consumption and a small area. The DECC using 10-bit DAC, charge transfer switches, and a charge-storing capacitor can realize the equivalent capacitance of sub-fF range for compensating the offset by capacitance mismatch with a smaller area and higher accuracy than previous methods. After the PGA adjusts the gain of microaccelerometer, its sensitivities of the tri-axes are measured to be 3.87 mg/LSB, 3.87 mg/LSB and 3.90 mg/LSB, respectively. The offset calibration, controlled by 10-bit DECC, has a resolution of 12.5 LSB per step with high linearity, and it results in setting the offset error to be -4.8 LSB, -3.2 LSB and -4.75 LSB, respectively. The noise levels of the tri-axes are 349 μg/√Hz, 341 μg/√Hz and 411 μg/√Hz.

REFERENCES

[1] W. Bracke, P. Merken, R. Puers and C. Van Hoof, "On the optimization of ultra low power front-end interfaces for capacitive sensors," *Sensors and Actuators A: Physical*, Vol.117, No. 2, pp.273-285, Jan., 2005.

[2] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of IEEE*, Vol.84, No.11, pp.1584–1614, Nov., 1996.

[3] J. Chen, X. Ni and B. Mo, "A low noise CMOS charge sensitive preamplifier for MEMS capacitive accelerometer readout," *ASIC, 2007. ASICON '07, 7th International Conference on*, pp.490-493, Oct., 2007.

[4] M. Lemkin and B.E. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *Solid-State Circuits, IEEE Journal of*, Vol.34, No.4, pp.456-468, Apr.,1999.

[5] H. Ko and D. Cho, "Low noise accelerometer microsystem with highly configurable capacitive interface," *Analog Integrated Circuits and Signal Processing*, Vol. 67, No.3, pp.365-373, June, 2011.

[6] H. Rodjegard and A. Loof, "A differential charge-transfer readout circuit for multiple output capacitive sensors," *Sensors and Actuators A*, Vol.119, No.2, pp.309-315, Apr., 2005.

[7] H. Ouh, et al., "Sub-fF trimmable readout circuit for tri-axes capacitive microaccelerometers," *Sensors, 2012 IEEE*, pp.1-4, Oct., 2012.

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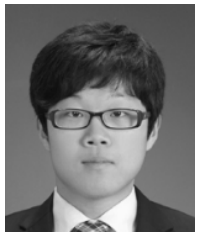

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