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A Nano-power Switched-capacitor Voltage Reference Using MOS Body Effect for Applications in Subthreshold LSI

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***Abstract*—A nano-power CMOS voltage reference is proposed in this paper. Through a combination of switched-capacitor technology with the body effect in MOSFETs, the output voltage is defined as the difference between two gate-source voltages using only a single PMOS transistor operated in the subthreshold region, which has low sensitivity to the temperature and supply voltage. A low output, which breaks the threshold restriction, is produced without any subdivision of the components, and flexible trimming capability can be achieved with a composite transistor, such that the chip area is saved. The chip is implemented in 0.18 μm standard CMOS technology. Measurements show that the output voltage is approximately 123.3 mV, the temperature coefficient is 17.6 ppm/°C, and the line sensitivity is 0.15 %/V. When the supply voltage is 1 V, the supply current is less than 90 nA at room temperature. The area occupation is approximately 0.03 mm^2.**

***Index Terms*—CMOS voltage reference, low power, low output, subthreshold, switched-capacitor, body effect**

I. INTRODUCTION

Interest in subthreshold CMOS circuits with power supply voltages below V_{th} (the transistor threshold voltage when other effects are neglected) is growing because reducing the operating voltage can effectively achieve ultra-low-power dissipation [1-4]. For these circuits, the reference voltage decreases as the supply voltage is reduced. Hence, a voltage reference (VR) that produces a low output voltage ($< V_{th}$) and consumes power in the sub-μW range is required. However, few studies have been explored to meet such requirements in VRs. Several reported VRs use only MOSFETs and allow for nano-power consumption [5-8]. The outputs of these VRs are above the threshold voltage while the V_{th} of the MOS diodes are used as the absolute voltage reference source. When process variations are considered, a low enough temperature coefficient (T.C.) and accuracy of the output voltage are not sufficient because the trimming procedures are not implemented for these structures.

Resistive dividers are commonly used to achieve low output ($< V_{th}$) [9-11]. However, operation is difficult with nano-power dissipation because a trade-off between the design area and power consumption (low current requires large resistor) always exists, the resistor network required for trimming implementation occupies a large area of the chip.

Recently, several solutions employ two devices with different V_{th} values to achieve a low output [12-14]. Because the bandgap reference source is used in [12], the output voltage is larger than the threshold voltage, and the power dissipation is still high because resistors are used. In [13, 14], ultra-low-power dissipation can be achieved. However, these designs require a process with multiple-V_{th} values. The output voltage depends entirely

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on the V_{th} difference from two distinct devices. Thus, the value is constrained by the process technology chosen, and the impact of process variations is increased.

A new method for the design of a low reference voltage ($< V_{th}$) through the use of the body effect in MOSFETs is proposed in [15]. Fig. 1 shows the circuit by which a VR with low T.C. can be implemented by using the reverse-bias body effect in transistor M1. The output voltage (V_{ref}), which is based on the difference between the two gate-source voltages ($V_{ref} = V_{sg1} - V_{sg2}$), is independent of V_{th}. However, the typical structure has the following drawbacks: the supply current remains large (1.2 μA); and the output suffers from the offset of the amplifier; the performance is degraded when the value of the resistor varies with the process, the large resistor occupies more chip area; the output voltage and the T.C. are subject to component mismatches and deviations resulting from process variations; the deviations and the mismatches are not well discussed, and the trimming procedures are not considered.

Generally, the switched-capacitor (SC) technique is popular for the design of bandgap VRs [16-18] because of the following advantages [19]: the offset of the amplifier can be canceled; instead of two transistors, only one transistor is used to generate the output voltage, thereby reducing the chip area and avoiding mismatch between transistors; the capacitors match better and occupy less area; and the low current does not require large resistors. A CMOS-based switched-capacitor voltage reference (SCVR) [20] is proposed to improve the design in [6]. Low output is produced through capacitive subdivision instead of the resistive subdivision used in [11], and nano-power dissipation can be achieved. The trimming capacitors can be adjusted for process variations to obtain a low T.C.. However, this operation conventionally requires three capacitors, and the capacitive subdivision requires a large value. Thus, this operation occupies more chip area. Therefore, a method that combines the SC-based technology with the body-biasing technology in MOSFETs is explored in this paper to solve the aforementioned problems. Low output ($< V_{th}$) is produced and can be scalable with standard CMOS technology, and the method achieves power and area savings. The remainder of this paper is organized as follows: Section II describes the operating principle of the proposed SCVR. In Section III, implementation of the circuit is presented. Considerations for this design and simulations are discussed in Section IV, and measurement results are demonstrated in Section V. Finally, Section VI provides the conclusions.

II. Operating Principles of Proposed SCVR Circuit

The proposed SCVR circuit shown in Fig. 2 is based on a sample and hold structure [19]. The circuit is composed of a bias current circuit, a core circuit, switched capacitors, and an operational trans-conductance amplifier (OTA). The switches S_{W1}-S_{W8} are controlled by non-overlapping clock signals (Φ_1, Φ_2, Φ_3, Φ_4, Φ_5). The core circuit inputs two different gate-source voltages (and V''_{sg1}) in M1 to the OTA during $\Phi_1 = 1$ and $\Phi_2 = 1$, respectively. If the clock signals Φ_1 and Φ_2 overlap, M1 will be biased at a state where the body of

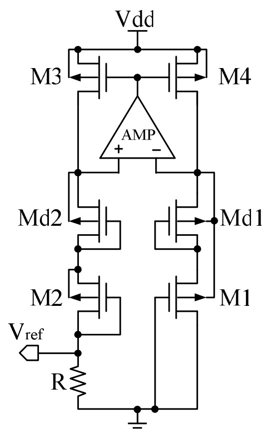


Fig. 1. Prior art: VR using the body effect in MOSFETs [15].

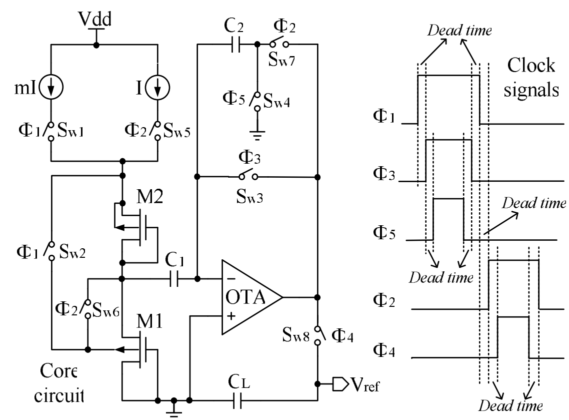


Fig. 2. Proposed SCVR using MOS body effect.

M1 is connected to its source and to the source of M2 during the overlap. As a result, an invalid gate-source voltage of M1 will be stored in C_1 and the invalid voltage will degrade the accuracy of the reference voltage because the reference voltage appears during $\Phi_2 = 1$. Meanwhile, more power will be dissipated during the overlap. Hence, the dead time between Φ_1 and Φ_2 is necessary to ensure accurate output and to preserve power dissipation. Φ_3 is designed to turn off the switch before Φ_1 so that the stored voltage in capacitor C_1 will be immune to the input-dependence charge injection from the switch; In addition, Φ_5 should be turned off before Φ_3 to avoid charge injection and storage on capacitors C_1 and C_2.

The dead-time region between Φ_2 and Φ_4 prevents the accuracy of V_{ref} from being impacted by the charge injection effect.

The equivalent structure of the proposed SCVR circuit is presented in Figs. 3(a) and (b). During the sampling state ($\Phi_1 = 1$ and $\Phi_2 = 0$), the PMOS transistor M1 is biased at mI (m is the ratio between the two different currents), and a gate-source voltage V'_{sg1} is stored in capacitor C_1. Capacitor C_2 is connected to the ground. During the hold state ($\Phi_1 = 0$ and $\Phi_2 = 1$), M1 is biased at I and another gate-source voltage is provided as input to C_1, while C_2 is connected to the output to form a negative feedback loop. The charges (and ΔQ_2) on each capacitor in terms of the offset voltage V_{off} of the OTA are given by Eqs. (1) and (2)

$$\begin{aligned}\Delta Q_1 &= C_1\left(V'_{sg1} - V_{off}\right) - C_1\left(V''_{sg1} - V_{off}\right)\\ &= C_1(V'_{sg1} - V''_{sg1})\end{aligned} \quad (1)$$

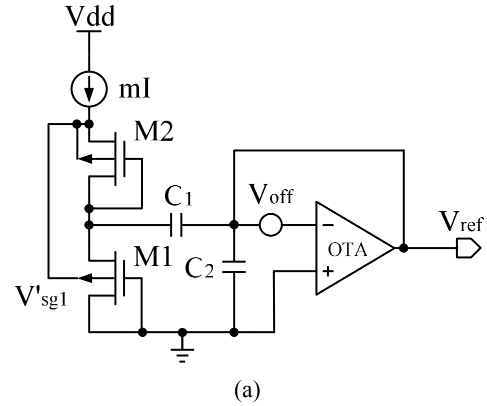
$$\Delta Q_2 = C_2\left(-V_{off}\right) - C_1\left(V_{ref} - V_{off}\right) = -C_2 V_{ref} \quad (2)$$

From the equations, V_{off} can be eliminated by storing the capacitors, which is auto-zeroing technology. According to the law of conservation of charge, the charges must be equal to each other

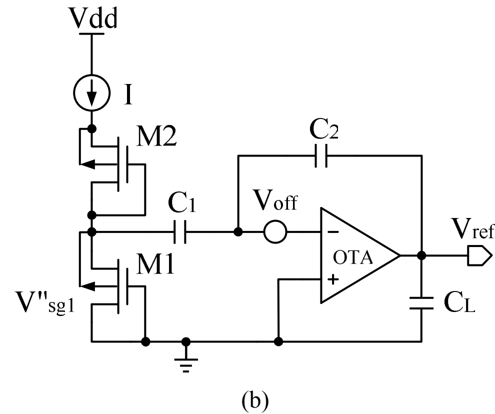
$$\Delta Q_1 + \Delta Q_2 = 0 \quad (3)$$

From Eqs. (1) and (2), the output voltage can be expressed as

$$V_{ref} = \frac{C_1}{C_2}(V'_{sg1} - V''_{sg1}) \quad (4)$$



(a)



(b)

Fig. 3. Equivalent schematic of the proposed SCVR circuit (a) when $\Phi_1 = 1$ and $\Phi_2 = 0$, (b) when $\Phi_1 = 0$ and $\Phi_2 = 1$.

The load capacitor C_L, which is usually off-chip [16-18, 20], ensures that the output is valid during the sampling period. The control circuit of the switches for the non-overlapping clock signals is presented in Figs. 4(a) and (b). The operation is shown in Fig. 5. The result is the difference between the two gate-source voltages (ΔV_{sg}) of M1 during the two phases.

The gate-source voltage V_{sg} of the PMOS transistor in the subthreshold region can be expressed as ($V_{sd} > 4V_T$)

$$V_{sg} = V_{th} + nV_T \ln\left[\frac{I_D}{KI_t}\right] \quad (5)$$

$$I_t = \mu_p (n-1) C_{ox} V_T^2 \quad (6)$$

where I_D is the drain current, n is the subthreshold slope factor, V_T (= kT/q, where k is Boltzmann's constant) is the thermal voltage, K (= W/L) is the aspect ratio of the transistor, C_{ox} is the oxide capacitance per unit area, and μ_p is the hole mobility.

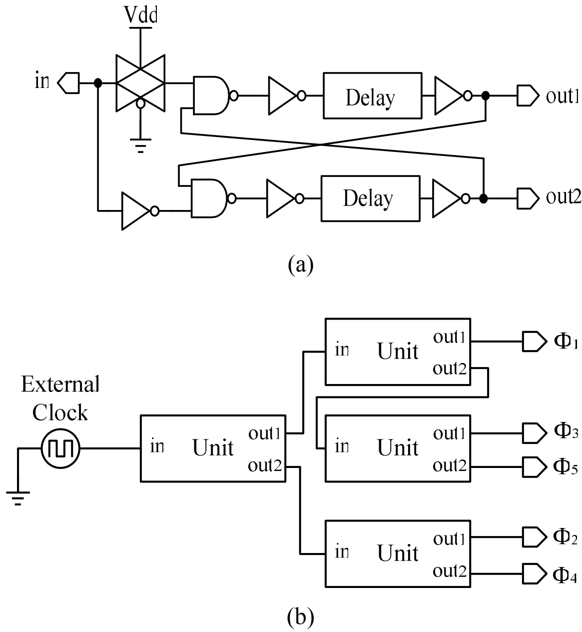


Fig. 4. Control circuit for switches (a) The non-overlapping clock unit, (b) The whole circuit for the clock signals.

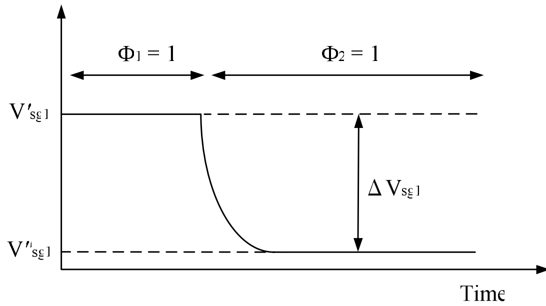


Fig. 5. Gate-source voltage of M1 during the two phases.

As shown in Figs. 3 and 5, the body of M1 is connected to the source of M2 during the sampling state ($\Phi_1 = 1$) to form a reverse-bias connection; thus, V'_{sg1} is defined as

$$V'_{sg} = V'_{th1} + nV_T \ln\left[\frac{mI}{K_1 I_t}\right] \tag{7}$$

$$V'_{th1} = V_{th0} + \gamma(\sqrt{2\Phi_B + V_{bs1}} - \sqrt{2\Phi_B}) \tag{8}$$

where V_{th0} is the threshold voltage when $V_{bs1} = 0$, γ is the body-effect coefficient, Φ_B is the Fermi potential, and V_{bs1} is the source-substrate voltage of M1. During the hold state ($\Phi_2 = 1$), V''_{sg1} can be given by

$$V''_{sg} = V''_{th1} + nV_T \ln\left[\frac{I}{K_1 I_t}\right] \tag{9}$$

$$V''_{th1} = V_{th0} \tag{10}$$

With Eqs. (7) to (10) and $V_{bs1} = V_{sg2}$, Eq. (4) can be presented as

$$V_{ref} = \frac{C_1}{C_2}\left[\gamma\left(\sqrt{2\Phi_B + V_{sg2}} - \sqrt{2\Phi_B}\right) + nV_T \ln(m)\right] \tag{11}$$

$$V_{sg2} = V_{th2} + nV_T \ln\left[\frac{mI}{K_2 I_t}\right] \tag{12}$$

In Eq. (11), the first term inside the square brackets is complementary to the absolute temperature (CTAT) and achieves a negative T.C. [15]. The second term is proportional to the absolute temperature (PTAT) and implements a positive T.C.. Because of the body-biasing effect from the bias voltage V_{sg2}, the CTAT term is achieved with two distinct threshold voltage levels (and). Therefore, the absolute value of V_{th0} in V_{ref} is canceled. Under the assumption that $C_1 = C_2$, a low output voltage ($V_{ref} < V_{th0}$) is obtained.

The proposed SCVR has advantages as follows: The operation only requires two capacitors (C_1 and C_2), whereas other SCVRs require more [18, 20]. Based on Eqs. (4) and (11), the low output does not require capacitive subdivision; furthermore, the ratio C_1/C_2 can be used to determine the scale of the output. The reference voltage is implemented with only one transistor (M1) in the standard process, such that the component matching errors are decreased, and the chip area is saved. The input offset of the amplifier can be canceled. The bias currents only require nano-ampere levels because M1 and M2 work in the subthreshold region, and the current ratio m can be selected to obtain a zero T.C., as demonstrated in the next section.

III. IMPLEMENTATION OF PROPOSED SCVR CIRCUIT

Fig. 6 shows the proposed SCVR circuit composed of the start-up circuit, the bias current circuit, the core circuit, and the OTA.

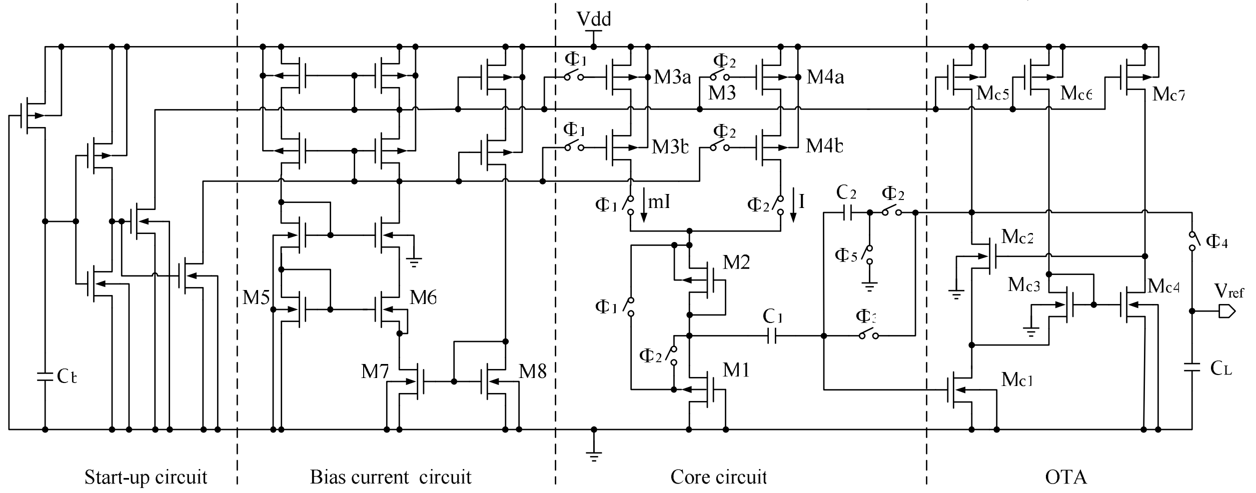


Fig. 6. Proposed switched-capacitor voltage reference circuit.

1. Nano-ampere Bias Current Circuit

The cascode current-bias circuit [21] can generate a nano-level current that is insensitive to technology, temperature, and supply voltage; thus, low-power dissipation can be ensured. Transistors M5 and M6 operate in the subthreshold region, whereas M7 and M8 work in the linear region and the saturation region, respectively. Current mirrors in the cascode structure improve line sensitivity; however, the structure increases the minimum supply voltage. For the subthreshold operation in current mirrors and the saturation operation in M8, the minimum supply voltage must ensure $V_{sd} > 4V_T$ and $V_{gs8} > V_{th8}$. Thus, the minimum supply voltage can be redistributed as the sum of two drain-source voltages V_{ds} and a gate-source voltage V_{gs8} in the branches of the circuit ($Vdd > V_{th8} + 8V_T$).

2. Control of T.C.

The core circuit consists of transistors M1 and M2, switches, and capacitors. The zero T.C. is satisfied by

$$\frac{\partial V_{ref}}{\partial T}|_{T=T_0} = 0 \tag{13}$$

where T_0 is room temperature. Thus, the temperature dependence of the SCVR can be obtained by differentiating Eq. (11) with respect to temperature and can be given by

$$\frac{C_1}{C_2}\left\{\frac{1}{2}\gamma\left[\left(2\Phi_B(T_0)+V_{sg2}(T_0)\right)^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}+\frac{\partial V_{sg2}}{\partial T}\right)\right.\right.$$
$$\left.\left.-\left(2\Phi_B(T_0)\right)^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}\right)\right]+n\frac{V_T}{T}\ln(m)\right\}=0 \tag{14}$$

In this work, the T.C. of Φ_B is approximately -0.7 mV/°C , the T.C. of V_{sg2} is approximately -1.25 mV/°C, Φ_B is approximately 0.35 V, γ is approximately 0.5 $\sqrt{\text{V}}$, n is approximately 1.2, and V_{sg2} is approximately 0.31 V. For Eq. (14), the first term in the brace has a negative T.C., whereas the thermal voltage V_T has a positive T.C. (≈ 0.087 mV/°C) [22] in the second term. Hence, a zero T.C. can be achieved by choosing an adaptive biased-current ratio m that is the size ratio between M3a (M3b) and M4a (M4b). With the value of the parameters in Eq. (14), the value of m can be calculated from

$$m=\exp\left\{\frac{\gamma T}{2nV_T}\left[2\Phi_B(T_0)^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}\right)\right.\right.$$
$$\left.\left.-\left(2\Phi_B(T_0)+V_{sg2}(T_0)\right)^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}+\frac{\partial V_{sg2}}{\partial T}\right)\right]\right\} \tag{15}$$

3. OTA Circuit

The OTA [23] consists of the transistors M_{o1}-M_{o7}. The input offset resulting from asymmetries and process variations is canceled by the use of the switched-

capacitor network. The transistors M_{o1} and M_{o2} form the cascode amplifier, and M_{o3} and M_{o4} constitute the feedback loop to increase the output impendence and boost the gain of the OTA, thereby enhancing the precision and speed of the switched-capacitor amplifier. The OTA can be operated with a nano-current supply. From simulations, the gain of the OTA is approximately 70 dB when Vdd = 1 V at room temperature.

IV. DESIGN CONSIDERATIONS AND SIMULATIONS

1. Charge Injection Effects and Clock Feed-through

The switched-capacitor circuit suffers from charge-injection errors and clock feed-through, which influences the precision. The priori method is the transmission gate at the switch [22]. The charge injection and clock feed-through effects can be effectively eliminated with the complementary structure because the opposite charge packets (holes and electrons) injected from the PMOS and NMOS cancel each other, and the on-resistance in the switch can be reduced to achieve high-speed operation.

2. Operational Clock Frequency

For SC circuits, the output is not valid in one phase because of the discrete-time nature of these circuits; the solution is to use an output filter capacitor. However, a droop of the output voltage across the load capacitor is caused by leakage current that mainly consists of the switch leakage current and bias current of amplifier. Thus, a ripple always exists at the output. The value of the ripple (V_{ripple}) is expressed by [24]

$$V_{ripple} = \frac{I_{leak}}{C_L f_{clk}} \tag{16}$$

where I_{leak} is the leakage current that flows in or out of the hold capacitor when the sampled and hold amplifier is in hold mode, and f_{clk} is the clock frequency. There is a trade-off between the clock frequency and power consumption; the lower the frequency, the less the power dissipated. However, lower frequency can result in larger voltage ripples and can degrade the accuracy of the output voltage according to Eq. (16). Hence, the operational frequency must not be too small. With our design used in analog-digital converter (ADC) [4], the output voltage is not allowed to droop by more than 1/2 LSB. With a large leakage current at 80 °C, the transient analysis is simulated to evaluate the performance, as shown in Fig. 7. The ripple is approximately 0.5 mV with a 100 pF output capacitor when the clock frequency is 1 kHz.

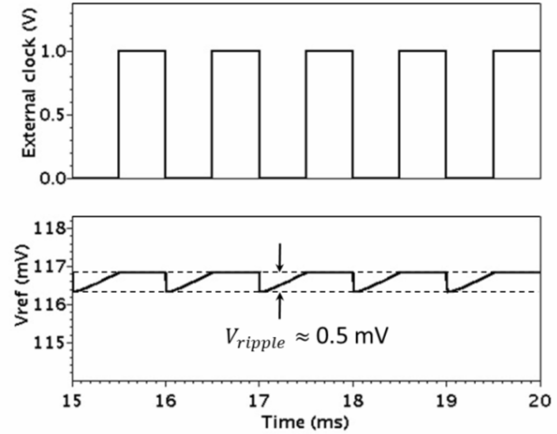


Fig. 7. Simulated output waveforms when C_L is 100 pF at 80 °C.

3. Process Variations and Trimming

Process variations are generally distinguished between within-die (WID) variations and die-to-die (D2D) variations [7]. WID variations (e.g., σV_{th}, $\sigma W/L$) cause mismatch between transistors of the same chip and influence the relative accuracy of the transistor parameters, whereas D2D variations (e.g., ΔV_{th}, $\Delta W/L$) influence the absolute accuracy of the transistor parameters. For the core circuit in this study, the influence of WID variation (V_{th}) decreases because only one transistor is used for the voltage reference generator. The zero T.C. is primarily determined by the size ratio between M3a (M3b) and M4a (M4b); thus, the mismatch of W/L ($\sigma W/L$) between transistors results from WID variations. This effect can be effectively reduced because of the careful layout techniques and large sizes of transistors [22].

However, D2D variations cannot be avoided. The influence of ΔV_{th} is dominant because V_{th} is poorly controlled in a manufacturing environment. As shown in Eq. (12), V_{sg} suffers from ΔV_{th} because of process

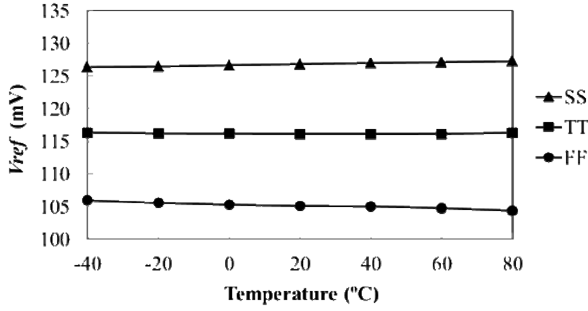


Fig. 8. Simulated V_{ref} as a function of temperature at different corners. TT: typical PMOS/typical NMOS; SS: slow PMOS/slow NMOS; FF: fast PMOS/fast NMOS.

variations. Thus, according to Eqs. (11) and (14), the process variations result in spreads in the output voltage and in the T.C.. In particular, the T.C. is more significantly impacted. To investigate the impact, Fig. 8 shows the simulated results for the T.C. when Vdd = 1.5 V and $C_1 = C_2$ = 600 fF. Because $V_{th}(S) > V_{th}(T) > V_{th}(F)$, $V_{sg2}(S) > V_{sg2}(T) > V_{sg2}(F)$ at room temperature T_0 for M2. Thus, from Eqs. (14) and (15), if the adaptive size ratio m between M3a (M3b) and M4a (M4b) is set to achieve a zero T.C. for TT, then the absolute value of the negative T.C. is equal to that of the positive T.C.. For SS, $V_{sg2}(S)$ causes a decrease in the value of the negative T.C. in accordance with Eq. (14), such that the absolute value of the negative T.C. is smaller than that of the positive T.C., and the output voltage shows a positive temperature variation. Conversely, $V_{sg2}(F)$ leads to an increase in the value of the negative T.C., such that the absolute value of the negative T.C. is larger than that of the positive T.C. for FF, and the output voltage exhibits a negative temperature dependence. Therefore, current trimming (changing the T.C. of the PTAT term) is used to correct the slope (compensate for the T.C. variation in the CTAT term); thus, the size ratio m should be adjustable after chip fabrication. One solution is the use of a composite transistor [25], Fig. 9(a) presents the trimming network. The trim range and the resolution are determined from the simulations shown in Fig. 8. The aspect ratios of M3a and M3b can be changed by digital logic control to adjust the T.C., as shown in Fig. 10. The solid lines show the temperature characteristics for the typical code of "111000" (S_1 to S_6: 111000, where "1" indicates that the switch turns on, whereas "0" means the switch turns off). The trimming performance is shown by the dashed lines in Fig. 10. For SS, the temperature characteristics have a negative variation with the lowest code of "000000," and the temperature characteristics for FF have a positive variation with the highest code of "111111." Hence, the resolution of 2% is enough for adjustment to obtain a zero T.C. within the range of variation because SS and FF are the worst cases in this process, and the spread of V_{ref} is also minimized. The adjustable range of m has little impact on the power dissipation and the signal-to-noise ratio because the bias circuit generates a bias current of several nano-amperes.

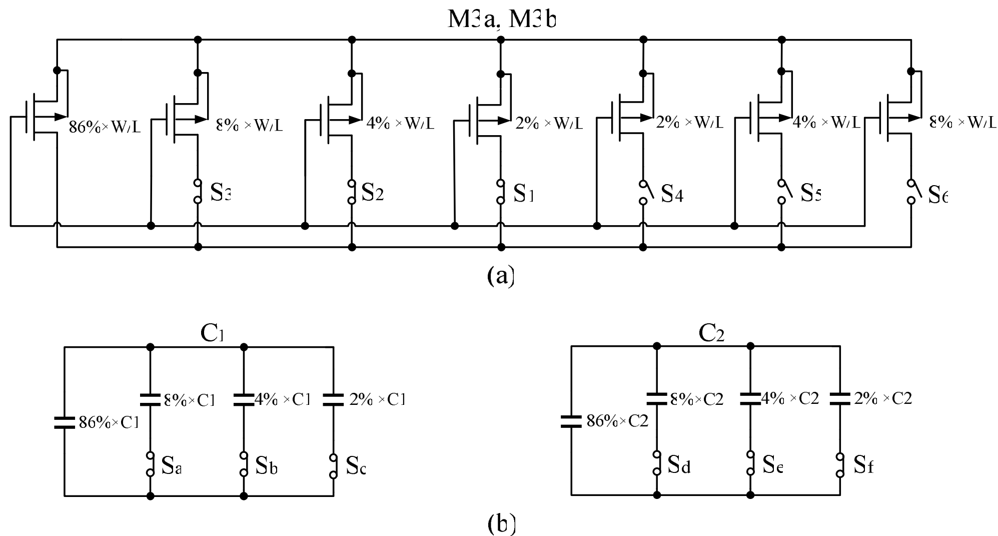


Fig. 9. (a) Composite structure in M3a and M3b for trimming, (b) implementation of scalable output for C_1 and C_2.

Table 1. Programmable outputs by digital code S_a to S_f

S_a	S_b	S_c	S_d	S_e	S_f	V_{ref} (mV)
0	0	0	1	1	1	99.8
0	0	1	1	1	1	102.2
0	1	0	1	1	1	104.5
0	1	1	1	1	1	106.8
1	0	0	1	1	1	109.1
1	0	1	1	1	1	111.5
1	1	0	1	1	1	113.8
1	1	1	1	1	1	116.1
1	1	1	1	1	0	118.5
1	1	1	1	0	1	120.9
1	1	1	1	0	0	123.5
1	1	1	0	1	1	126.2
1	1	1	0	1	0	129.0
1	1	1	0	0	1	131.9
1	1	1	0	0	0	135.0

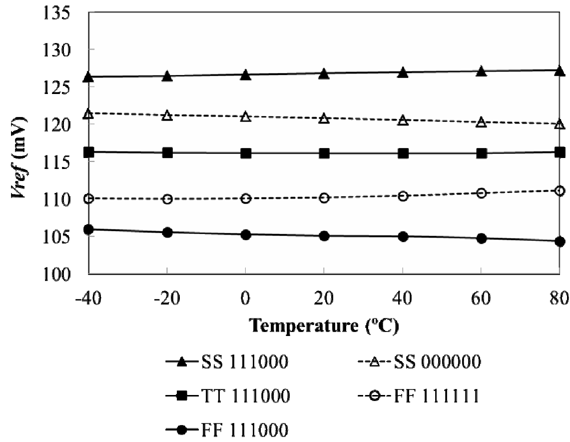


Fig. 10. Simulated corner analysis under different code conditions.

Based on Eq. (11), the programmable outputs can be implemented by adjusting the ratio between C_1 and C_2; the method can also effectively reduce the output voltage spread. Fig. 9(b) shows such an adjustment with 2% resolution. Six digital control bits are used to satisfy the requirement of increasing or decreasing the output value. Table 1 shows the simulated programmable outputs for TT at room temperature, the value is scalable from 99.8 mV to 135.0 mV by changing the ratio between C_1 and C_2.

In our work, the purpose of the trimming process is to obtain the zero T.C. as well as the minimum output spread. The detailed trimming procedures are as follows. First, the circuit is fabricated with the typical trimming code for the initial state; then, the voltage reference is measured from -40 °C to 80 °C in 20 °C intervals. With these collected data, the T.C. is obtained. If the T.C. is not equal to zero because of process variations; then, the T.C. curve has a slope S_p. From Eq. (14), the slope S_p can be defined as

$$S_p = \frac{C_1}{C_2}\left[N + n\frac{V_T}{T} ln(m) \right] \tag{17}$$

where

$$N = \frac{1}{2}\gamma\left[\left(2\Phi_B(T_0) + V_{sg2}(T_0)\right)^{-\frac{1}{2}} \left(2\frac{\partial\Phi_B}{\partial T} + \frac{\partial V_{sg2}}{\partial T} \right) - \left(2\Phi_B(T_0)\right)^{-\frac{1}{2}} \left(2\frac{\partial\Phi_B}{\partial T} \right) \right]$$

To obtain the zero T.C., m should be adjusted to compensate for the slope; then, Eq. (17) is expressed by

$$\frac{C_1}{C_2}\left[N + n\frac{V_T}{T} ln(m + \Delta m) \right] = 0 \tag{18}$$

where Δm is the required range for trimming. The n and T.C. of V_T are assumed to have minimal sensitivity to the process variation, and capacitors are assumed to match very well. With Eqs. (17) and (18), the required trimming code can be calculated by

$$\frac{\Delta m}{m} = exp\left(-\frac{C_2 S_p q}{C_1 nk} \right) - 1 \tag{19}$$

After obtaining the zero T.C., the output voltage spread can be reduced by changing the ratio between C_1 and C_2.

NMOS transistors are used as switches (S_1 to S_6, S_a to S_f). In production lines, one-time-programmable (OTP) memories such as fuses can be used to control the switches with minimal power consumption [26].

4. Effects from Noise

The noise performance should be considered in the SCVR circuit. The most critical noise sources are the non-zero resistance switches, the active transistors inside the OTA, and the noise induced by the clocks. The high-frequency noise is folded back into the signal's baseband in sampled data networks clocked at the same frequency

as f_{clk} because of fold effects in sampled noise [27],

For OTA, thermal noise can be reduced by designing a large trans-conductance $g_{m(o1)}$ in M_{o1} and a small trans-conductance $g_{m(o5)}$ in M_{o5} because the noise is proportional to $g_{m(o5)}/g_{m(o1)}$ [22]. The use of transistors with large widths and lengths can decrease flicker noise.

For the switches S_{W1}-S_{W8} shown in Fig. 2, the noise analysis is as follows. During the sampling mode (Φ_1 = 1), the switches S_{W1}, S_{W2}, S_{W3} and S_{W4} turn on; thus, the contributor of the noise is the on-resistors of the switches S_{W1}, S_{W2}, S_{W3} and S_{W4}. Then, the total input–referred noise variance is sampled by the capacitors C_1 and C_2, which can be expressed by [22]

$$V_{ni}^2 = \frac{kT}{C_1} + \frac{kT}{C_2} \tag{20}$$

With the closed-loop gain in OTA (A_{cl} = $-C_1/C_2$), during hold mode (Φ_2 = 1), the total output noise variance contributed by the switches S_{W1}, S_{W2}, S_{W3} and S_{W4} is given by

$$V_{no1}^2 = \frac{kT}{C_1} \bullet A_{cl}^2 + \frac{kT}{C_2} = \frac{kTC_1}{C_2^2} + \frac{kT}{C_2} \tag{21}$$

During the hold mode (Φ_2 = 1), the switches S_{W5}, S_{W6}, S_{W7} and S_{W8} turn on; thus, the noise is from the on-resistors R_5, R_6, R_7 and R_8 of the switches S_{W5}, S_{W6}, S_{W7} and S_{W8}, respectively. Fig. 11 illustrates the equivalent small signal model for noise analysis. C_{in} is the input parasitic capacitance, G_m is the trans-conductance of OTA, R_{out} is the output resistance, and V_{n5}, V_{n6}, V_{n7} and V_{n8} are the noise sources that model thermal noise of R_5, R_6, R_7 and R_8, respectively. The output noise variation due to R_8 is kT/C_L; then, the total output noise variance contributed by the switches S_{W5}, S_{W6}, S_{W7} and S_{W8} can be calculated by [28]

$$V_{no2}^2 = \left(\frac{kTRC_2^2}{C_1^2} + kTR_7 \right) B_w + kT\left[\frac{C_2 C_m}{C_L (C_L C_n + C_2 C_m)} \right] + \frac{kT}{C_L} \tag{22}$$

where $B_w = G_m C_2/(C_L C_n + C_2 C_m)$, with $C_m = C_1 + C_{in}$ and $C_n = C_2 + C_1 + C_{in}$, is the bandwidth of the circuit in Fig. 11 with $R_{out} >> (C_m + C_2)/C_2 G_m$, and $R = R_5 R_6/(R_5 + R_6)$. All on-resistors of switches are assumed to have the same

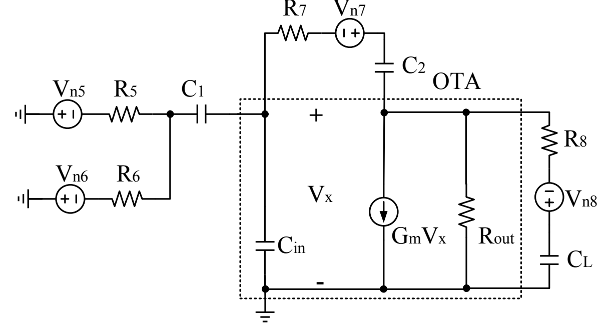


Fig. 11. Equivalent small signal model for noise analysis due to the switches S_{W5}-S_{W8}.

value. From Eqs. (21) and (22), with the folding effects, the total noise variance from the switches S_{W1}-S_{W8} can be expressed by [29]

$$V_{ntot}^2 = \left(V_{no1}^2 + V_{no2}^2 \right) \left(1 + \frac{2f_{on}}{f_{clk}} \right) \tag{23}$$

where f_{on} is the cutoff frequency of the switched-capacitor amplifier.

V. Measurement Results

The proposed SCVR circuit is fabricated in the CMOS 0.18 μm process. For this circuit, capacitors C_1 and C_2 are approximately 600 fF, Fig. 12 shows the chip micrograph, and the chip area is approximately 0.03 mm^2 . The clock frequency is 1 kHz, and the off-chip capacitor C_L used for the output filter capacitor is 100 pF. The measured output waveforms are shown in Fig. 13.

Fig. 14 shows the plot of the output voltage as a function of temperature (-40 °C to 80 °C) with the simulated and test results, the measured T.C. after trimming is approximately 17.6 ppm/°C at Vdd = 1.5 V, and the output voltage is approximately 123.3 mV. Additionally, the temperature characteristics of V_{ref} when the supply voltage ranges from 1 V to 3 V, are presented in Fig. 15. Based on the measurements at -40 °C , proper operation is obtained for $Vdd \geq 1$ V. The measurement line sensitivity is approximately 0.15 %/V when Vdd varies from 1 V to 3 V at room temperature. Fig. 16 shows a plot of the supply current as a function of temperature at different supply voltages, the supply current is approximately 90 nA at room temperature when Vdd is 3 V, and the operating currents of the biased

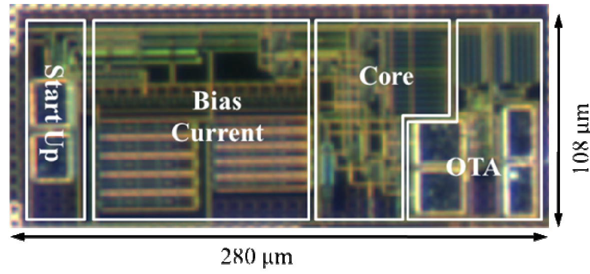


Fig. 12. Chip micrograph of the proposed SCVR.

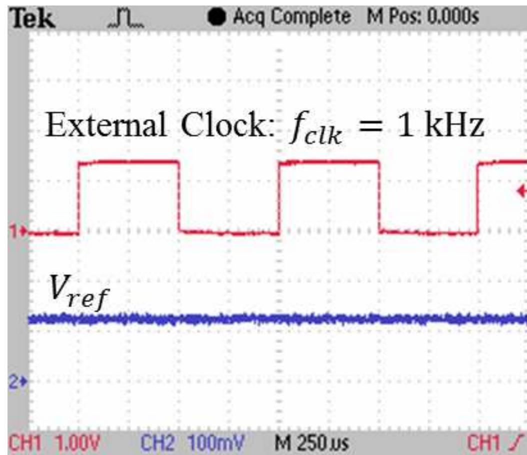


Fig. 13. Measured output waveforms of the proposed SCVR.

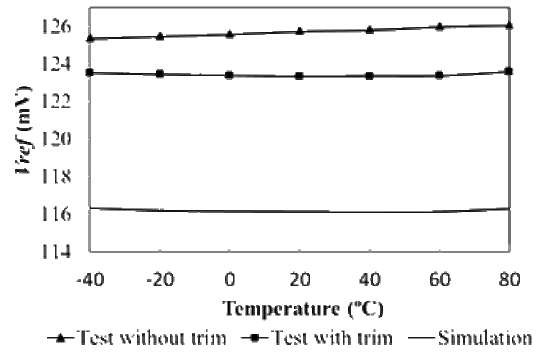


Fig. 14. Measured and simulated temperature dependence at Vdd = 1.5 V.

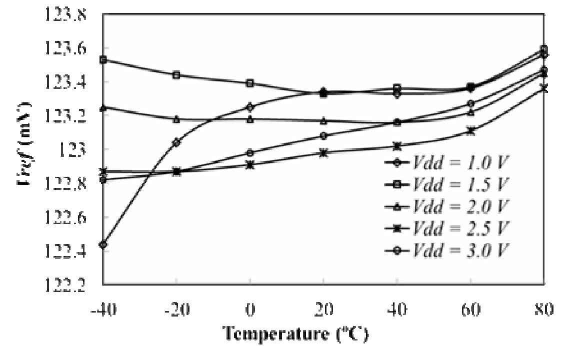


Fig. 15. V_{ref} as a function of temperature for different supply voltages.

Table 2. Comparison with other reported low-power CMOS voltage references

	This work	Ref [20]	Ref [11]	Ref [13]	Ref [14]
Process	0.18-μm	0.35-μm	0.35-μm	0.18-μm	0.13-μm
Threshold voltage (V)	V_{thp} = -0.383 V_{thn} = 0.459	V_{thp} = -0.7 V_{thn} = 0.55	V_{thp} = -0.75 V_{thn} = 0.45	V_{thp} = -0.456 V_{thn} = 0.33	N/A
Supply voltage (V)	1 to 3	1 to 4	1.5 to 4.3	0.45 to 2	0.5 to 3
Supply current @ room temperature	< 90 nA @ 1 V	250 nA @ 1 V	1200 nA @ 1 V	7 nA @ 0.45 V	59 pA @ 0.5 V
V_{ref} (mV)	123.3	190.1	168	257.5	176.1
T.C. (ppm/°C) Temp range (°C)	17.6 -40 to 80	16.9 -40 to 80	25 0 to 80	165 0 to 125	5.3-47.4 -20 to 80
Line sensibility (%/V)	0.15	0.76	0.95	0.44	0.036
Chip area (mm^2)	0.03	0.049	0.08	0.043	0.0093
Component subdivision	-	Capacitors	Resistors	-	-
Trimming components	Transistors Capacitors	Capacitors	Resistors	-	Transistors
Output voltage	Scalable	Scalable	Scalable	Constrained	Constrained
Device type	Standard	Standard	Standard	High-V_{th}	Native

circuit, the core circuit, and the OTA are approximately 15 nA, 30 nA, and 45 nA, respectively.

The measured results of the SCVR for the three trimmed samples are shown in Fig. 17. The average voltage variation is approximately 1 mV, and the T.C. from the three samples are 19.5 ppm/°C, 17.6 ppm/°C ,

and 15.6 ppm/°C, respectively.

The output noise spectrum is measured with a 100 pF output capacitor at room temperature, as shown in Fig. 18. The peak value is approximately 367 $\mu V / \sqrt{Hz}$ at 1 kHz.

Table 2 compares the proposed SCVR with other reported low-power CMOS VRs with low output (< V_{th}).

The results show that the SCVR circuit can be implemented in standard CMOS technology and that, low output, under threshold voltage, is achieved without using any component subdivision, and is scalable. The output voltage has satisfactory sensitivity to the temperature and supply voltage. The circuit also has advantages in nano-level power dissipation and compact silicon occupation.

VI. Conclusions

A CMOS switched-capacitor voltage reference with body biasing technology at subthreshold operation is proposed in this paper. The low output voltage, which is below the threshold voltage, can be achieved with standard technology and without using any component subdivision. In addition, the value can be made scalable. The T.C. is 17.6 ppm/°C, the line sensitivity is approximately 0.15 %/V, and the circuit consumes power at the nano-level and occupies a small area. The influences resulting from process variations can be effectively suppressed, and the proposed trimming procedure with a composite transistor improves the T.C. when the circuit suffers from D2D variations. The design can ensure a precise voltage reference for applications in subthreshold integrated circuits.

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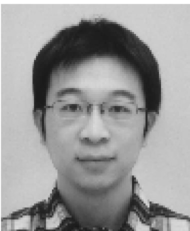

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