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Scaling Down Characteristics of Vertical Channel Phase Change Random Access Memory (VPCRAM)

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Abstract—**In this paper, scaling down characteristics of vertical channel phase random access memory are investigated with device simulator and finite element analysis simulator. Electrical properties of select transistor are obtained by device simulator and those of phase change material are obtained by finite element analysis simulator. From the fusion of both data, scaling properties of vertical channel phase change random access memory (VPCRAM) are considered with ITRS roadmap. Simulation of set reset current are carried out to analyze the feasibility of scaling down and compared with values in ITRS roadmap. Simulation results show that width and length ratio of the phase change material (PCM) is key parameter of scaling down in VPCRAM. Thermal simulation results provide the design guideline of VPCRAM. Optimization of phase change material in VPCRAM can be achieved by oxide sidewall process optimization.**

Index Terms—**Phase change RAM, scaling down, phase change material, finite element analysis**

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I. INTRODUCTION

A phase change random access memory (PCRAM) is one of the most promising candidates for next-generation high-density embedded nonvolatile memory [1, 2]. In the PCRAM, diode has been commonly used as a select device. However diode had leakage current problem with unselected cell. To avoid leakage current problem, metal oxide semiconductor field effect transistor (MOSFET) was applied to select device of PCRAM to reduce leakage current of unselected cell. However, the PCRAM with MOSFET has disadvantage in scaling down compared with PCRAM with diode. To reduce the unit cell size, we suggested a vertical channel PCRAM (VPCRAM) which have vertical channel and phase change material [3]. Since electrodes and phase change material were able to be patterned by self-aligned sidewall process, suggested structure ideally could reduce device area and fabrication steps. Furthermore, short-channel effects (SCEs) can be effectively suppressed, and a larger sensing margin is expected since the device channel length determined by the silicon trench height along the word ling (WL) direction can be simply controlled by anisotropic dry etch [4]. Fundamental electrical characteristics and disturbance characteristics were investigated in previous works [3, 4]. Scaling down characteristics of Si wall were investigated with device simulations in previous work [4]. However, most of the results in previous works were focused on the characteristics of select devices [5, 6]. In this paper, scaling down properties of PCM would be investigated and focused. Resistance of PCM is extracted from finite element simulation and that is applied to device

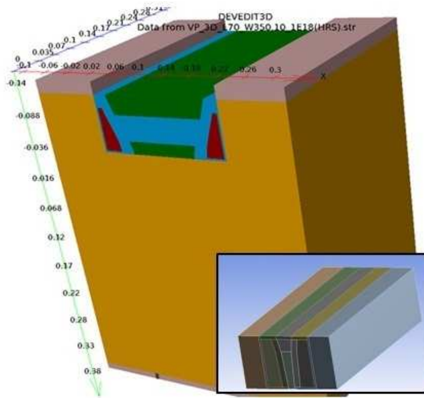


Fig. 1. Device simulation structure of VPCRAM with 90 nm effective channel length. Finite element analysis simulation structure for PCM resistance extraction (inset).

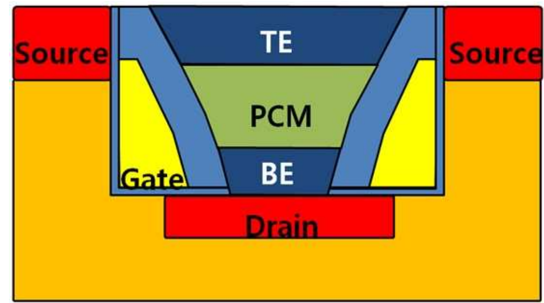
simulation.

II. SIMULATION STRUCTURE

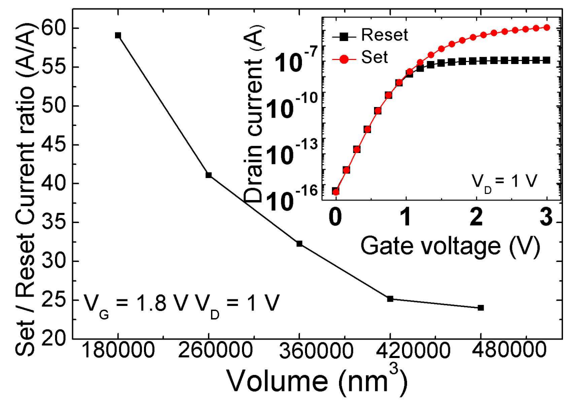
Fig. 1 shows the device structure of a VPCRAM. Select transistor of VPCRAM is based on the vertical channel MOSFET structure. The thickness of gate oxide and top oxide over the gate poly are 3 nm and 20 nm respectively. Gate in the VPCRAM is formed by using sidewall process. Gate isolating oxide on the each gate isolates gate from the electrodes and phase change material (PCM). Gate material is n+ poly silicon and PCM is $Ge_2Sb_2Te_5$ (GST) in this work [7]. The PCM in this work has low resistivity (42 mΩ•cm) state (SET) and the amorphous state has high resistivity(250 Ω•cm) state (RESET) respectively [4]. Doping concentration of substrate is 1×10^{18} cm^{-3} and that of source/drain is 1×10^{19} cm^{-3}.

III. RESULTS AND DISCUSSIONS

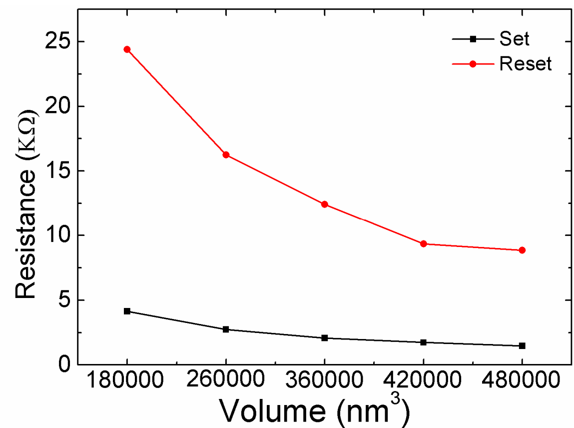
Scaling down of PCM in this work is separated in lateral direction and vertical direction. The structure of PCM and scaling down directions are introduced in Fig. 2(a). Since the PCM in VPCRAM uses deposition and etching process, lateral scaling of PCM width is determined by thickness of top oxide on the polysilicon gate. This is determined by oxidation process of gate polysilicon. Another direction of PCM scaling, vertical scaling is determined by etching process of PCM. In this paper, both of scaling direction properties are considered



(a)



(b)



(c)

Fig. 2. (a) Cross section of VPCRAM and scaling direction of PCM, (b) Lateral scaling of PCM with SET and RESET current ratio. Drain current characteristics with SET and RESET states (inset), (c) PCM resistances with lateral scaling down.

with fabrication feasibility. Memory operation of VPCRAM is shown in inset of Fig. 2(b). SET and RESET state are separated with resistance change and resistance is extracted by previous work. Different current level means separated state '0' and '1'. Current ratio between SET and RESET state means the margin of

data in VPCRAM. As shown in Fig. 2(b), lateral scaling of PCM is investigated with SET/RESET current ratio. As lateral size of PCM is decreased, total volume of PCM is decreased and SET/RESET current ratio is increased. PCM in the Fig. 2(b) has 40 nm height and 100 nm width. Volume is varied with top side length and bottom side length.

In the VPCRAM operation, atomic structure and resistivity of PCM is changed with thermal energy. Resistance is determined by resistivity (ρ) and length (l) and area of cross section (A) as shown in below equation.

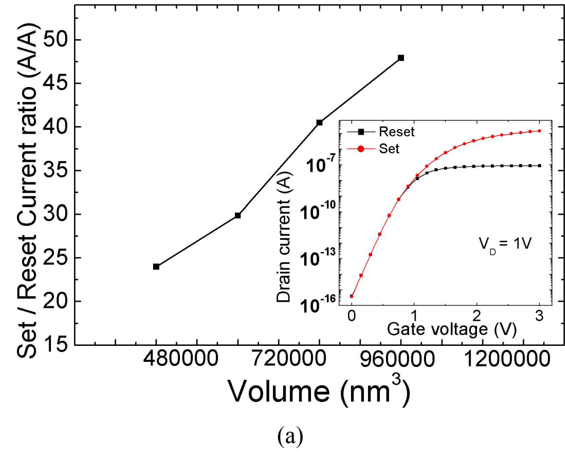
$$R= (\rho\times l)/A \quad (1)$$

Since the area of cross section is decreased, total resistance of PCM is increased with lateral scaling down. Furthermore resistance difference between SET and RESET states are also increased with lateral scaling down.

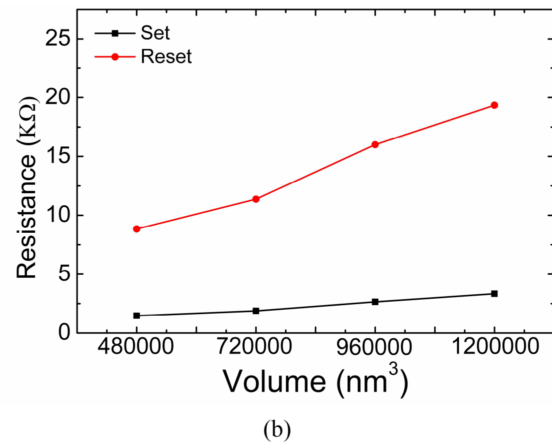
However, the vertical size scaling down of PCM has different characteristics. As shown in Fig. 2(a), vertical size means the thickness of PCM. The current ratio of VPCRAM with vertical scaling down has opposite characteristics compared with lateral scaling down. As shown in Fig. 3(a), SET/RESET current ratio of VPCRAM is decreased with PCM scaling down. This phenomenon is also explained with resistance of PCM. Vertical size of PCM is the length of PCM and this is directly related with resistance of PCM. PCM in the Fig. 3(a) has 100 nm width, and both top side length and bottom side length are varied with vertical scaling.

PCM resistance in SET state is one of the most important parameter in PCRAM. According to 2012 ITRS road map, SET state resistance of 2012 and 2013 is 2.6 and 3.1 k ohm respectively [8]. As shown in Fig. 2(c), SET resistance of ITRS road map is satisfied with PCM volume less than 260000 nm^2. Trench width between neighbor sources and top oxide thickness is key fabrication process parameter of SET resistance.

Furthermore, the temperature of PCM should be considered with PCM scaling down. Fig. 4 shows the maximum temperature of PCM with SET state. Maximum temperature data is extracted from finite element analysis simulation. Thermal conductivity Thermal conductivity of oxide is 1.4 $Wm^{-1}K^{-1}$ and that of TiW is 21.7 $Wm^{-1}K^{-1}$. Convection coeffieicnt is fixed at



(a)



(b)

Fig. 3. (a) Vertical scaling of PCM with SET and RESET current ratio. Drain current characteristics with SET and RESET state (inset), (b) PCM resistances with vertical scaling down.

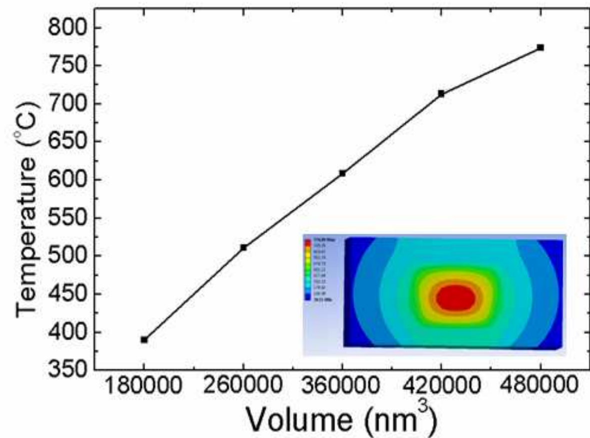


Fig. 4. Lateral scaling down property of PCM maximum temperature with SET state. Finite element simulation results of temperature distribution in PCM (inset).

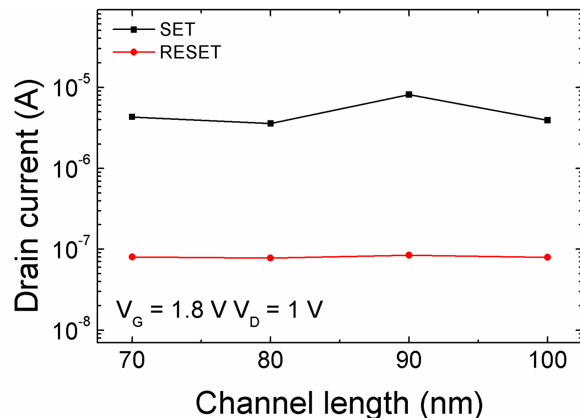


Fig. 5. SET and RESET current of VPCRAM with channel length variation when the volume of PCM is fixed.

2.0 x 10^7 W/m^2°C and all of thermal parameters were same with previous work [4]. Although the small volume PCM has high SET/RESET current ratio as shown in Fig. 2(b), small volume PCM can be suffer from low SET temperature. This result means that optimization of PCM volume should be carefully considered with electric properties and also temperature properties.

If volume of PCM is fixed and channel length is varied, the change of SET and RESET current characteristics are negligible as shown in Fig. 5. This data shows the effect of PCM volume change on the selective device. Due to the resistance differences between PCM and select MOSFET channel, effects of PCM are dominant in VPCRAM. Optimization of scaling down in VPCRAM, dependency of SET/RESET current ratio can be an important parameter.

IV. CONCLUSIONS

Scaling down propertied of VPCRAM is investigated with PCM scaling down. In the VPCAM, scaling of PCM has different characteristics with scaling direction of PCM. Lateral scaling of PCM increases SET/RESET current ratio which determine the margin of memory operation. However vertical scaling of PCM decreases SET/RESET ratio. The results mean that the height and the width of PCM should be carefully considered in VPCRAM scaling down. SET resistance of PCM is compared with ITRS roadmap 2012 data and possibility of device development is confirmed with simulation results. Channel length scaling down properties is also investigated but has negligible effect on SET/RESET ratio. Guideline of VPCRAM scaling down for device performance enhancement is suggested with PCM scaling down properties.

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Chun Woong Park photograph and biography not available at the time of publication.

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Woo Young Choi photograph and biography not available at the time of publication.

Dongsun Seo photograph and biography not available at the time of publication.

Cherlhyun Jeong photograph and biography not available at the time of publication.

Il Hwan Cho was born in Anyang, Korea, in 19772. He received the B.S. in Electrical Engineering from Korea Advanced Institute of Science and Technology(KAIST), Daejon, Korea, in 2000 and M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 2002, 2007, respectively. From March 2007 to February 2008, he was a Postdoctoral Fellow at Seoul National University, Seoul, Korea, where he was engaged in the research on characterization of bulk finfet SONOS flash memory. In 2008, he joined the Department of Electronic Engineering at Myongji University, Yongin, where he is currently an Associate Professor. His current research interests include improvement, characterization and measurement of non-volatile memory devices and semiconductor devices with high-k layer.