Bidirectional Transient Voltage Suppression Diodes for the Protection of High Speed Data Line from Electrostatic Discharge Shocks

Daoheung Bouangeune[1], Sang-Sig Choi[2], Chel-Jong Choi[1], Deok-Ho Cho[2], and Kyu-Hwan Shim[1]

Abstract—**A bidirectional transient voltage suppression (TVS) diode consisting of specially designed p^{-}-n^{++}-p^{-} multi-junctions was developed using low temperature (LT) epitaxy and fabrication processes. Its electrostatic discharge (ESD) performance was investigated using I-V, C-V, and various ESD tests including the human body model (HBM), machine model (MM) and IEC 61000-4-2 (IEC) analysis. The symmetrical structure with very sharp and uniform bidirectional multi-junctions yields good symmetrical I-V behavior over a wide range of operating temperature of 300 K – 450 K and low capacitance as 6.9 pF at 1 MHz. In addition, a very thin and heavily doped n^{++} layer enabled I-V curves steep rise after breakdown without snapback phenomenon, then resulted in small dynamic resistance as 0.2 Ω, and leakage current completely suppressed down to pA. Manufactured bidirectional TVS diodes were capable of withstanding ± 4.0 kV of MM and ± 14 kV of IEC, and exceeding ± 8 kV of HBM, while maintaining reliable I-V characteristics. Such an excellent ESD performance of low capacitance and dynamic resistance is attributed to the abruptness and very unique profiles designed very precisely in $p^{-}n^{++}p^{-}$ multi-junctions.**

Manuscript received Jul. 31, 2013; accepted Oct. 29, 2013
A part of this work was presented in Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices, Seoul in Korea, June 2013
[1] School of Semiconductor and Chemical Engineering, Semiconductor Physics Research Center, Chonbuk National University, Jeonju 561-756, Republic of Korea.
[2] R&D Division, Sigetronics, Inc., Jeonju 561-756, Republic of Korea.
E-mail : khshim@jbnu.ac.kr.

Index Terms—**ESD, HBM, IEC 61000-4-2, MM, TVS diode**

I. INTRODUCTION

Electrostatic discharge (ESD) is known as a high pulse current and voltage with a fast decay time source, which can break the insulators, junctions and metal interconnects in electronic devices and the integrated circuits (ICs) [1]. As the IC dimension has been continuously scaled down, it realized higher packing density, faster operation speed and lower power dissipation. The semiconductor components also become smaller and lead to the increase in the probability of being damaged by ESD [2]. In general, since ESD can have either a positive or negative polarity, bidirectional ESD protection devices are necessary to protect sensitive electronic components, IC chips and circuits, especially, a bidirectional signal I/O line. Both n-p-n and p-n-p structures have been widely used as the main part of a bidirectional ESD protection device such as bidirectional silicon control rectifiers (SCRs) [3, 4] and punch-through diode [5]. Bidirectional snapback devices like SCRs are excellent in achieving low clamping voltage and small turn-on resistance. However, low holding and high triggering voltages are the main problem. Moreover, the complicated lateral structure affects the carrier transportation as current crowded, and leads to the increase in the device temperature more seriously as compared to vertical structure. The heating problem is the major cause of degradation and failure, and results in poor ESD performance. Meanwhile, the punch-through diodes get a lot of expediency such as low leakage current, capacitance and breakdown without snapback [6]. Conventional, punch-through diodes are essentially three-layer structures (n^+pn^+ or p^+np^+) using wide lightly doped base region, which leads to high dynamic resistance (turn on resistance) [7, 8]. In previous works [9, 10], it was reported that transient voltage suppression (TVS) diodes ($p^+p^-n^+$ and $n^+n^-p^+$ structures) achieved excellent ESD performance, small dynamic resistance and low clamping voltage.

Therefore, in this work, we purpose to develop a new bidirectional TVS diode consisting of $p^{++}p^-n^{++}p^-p^{++}$ junction structures using epitaxial layers. To avoid the snapback phenomenon, the p-n-p structure is known more attractive in fact [11]. The vertical structure with a very thin and heavily doped n-type layer enabled I-V curve steeper after breakdown to suppress snapback phenomenon. Such structure can achieve lower dynamic resistance and improved ESD performance.

In addition, we demonstrate its ESD performance and reliability on the basis of ESD tests including the human body model (HBM), machine model (MM), and IEC 61000-4-2 (IEC). HBM and MM as prevailing ESD simulator models represent the effect of statistic charges generated by the human body and machine. Human bodies are charged by walking across a carpeted floor or removing a sweater, likewise machine components are charged by rubbing non-conductive materials during operation [12]. Meanwhile, IEC 61000-4-2 is part of a large family of IEC 61000-4 standards, which regulate the minimum ESD level of acceptability, essential performance for all electronic devices sold in the European Union [13]. Fig. 1 represents various ESD waveforms used in this work, and their details can be found elsewhere [12-14].

II. Experimental Procedure

The proposed bidirectional TVS diode as shown in Fig. 2 has planar junctions with thin Si epitaxial films of $p^{++}/p^-/n^{++}/p^-/p^{++}$ junction structure grown on the heavily doped p-type silicon (100) substrate with a thickness of 600 μm. Its fabrication process starts by cleaning Si substrates in HF solution to remove native oxides. After inserting into a reduced-pressure chemical vapor deposition (RPCVD) chamber via a nitrogen purged load-lock chamber, the substrates experienced high temperature (HT) hydrogen baking at 950 °C for 5 min, then Si epitaxial layers were grown using doping gases of diborane (B_2H_6) and phosphine (PH_3). The epitaxy process was performed at low temperature (LT) around 600-800 °C to minimize the diffusion of dopant atoms and possible degradation of device performance due to the non-uniform local electric field concentrated at SiO_2/Si interfaces. Linearly-graded junctions are frequently formed at HT for conventional drive-in processes. As the top electrode contact, Ti/Ni/Au (100/500/150 nm) films were deposited through the square shape pattern of 140×140 μm^2 in size using an e-beam evaporator. The back side of substrates was grinded down to 150-µm thickness, and followed by the backside metal electrode contract.

Temperature dependent current-voltage (I-V-T) measurement was performed using a semiconductor parameter analyzer, HP4155A equipped with a probe station. The temperature was controlled using a thermal

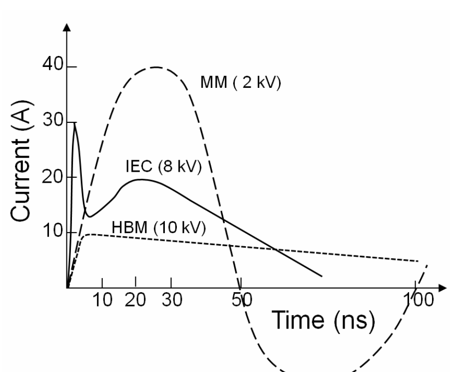

Fig. 1. Dynamic parameters comparison of typical ESD waveforms used in the proposed work [14].

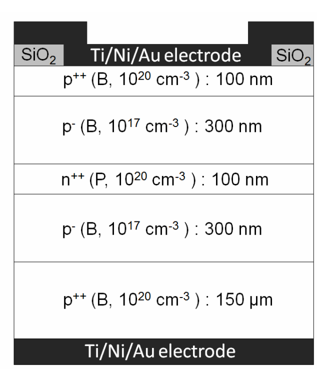

Fig. 2. Cross-section view of a bidirectional TVS diode with abrupt multiple junctions.

chuck attached inside a shielded cover. Capacitance-voltage (C-V) curves were measured under the reverse bias condition at a frequency range of 1 kHz to 1 MHz using a precision LCR meter (Agilent 4284A). ESD properties were analyzed using an ESD simulator, NoiseKen ESS-6008 for the machine model (MM) and human body model (HBM), and an ESS-2000 with a discharge gun TC-815R for IEC 61000-4-2 standard (also called IEC). Manufactured TVS diodes were subjected to various levels of ESD pulse of 10 discharges in both positive and negative polarities with 1 Sec time intervals.

III. Results and Discussion

Fig. 3 represents the I-V characteristics of a bidirectional TVS diode measured at a wide temperature range of 300 K - 450 K. For all temperatures, the device shows good symmetrical I-V behavior without degradation of the device performance. The increase in temperature led to noticeable changes in the breakdown voltage and leakage current. Since the carriers in the semiconductor follow the Boltzmann statistics, the reverse leakage current also increased at high temperature as normally observed in semiconductors. The temperature coefficient of the leakage current was measured to be 9×10^{-7} A/K at ± 6 V, while the reverse leakage current was kept below 10^{-6} A. The small reverse leakage current may ensure the strong points in reliability, noise performance, and ESD robustness of the TVS device.

Manufactured bidirectional TVS diodes have a breakdown voltage (BV) of ± 10 V, which imply that the breakdown occurs mostly in the Avalanche breakdown mode. However, as shown in Fig. 3, it is observed the TVS diode shows the negative temperature coefficient (NTC) of the breakdown voltage (ΔBV) which obtained as small as - 0.013 V/K at 10^{-6} A. We propose two possible mechanisms to explain the NTC phenomena of breakdown. At first, we may discuss the temperature compensation for the bidirectional TVS diode, as imaged as a pair of back to back unidirectional TVS diodes as shown in Fig. 4. Total temperature dependence can be given as $BV=V_D + BV_{Uni} + (BV_{Uni} + \Delta V_D)$, where V_D is the voltage dropped across the diode in forward bias and BV_{Uni} is the breakdown voltage of the unidirectional TVS diode. In fact, unidirectional TVS diodes have ever revealed negative and positive values of ΔV_D and ΔBV_{Uni}, respectively [9, 10]. The BV value decreases as the temperature increases while $\Delta V_D > \Delta BV_{Uni}$. The second mechanism is based on the thermal generation of electron-hole pairs (EHPs) in the depletion region. The thermal generation of EHPs can induce the reduction of the depletion width at p-n junctions, which leads to increased carrier tunneling probability. The tunneling mechanism is known to dominate up to a breakdown voltage of 30 V [15]. The tunneling current may inject enough carriers to support a fast avalanche turn-on. Therefore, the BV value can be decreased as the temperature increases while tunneling-assisted impact ionization dominates.

As shown in Fig. 5, the dynamic resistance, R_D is plotted as a function of temperature, which is derived from the transient region of the I-V characteristics given above in Fig. 3. The R_D values obtained as 0.2 Ω at room temperature (RT), gradually increased while the temperature ramps up. Then, the R_D values are still

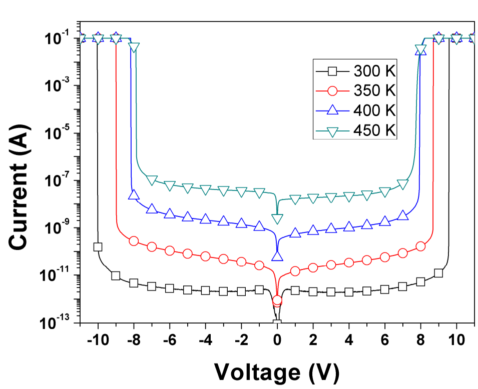

Fig. 3. I-V characteristics as measured from a bidirectional TVS diode at various temperatures of 300, 350, 400, and 450 K.

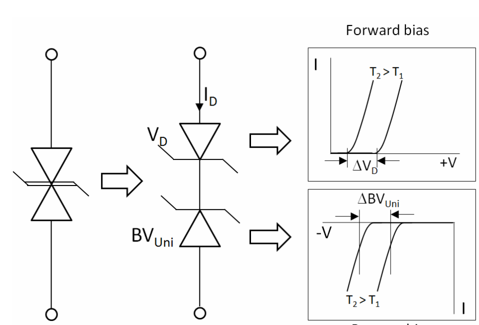

Fig. 4. Schematic shows principle of temperature compensation for a bidirectional TVS diode.

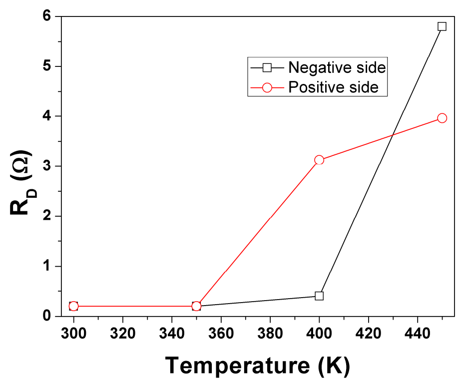

Fig. 5. Dynamic resistances of a bidirectional TVS diode measured at various temperatures.

observed to be below 6 Ω at high temperature (HT) of 450 K. These values are quite small compared to the conventional bidirectional SCR [4] and punch-through diodes [7]. The diode with small R_D would exhibit enhanced ESD performance in terms of small clamping voltage (V_c) and minimized Joule heating known as the principal cause of degradation or damage. This perspective consideration is discussed below in accordance with the ESD data as measured in experiments.

TVS diode samples have been used for ESD test as provided on the wafer. I-V curves were measured each and every time for the samples after experiencing ESD shocks. The degree of degradation is also determined according to the leakage current level and breakdown voltage caused by ESD stresses.

Usually, our TVS diodes exhibit excellent strength against all ESD stresses. The HBM stress led to the negligible degradation of device performance with I-V curves showing almost identical behaviors. Moreover, the leakage current level was maintained in pA even after the HBM pulses of ± 8 kV (a maximum available voltage) as shown in Fig. 6(a). Similarly, the TVS diodes were capable of withstanding ± 4.0 kV for MM and ± 14 kV for IEC as shown in Figs. 6(b) and (c), respectively. However, both ± 5 kV MM and ± 15 kV IEC shocks resulted in a rapid increase in the leakage current indicating typical electrical failures.

It is obvious that the bidirectional TVS diode can’t avoid hard breakdown and failure at high voltage after all. The scanning electron microscope (SEM) pictures given in Figs. 7(a) and (b) reveal the surface of the TVS diodes damaged respectively by ± 5 kV MM and ± 15 kV IEC

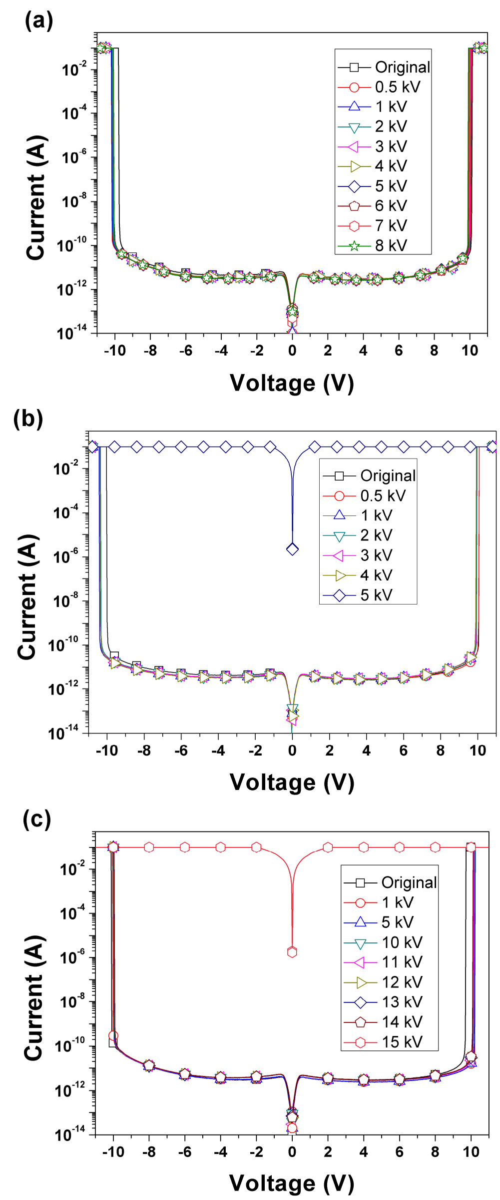

Fig. 6. I-V characteristics measured before and after experiencing various ESD stresses (a) HBM, (b) MM, (c) IEC.

shocks. The ESD shocks induced burning of metal electrode with lots of pinholes. This indicates that the epitaxial grown junction was damaged, and should be responsible for the device failure.

Another important parameter of the TVS diode is capacitance, which should be small enough to increase the cut-off frequency, and minimize the signal attenuation at high speed data rate. The capacitance values are obtained in the range of 12 pF ~ 6.8 pF at various frequencies from 1 kHz to 1 MHz as shown in Fig. 8. The capacitance values are quite small compared

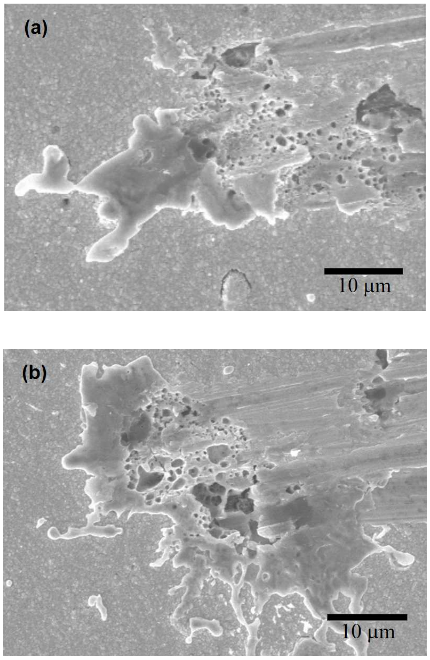

Fig. 7. SEM images showing the damaged region by (a) ± 5 kV MM, (b) ± 15 kV IEC shocks.

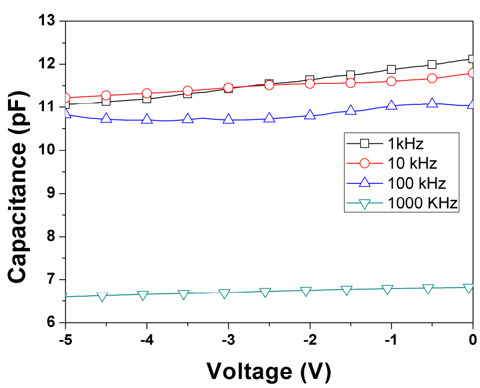

Fig. 8. C-V characteristics measured from a bidirectional TVS diode at frequency range of 1 kHz to 1 MHz.

to the conventional punch-through devices of 10^3 pF [16] and the unidirectional TVS diode of 60 pF [10]. Due to the bidirectional TVS structure, the capacitance value was expected to be one-half of the unidirectional TVS diode in principle.

In order to discuss the possibility for the device to guarantee specifications for the high data rate communications, the insertion loss was measured as a function of frequency from 3 MHz to 3 GHz, as shown in Fig. 9. The bidirectional TVS diode shows the uniform and wide signal band pass, up to a cut off frequency of 500 MHz. It implies that the bidirectional TVS diode can

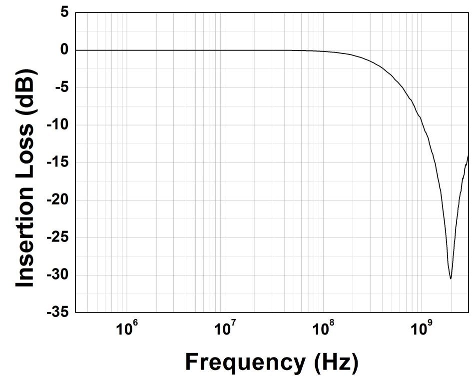

Fig. 9. Plots insertion loss as a function of frequency for the bidirectional TVS diode.

be used for the high data rate communications as well as for the ESD/EMI filter attenuating the RF noise in GHz range.

According to the experimental results as discussed above, the manufactured bidirectional TVS diodes presented excellent ESD robustness along with small values in leakage current, dynamic resistance and capacitance. The breakdown voltage decreased from ±10 V to ± 8 V, while the temperature was varied from 300 K to 450 K. The stand-off voltage values (V_{ST}, usually equals 0.8×BV, as defined a level that the TVS diode is non-conductive and safe) range from ± 8 V to ± 6.4 V at RT and HT. Such properties, the manufactured TVS diodes are suitable for the protection of 6 V high speed bidirectional signal I/O line such as peripherals, portable electronics and mobile devices.

IV. CONCLUSIONS

We have developed a new bidirectional TVS diode consisting of $p^{++}p^{-}n^{++}p^{-}p^{++}$ junction structures. The reduced pressure chemical vapor deposition technology enables us to grow uniform thin Si films with various doping conditions and thicknesses. Because of the vertical structure with a very thin and heavily doped n^{++}-type layer, the I-V curve showed relevant conduction property after breakdown without any serious snapback phenomenon, and resulted in small values in dynamic resistance, capacitance and leakage current as well. The bidirectional TVS diodes presented an excellent ESD performance, withstanding ± 4.0 kV MM and ± 14 kV IEC, and ± 8 kV HBM while maintaining reliable I-V characteristics. Such outstanding properties are attributed to the unique structure of $p^{++}p^{-}n^{++}p^{-}p^{++}$ multiple junctions along with the LT epitaxy and fabrication processes.

ACKNOWLEDGMENTS

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2009-0094031 and Grant No. 2013R1A1A2010053). It was also supported by a grant from the R&D Program for Industrial Core Technology funded by the Ministry of Trade, Industry and Energy (MOTIE), Republic of Korea (Grant No. 10044651).

REFERENCES

[1] C. Duvvury and A. Amerasekera, "Handbook of Failure Modes, Reliability Issues, and Case Studies, ESD in Silicon Integrated Circuits," 2nd Edition John Wiley & Sons, Ltd, chapter 8, pp.228-272, 2002.

[2] A. Amerasekera and C. Duvvury, "The Impact of Technology Scalingon ESD Robustness and Protection Circuit Design," IEEE Trans. Compon., Packag., Manuf. Technol, Vol.18, NO.2, pp.314-320, June, 1995.

[3] J.A. Salcedo, J.-J. Hajjar, S. Malobabic and J.J. Liou, "Bidirectional Devices for Automotive-Grade Electrostatic Discharge Applications," IEEE Electron Device Lett., Vol.33, NO.6, pp.860-862, June, 2012.

[4] Zhiwei Liu, J. Vinson, Lifang Lou and J.J. Liou, "An Improved Bidirectional SCR Structure for Low-Triggering ESD Protection Applications," IEEE Electron Device Lett., Vol.29, NO.4, pp.360-362, Apr., 2008.

[5] D. de Cogan, "The punch-through diode", Microelectronics, Vol. 8, NO.2, pp.20-23, 1977.

[6] Ya-Chin King, Bin Yu, J. Pohlman and Chenming Hu, "Punchthrough diode as the transient voltage suppressor for low-voltage electronics," EEE Trans. Electron Devices, Vol.43, NO.11, pp.2037-2040, Nov., 1996.

[7] D.de Cogan, "Punch-through diode as a power device," Solid-State and Electron Devices, IEE. Proc, Vol.127, NO.2, pp.67-71, Apr., 1980.

[8] J. Lohstroh, J. J. M. Koomen, A. T. Van Zanten and R. H. W. Salters, "Punch-through currents in p+np+ and n+pn+ sandwich structures," Solid StateElec., Vol.24, NO.9, pp.804-820, Sept., 1981.

[9] S. S. Choi, D. H. Cho and K. H. Shim, "Development of Transient Voltage Suppressor Device with Abrupt Junctions Embedded by Epitaxial Growth Technology," Electron.Mater.Lett. Vol.5, NO.2, pp. 59-62, June, 2009.

[10] D. Bouangeune, et al, "ESD robustness of low-voltage/high-speed TVS devices with epitaxial grown films," Proc. Of The 1st IEEE GCCE, pp.189-192, Oct., 2012.

[11] P. Renaud, A. Gendron, M. Bafleur and N. Nolhier, "High robustness PNP-based structure for the ESD protection of high voltage I/Os in an advanced smart power technology," Proc. Of the meeting of IEEE Bipolar/BiCMOS Circuits and Technology, pp.226-229, Sept., 2007.

[12] J.E. Vinson and J.J. Liou, "Electrostatic Discharge in Semiconductor Devices: An Overview," Proc. Of The IEEE, Vol.86, NO.2, pp. 399-420, Feb., 1998.

[13] B. Jeppesen and C. bussmann, "Electrostatic Discharge Specifications and protection Methods," Proc. Of The Conference Northcon, pp. 134-137, Oct., 1998.

[14] Michel Mardiguian, "Electrostatic Discharge, understand, simulate, and fix ESD problems," 3nd Edition, John Wiley & Sons, Inc, chapter 1, pp.30, 2009.

[15] A. G. Chynoweth and G. L. Pearson, "Effect of dislocations on breakdown in silicon p-n junctions," J. Appl. Phys., Vol.29, NO.7, pp. 1103–1110, Jul. 1958.

[16] Ya-Chin King, Bin Yu, J. Pohlman and Chenming Hu, "Punchthrough Transient Voltage Suppressor for Low-Voltage Electronics," IEEE Electron Device Lett., Vol.16, NO.7, pp. 303–305, July, 1995.

Daoheung Bouangeune was born in Sayaboury, Laos, on May 28, 1986. He received the B.S degree in physic from National University of Laos in 2008 and M.S degree in applied physic from National University of Laos in 2011. He is currently working toward the PhD degree on semiconductor engineering at Chonbuk National University, South Korea. His research interests in fabrication and developing ESD protection devices which relative to Zener diode, TVS diode, RC and LC filter.

Sang-Sik Choi is a Research and Development Division, Sigetronics, Inc., Jeonju 561-756, Republic of Korea.

Chel-Jong Choi was born in Korea, on June 16, 1974. He received the B.S. degree in ceramic engineering from Hanyang University, Seoul, Korea, in 1997, and the M.S. and Ph.D. degrees in materials science engineering from the Gwangju Institute of Science and Technology (GIST), Gwangju, Korea, in 1999 and 2003, respectively. From 2003 to 2005, he was with the Samsung Advanced Institute of Technology (SAIT), Suwon, Korea, in the areas of semiconductor-device characterization. From 2005 to 2008, he worked with the Electronics and Telecommunications Research Institute (ETRI), Daejon, Korea, where he was involved in the process integration of nano-scaled Schottky barrier MOSFETs. Since 2008, he has been with Chonbuk National University, Jeonju, Korea. His research interests include the novel nano-scaled Ge- and III-V- based electronic devices for the ultimate CMOS and post-CMOS technologies.

Deok-Ho Chois a Research and Development Division, Sigetronics, Inc., Jeonju 561-756, Republic of Korea.

Kyu-Hwan Shim received his BS and MS degrees in materials science and engineering from Korea University in 1984 and 1986, respectively, and his PhD degree from the University of Illinois at Urbana-Champaign (UIUC). Meanwhile he joined the Electronics and Telecommunications Research Institute (ETRI) in 1986, where his major activities were focused on compound semiconductor processes and devices like GaAs MESFETs until 1992. Thanks to ETRI's program, he could study at UIUC for his PhD degree and specialize the epitaxial growth and device development of GaN-based heterostructures. For five years after 1999, while working as a principal research member, his efforts were devoted to SiGe HBTs, BiCMOS integrated circuits, and strained-silicon MOSFETs. Then he moved to the Chonbuk National University (CBNU) to become a professor in 2004, and continued his research on SiGe and related semiconductor materials, processes, and devices in his lab Intelligent Semiconductor Research Lab (ISRL). At the same time, he started to serve as a CEO for a new lab-based venture company, Sigetronics Ltd. established inside the CBNU campus, where various semiconductor devices such as Zener diode(for LEDs), TVS, ULC-TVS, ESD/EMI Filter, SBD, FRD, Power-FETs have been developed and commercialized. His research is focused mostly on the epitaxial growth of germanium on silicon substrates (Ge-on-Si) and its application for future electrical and photonic devices including the beyond-CMOS and the emitters/receivers of optical signals for communications and image signal processing as well. He wants to assist for a new generation started on the basis of GaN, Ge, Si in every academic and industrial sectors.