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A Highly Efficient Dual-Mode 3G/4G Linear CMOS Stacked-FET Power Amplifier Using Active-Bypass

Unha Kim* · Yong-Gwan Kim · Jung-Lin Woo · Sunghwan Park · Youngwoo Kwon

Abstract

A highly efficient dual-mode linear CMOS stacked-FET power amplifier (PA) is implemented for 3G UMTS and 4G LTE handset applications. High efficiency is achieved at a backed-off output power (P_{out}) below 12 dBm by employing an active-bypass amplifier, which consumes very low quiescent current and has high load-impedance. The output paths between high- and low-power modes of the PA are effectively isolated by using a bypass switch, thus no RF performance degradation occurs at high-power mode operation. The fabricated 900 MHz CMOS PA using a silicon-on-insulator (SOI) CMOS process operates with an idle current of 5.5 mA and shows power-added efficiency (PAE) of 20.5%/43.5% at P_{out} = 12.4 / 28.2 dBm while maintaining an adjacent channel leakage ratio (ACLR) better than –39 dBc, using the 3GPP uplink W-CDMA signal. The PA also exhibits PAE of 35.1% and $ACLR_{E\text{-}UTRA}$ of –33 dBc at P_{out} = 26.5 dBm, using the 20 MHz bandwidth 16-QAM LTE signal.

Key Words: Active-Bypass, CMOS, Efficiency, Linear, LTE, Power Amplifier, Stacked-FET, W-CDMA.

I. INTRODUCTION

As a mobile communication standard is evolved toward 3G UMTS and 4G LTE, the importance of power amplifier (PA) efficiency is growing to extend the battery lifetime of mobile terminals [1]. The explosive demand for high-speed data transmission has now led handset PA researchers to focus on improvement of efficiency at high power levels, since 4G LTE PAs cover a wide bandwidth signal (10–20 MHz) and are mostly operated in the high output power region (>24 dBm) to maximize the data rate. The efficiency enhancement at low-power level (<12 dBm) also remains important for extending talk-time of the voice-centric 2G/3G standards (backward compatibility); thus, this should be applied to PAs [1].

To enhance the efficiency in the low output power (P_{out}) level, several methods have been proposed [1–4]. Among these, an active stage-bypass technique is an attractive solution, because it can significantly reduce the average current consumption of a PA. This technique is subdivided into a conventional stage-bypass [3, 4] and an active full-bypass [2], which utilize a driver-stage and a separate bypass-stage, respectively. To achieve extremely low quiescent current (3–5 mA) and higher efficiency at backed-off P_{out} of more than 15 dB, the active full-bypass method is preferred.

Recent CMOS technology has also played an important role in handset PA design due to its size and cost benefits. By employing several power combining techniques such as the differential cascode and stacked-FET structures, the breakdown issue of a CMOS device is avoided and thus CMOS PAs are able to deliver watt-level P_{out} [3–7]. For these reasons, a multi-mode watt-level linear CMOS PA covering broad signal

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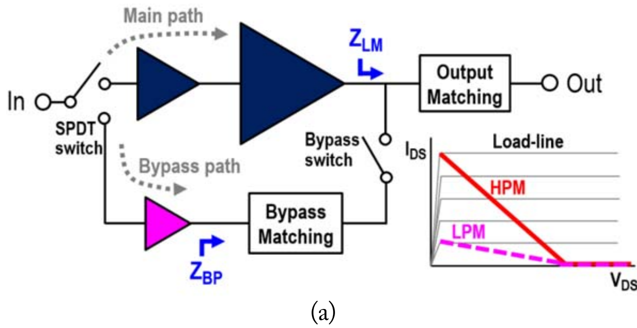
bandwidth is demanded.

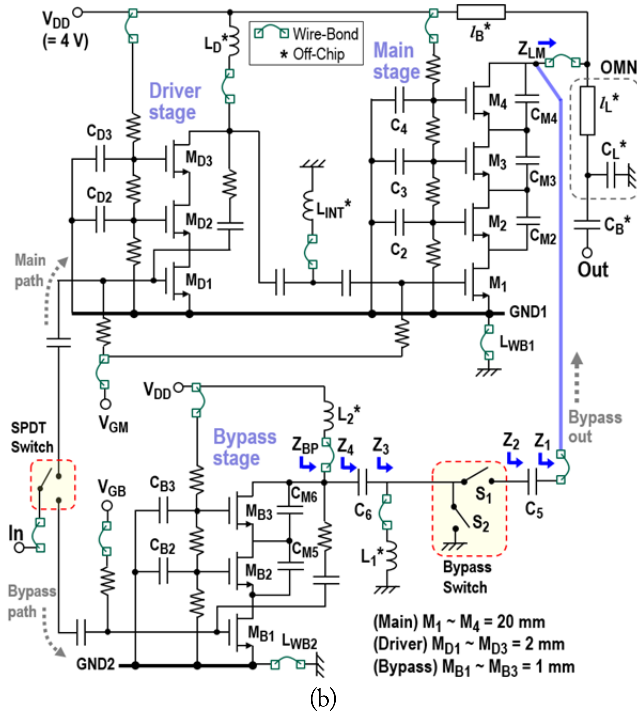
The authors' previous work [8] introduced a highly efficient stacked-FET linear CMOS PA using an active full-bypass for 3G handset applications. This paper expands the work [8] by presenting a detailed design description (in Section II) and fabrication and measurement results, including the 20 MHz bandwidth 4G LTE as well as the 3G W-CDMA (in Section III).

II. Circuit Design

Fig. 1(a) shows a block diagram of the proposed dual-mode linear CMOS stacked-FET PA. It consists of a two-stage main amplifier and a bypass amplifier, each aiming for high-power mode (HPM) and low-power mode (LPM) amplification. Since both amplifiers share an identical supply voltage, the load impedance of the bypass amplifier, Z_{BP}, should be far greater than that of the main amplifier (Z_{LM}) to achieve high efficiency at backed-off P_{out} of more than 15 dB. This is fulfilled by the bypass matching network. Another design requirement is to achieve an effective isolation between the HPM/LPM output paths during HPM operation. This is fulfilled by the bypass switch and the RF performance degradation at high P_{out} region can thus be avoided.



(a)



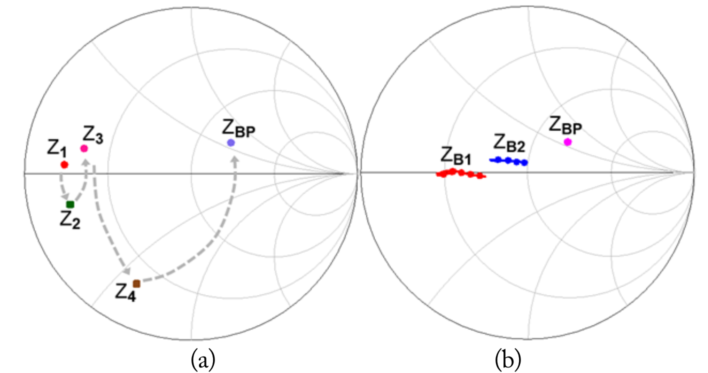
(b)

Fig. 1. (a) Conceptual block diagram of the proposed dual-mode active full-bypass power amplifier (PA). (b) Detailed schematic of the proposed PA using a stacked-FET PA structure.

The detailed schematic of the proposed PA is shown in Fig. 1(b). The PA design is based on a single-ended stacked-FET PA theory [5], where the main amplifier is composed of a triple-stack driver-stage (2 mm gate-width) and a quadruple-stack main-stage (20 mm gate-width) for watt-level power amplification under V_{DD} = 4 V condition. Extremely low quiescent current and high efficiency below 12 dBm is achieved by adopting a triple-stack bypass-stage with smaller size (1 mm gate-width). The design of the main-amplifier is almost identical that presented in [6], except for the gate capacitors (C_2–C_4) and output matching network (OMN); they are re-optimized to have lower load impedances of the top and internal FETs (M_1–M_4) compared to [6], which means that Z_{LM} = 5 Ω in this work whereas Z_{LM} = 6 Ω in [6]. Together with the load optimization and parasitic cancellation by employing the external drain-source Miller capacitors (C_{M2}–C_{M4}) [9], adequate linearity and efficiency can thus be achieved at high power region without an additional linearizer.

The efficiency during LPM operation is enhanced by designing the load impedance of the bypass-stage (Z_{BP} in Fig. 1(b)) to have a value that is 16 times greater than Z_{LM}. This operation is fulfilled by the four passive elements: C_5, L_1, C_6, and L_2. During LPM, S_1 and S_2 in Fig. 1(b) are closed and opened, respectively (and vice versa at HPM operation). Thus, the resultant Z_{BP} becomes approximately 80 Ω. Fig. 2 shows the simulated load impedance trajectory of the bypass amplifier.

The input and bypass switches are designed based on the required insertion loss, isolation, and power handling. Since the input SPDT switch does not require high power handling and



(a) (b)

Fig. 2. Simulated load impedances of the bypass-stage at low-power mode operation. (a) Impedance trajectory. (b) Load impedances of the bypass FETs (M_{B1}, M_{B2}, and M_{B3}) as a function of input power.

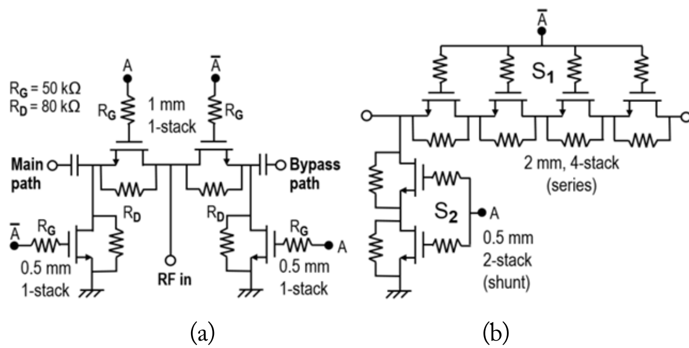


Fig. 3. Schematic of the RF switches for power-mode reconfiguration. (a) SPDT switch. (b) Bypass switch.

low loss, a simple single-stack series-shunt configuration is employed, as shown in Fig. 3(a). The simulated insertion loss and RF power handling of the SPDT switch are 0.1 dB and 19 dBm, respectively. On the other hand, the bypass switch experiences a high RF voltage swing during HPM and output thru-loss during LPM operation. Since the series-arm (S_1 in Fig. 1(b)) is off-state at HPM, its number of stacks is chosen to be the same as that of the main-stage (= 4) to with stand the large voltage swing. The shunt-arm (S_2 in Fig. 1(b)) is used to enhance the isolation. Thus, almost no performance degradation is achieved at HPM compared with the conventional PA without an active-bypass. An RF power of more than 15 dBm is withstood during LPM by adopting a double-stack for S_2. Loss and efficiency at LPM are strong functions of S_1 gate-width, because the series resistance of S_1 (R_S) and forwarding impedance (Z_2) with a low value are connected in series, as shown in Figs. 1(b) and 2(a). Fig. 4 shows the simulated power-added efficiency (PAE) as a function of S_1 gate-width at LPM. Since wider gate-width of S_1 with quadruple-stack gives rise to both advantage (better PAE) and disadvantage (larger IC area), its gate-width should carefully be determined. In this work, it is designed to be 2 mm, as shown in Fig. 3(b). Even though some loss is induced by S_1, this does not cause a significant efficiency degradation because the average efficiency at LPM is mainly determined by the idle current.

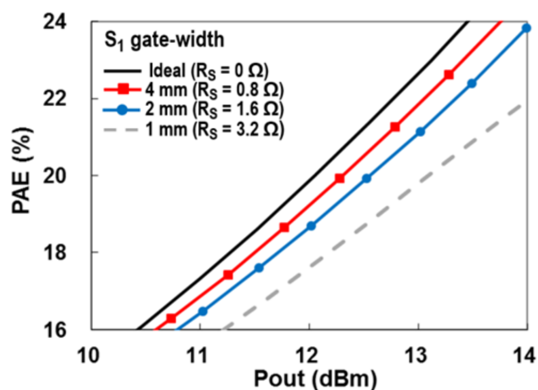
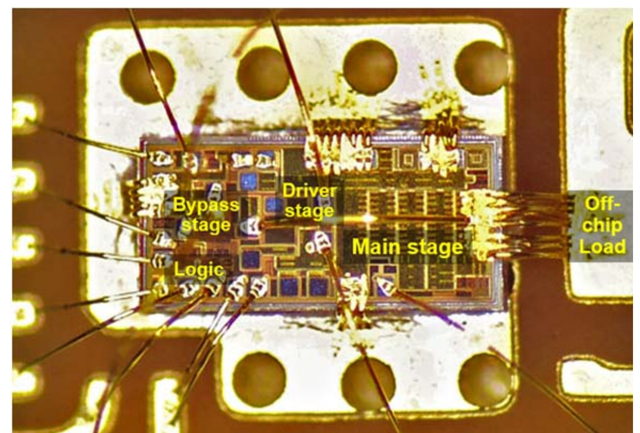


Fig. 4. Simulated power-added efficiency (PAE) for various S_1 gate-widths (R_S is the equivalent series resistance of S_1 at on-state).

III. Fabrication and Measurement

The designed PA was fabricated using a 0.18-μm silicon-on-insulator (SOI) CMOS process and all the MOSFETs used in this work have a gate-length of 0.32-μm (2.5-V device). A single NFET for RF switch offers a series resistance of 0.8 Ω and an off-capacitance of 310 fF/mm, resulting in figure-of-merit of 250 fsec [10]. Capacitances of the seven gate capacitors for common-gate FETs, C_2, C_3, C_4, C_{D2}, C_{D3}, C_{B2}, and C_{B3} are 33, 14, 12, 6, 2, 4, and 1.5 pF, respectively. Five external drain-source Miller capacitors, C_{M2}, C_{M3}, C_{M4}, C_{M5}, and C_{M6} have values of 3, 6, 10, 1, and 1 pF, respectively. Four inductors, L_{INT}, L_D, L_1, and L_2, were realized with off-chip elements, where L_1 and L_2 can be integrated on-chip while compromising slight PAE degradation at LPM operation. The switch operation is controlled by the integrated logic circuit. The IC was mounted on a 400-μm-thick FR4 PCB ($\varepsilon_r = 4.6$, $\tan\delta = 0.025$), where an LC-based OMN was realized with off-chip. The source degeneration effect was minimized by using multiple bond-wires for RF grounding. Fig. 5 shows photographs of the fabricated SOI CMOS PA IC and test module.



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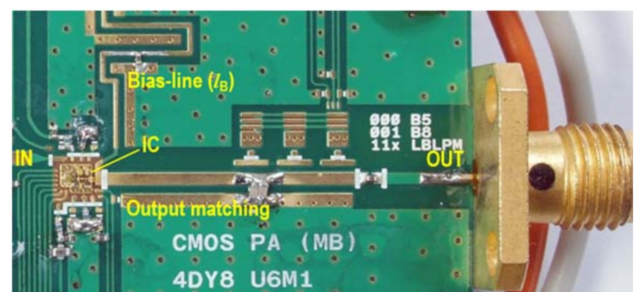
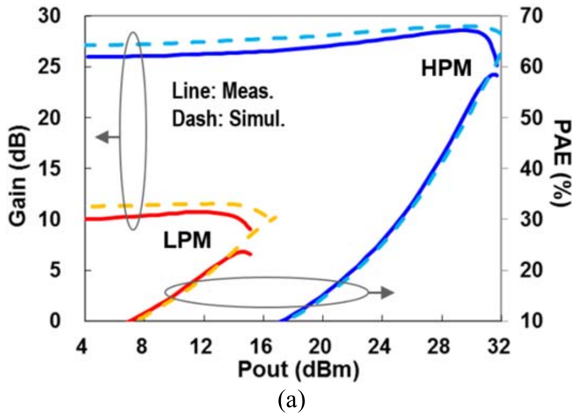


(b)

Fig. 5. Photograph of the fabricated (a) SOI CMOS PA IC mounted on a PCB (IC die size = 1.46 mm × 0.68 mm) and (b) test PA module. PA = power amplifier, PCB=printed circuit board, SOI = silicon-on-insulator.



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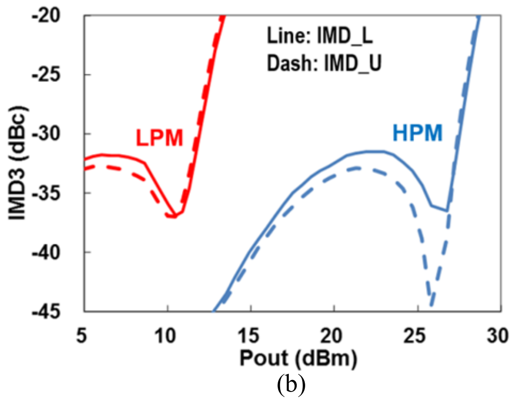
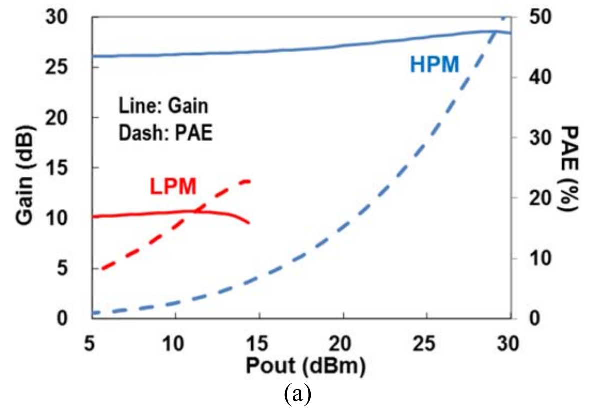


(b)

Fig. 6. Measured results. (a) Continuous wave (CW) gain and power-added efficiency (PAE). (b) Two-tone third-order intermodulation distortion (IMD3) (tone spacing = 4 MHz). HPM = high-power mode, LPM = low-power mode.



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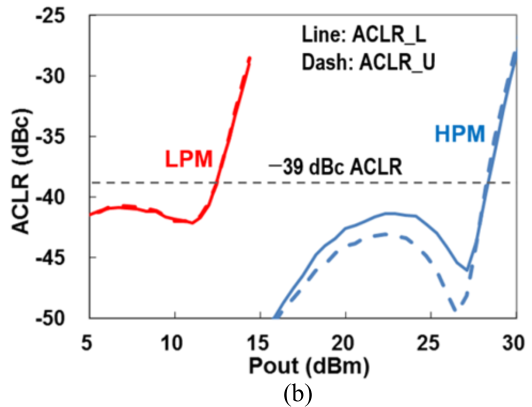

(b)

Fig. 7. Measured 3G W-CDMA results. (a) Gain and power-added efficiency (PAE). (b) Adjacent channel leakage ratio (ACLR). HPM = high-power mode, LPM = low-power mode.

The PA module was tested at 897.5 MHz (3G/4G Tx center frequency of band-8) and V_{DD} = 4 V. The quiescent current was 5.5/82 mA for LPM/HPM operation. For the measurement, continuous wave (CW)/two-tone, W-CDMA, and LTE signal were used. Fig. 6(a) shows the measured gain and PAE using CW signal, and Fig. 6(b) shows the measured third-order intermodulation distortion (IMD3) result using the two-tone signal. The PA showed a linear gain of higher than 10/26 dB, saturated P_{out} of 15.8/31.7 dBm, and peak PAE of 23.6%/58.5% for LPM/HPM operations. Maximum linear output powers meeting IMD3 of –28 dBc are 12/27.6 dBm at LPM/HPM regions.

Measured W-CDMA (Rel'99) results of the PA are plotted in Fig. 7. During HPM operation, the PA showed a linear gain of higher than 26 dB and an adjacent channel leakage ratio (ACLR) better than –39 dBc up to P_{out} = 28.2 dBm. PAE at 28.2 dBm was 43.5%. During LPM operation, the PA showed a gain of higher than 10 dB and ACLR better than –39 dBc up to P_{out} = 12.4 dBm. PAE of 20.5% was achieved at 12.4 dBm, which is PAE improvement of +16% compared with that at the same P_{out} of HPM operation.

Finally, LTE performance was measured using the 20 MHz-bandwidth 16-QAM signal (peak to average power ratio [PAPR] = 7.3 dB) and the result is plotted in Fig. 8. The signal was obtained from the Agilent's Signal Studio (N7624B). The PA showed $ACLR_{E\text{-}UTRA}$/error vector magnitude (EVM) of better than –33 dBc/3.8% up to P_{out} = 26.5 dBm. PAE at 26.5 dBm was 35.1%. Compared with the result using the 10 MHz-bandwidth LTE signal, which showed PAE of 35.6% and $ACLR_{E\text{-}UTRA}$ of –33 dBc at P_{out} = 26.6 dBm, negligible PAE degradation was measured. It should also be noted that the fabricated PA exhibits no significant memory effect (ACLR asymmetry) up to 20 MHz signal bandwidth.

The performance of recently reported multi-mode W-CDMA PAs is summarized in Table 1. Compared to the reported CMOS PAs, the proposed PA shows the lowest quiescent DC power (22 mW) and better linear efficiency below 12 dBm, thus resulting in a significant reduction on average current consumption. The linearity and efficiency of the proposed PA at both power modes are favorable among the reported CMOS PAs and are also comparable to the GaAs-based PAs.

IV. Conclusion

A 900 MHz dual-mode stacked-FET PA has been implemented using an SOI CMOS technology for 3G/4G handset applications. Employing an active-bypass amplifier and RF

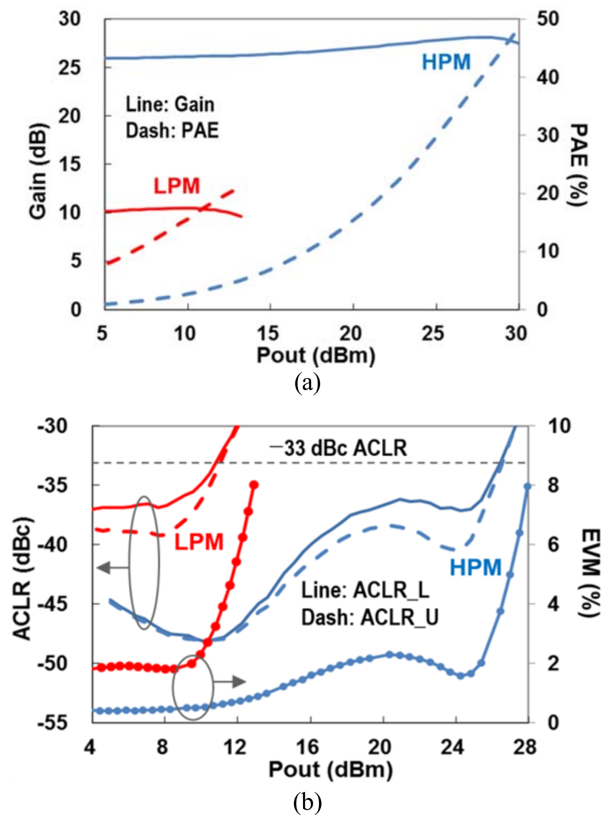

Fig. 8. Measured 4G LTE results using 20 MHz-BW 16-QAM signal. (a) Gain and power-added efficiency (PAE). (b) $ACLR_{E\text{-}UTRA}$ and error vector magnitude (EVM). HPM = high-power mode, LPM = low-power mode.

Table 1. Performance comparison of recently reported multi-mode W-CDMA PAs

Ref.	IC technology	P_{out} (dBm)	PAE (%)	ACLR (dBc)	$P_{DC,Q}$[a] (mW)	Freq. (GHz)
Hau & Singh [2]	GaAs BiFET	8.0 17.0 28.5	15 22 42	−40	12	1.95
Koo et al. [3][b]	CMOS 0.18 μm	16.4 28.0	27.4 36.4	−35	68	1.95
Jeon et al. [4][c]	CMOS 0.18 μm	15.7 26.6	16.4 35	−33	61[d]	1.95
This work	SOI 0.32 μm (W-CDMA)	12.5 28.0	20.5 43.1	−39	22	0.9
This work	SOI 0.32 μm (LTE 20)[e]	10.9 26.5	17.5 35.1	−33 3.8%[g]	22	0.9

PA=power amplifier, PAE=power-added efficiency, ACRL=adjacent channel leakage ratio, SOI=silicon-on-insulator.
[a]Quiescent DC power consumption.
[b]On-chip matching.
[c]IPD-based matching.
[d]Graphically estimated.
[e]LTE with 20 MHz-BW 16-QAM (PAPR = 7.3 dB).
[g]Error vector magnitude (EVM).

switches resulted in significant PAE improvement at low-power level while maintaining good RF performance at high-power region. The fabricated PA showed a PAE of 20.5%/43.5% and W-CDMA ACLR of –39 dBc at P_{out} = 12.4/28.2 dBm. The PA also covered wide bandwidth signal (LTE) up to 20 MHz-bandwidth. Its efficiency and linearity are comparable to those of GaAs-based PAs.

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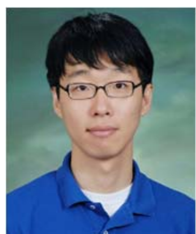

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