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Slew-Rate Enhanced Low-Dropout Regulator by Dynamic Current Biasing

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Abstract

We present a CMOS rail-to-rail class-AB amplifier using dynamic current biasing to improve the delay response of the error amplifier in a low-dropout (LDO) regulator, which is a building block for a wireless power transfer receiver. The response time of conventional error amplifiers deteriorates by slewing due to parasitic capacitance generated at the pass transistor of the LDO regulator. To enhance slewing, an error amplifier with dynamic current biasing was devised. The LDO regulator with the proposed error amplifier was fabricated in a 0.35-μm high-voltage BCDMOS process. We obtained an output voltage of 4 V with a range of input voltages between 4.7 V and 7 V and an output current of up to 212 mA. The settling time during line transient was measured as 9 μs for an input variation of 4.7–6 V. In addition, an output capacitor of 100 pF was realized on chip integration.

Key Words: Dynamic Current Biasing, Low-Dropout Regulator, Parasitic Capacitance, Slew-Rate.

I. INTRODUCTION

The design of power management in system-on-chip (SoC) for a wireless power transfer (WPT) system is now in active progress. The high-performance voltage regulation in terms of accuracy, power efficiency, response time, silicon area, and the off-chip component free feature is vital for power management in SoC. Of all types of voltage regulators, the low-dropout (LDO) regulator is regarded as a suitable choice for on-chip voltage regulation due to its fast transient response, low noise, and high stability and could be used as a building block for a WPT system receiver as shown in Fig. 1.

Because conventional LDO regulators for the receiver of a WPT system have been constituted with feedback topology (made up of voltage reference, error amplifier, and power device), frequency compensation is additionally required for closed-loop stability. This closed-loop stability is usually achieved with an off-chip capacitor's equivalent series resistance (ESR), which provides zero ESR for its open-loop transfer function and contributes pole-zero cancellation [1]. However, the stability significantly depends on the ESR, which cannot be easily controlled and changes with temperature. The off-chip capacitor is the main obstacle for the full integration of LDO regulators in SoC design. To resolve this issue, capacitor-free LDO regulators have been reported in [2–7].

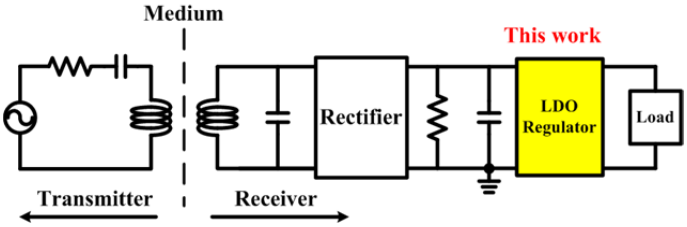

Fig. 1. Block diagram of wireless power transfer systems showing the low-dropout (LDO) regulator.

In LDO regulator design, accuracy and low-voltage dropout

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can be complemented by using the pass transistor, which is designed with a large transistor. The stability and phase margin can be improved by adding a Miller capacitor at the output stage of the error amplifier. However, parasitic capacitance around the large pass transistor and the Miller capacitor added for improving stability is seen as the output capacitance of the error amplifier and generates slewing, which slows the response of the pass transistor. This Miller capacitor provides a trade-off between stability and fast response. Since the receiver of a WPT system should produce electric power that responds quickly to inconsistent input power, a fast response is more important than stability. Therefore, the Miller capacitor was not employed for obtaining a fast response in this work. Based on this design philosophy, we designed an error amplifier with dynamic current biasing to improve the slew rate and verified the fast response and accuracy of the LDO regulator by using the proposed error amplifier with abrupt input changes.

II. Circuit Design and Analysis

1. Conventional LDO Regulators

Fig. 2 shows the block diagram of conventional LDO regulators. The most important feature of LDO regulators is the dropout voltage. To address this, the aspect ratio of the pass transistor is designed very large. As the parasitic capacitances (C_{gs} and C_{gd}) of a pass transistor become effective, these operate similar to the output capacitor of the error amplifier, causing an adverse effect.

The operational amplifier used for the error amplifier in Fig. 2 demonstrates a large output capacitance that causes slewing, as illustrated in Fig. 3. When the step input voltage is applied to *inp*, the voltage of the output node V_o does not precisely follow the instantaneously changing input voltage. In LDO regulators, the slew rate (SR) of a two-stage error amplifier is defined by the ratio of the tail current (I_{BIAS}) of the input node to the output capacitance (C_{OUT}), i.e., it can be expressed as

$$\mathrm{SR} = I_{BIAS}/C_{OUT}. \tag{1}$$

The error amplifier plays a crucial role in controlling the gate voltage of the pass transistor by rapidly detecting the change in output voltage against the reference voltage. A controlled gate voltage regulates the channel of the pass transistor, changing the current and dropout voltage. Therefore, slewing of the error amplifier prevents the quick detection of rapid change at the input. A method is needed to reduce the slew rate in order to improve accuracy and response of the LDO regulator. Based on Eq. (1), the slew rate can be enhanced by increasing the bias current.

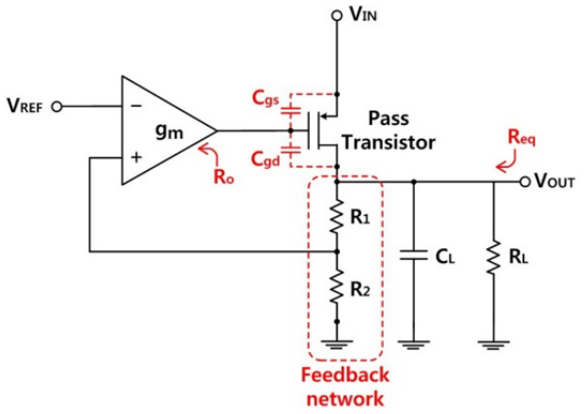


Fig. 2. Block diagram of a conventional low-dropout (LDO) regulator.

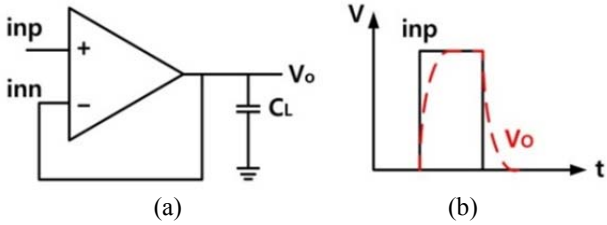


Fig. 3. Slewing of conventional op-amp.

2. Proposed LDO Regulators

As known from Eq. (1), the error amplifier of an LDO regulator requires more bias current to resolve slewing, and this can increase power consumption due to the excessive current. Thus, dynamic current biasing is proposed to improve the slew rate of an LDO regulator without consuming additional current.

Fig. 4 shows the CMOS rail-to-rail cascode amplifier working as an error amplifier of the LDO regulator. The first stage (input stage) designed in the rail-to-rail structure converts the input voltage to current. The second stage (trans-resistance amplifier stage), composed of a class-AB amplifier operating over a wide range, amplifies the converted current from the first stage, eventually controlling the pass transistor. The output of the LDO regulator is fed back to the input of the error amplifier since abrupt voltage change at the input needs to be detected in time [8].

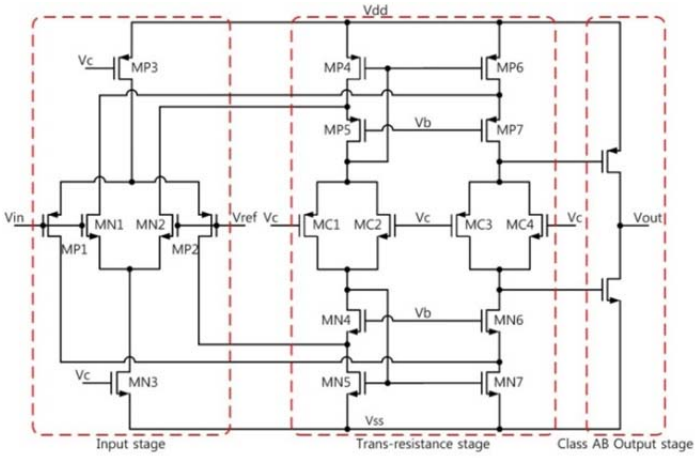


Fig. 4. CMOS rail-to-rail cascode amplifier.

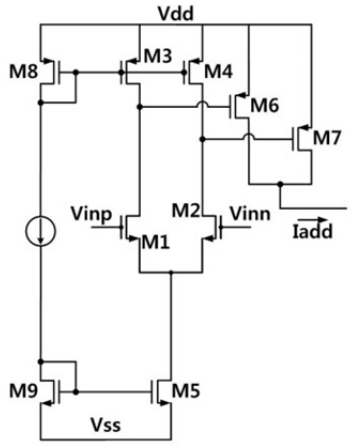


Fig. 5. Proposed dynamic current biasing.

The proposed dynamic current biasing is described in Fig. 5, which shows that current does not flow in a steady state but increases when slewing arises. The dynamic current bias circuit is composed of differential inputs (M1–M5) that can sense slewing and sub-current sources (M6, M7) that cause additional bias current. Operation of this dynamic current bias circuit is as follows:

V_{inp} and V_{inn} are assumed to have the same DC voltage levels. To maintain the drain voltages of M3–M4 close to V_{DD}, M3–M4 must be operating in a triode region. Therefore, M6 and M7 are turned off and do not generate additional current. However, when the step-input or rapidly changing signal is applied, the error amplifier brings about slewing. At this time, a tail current flows through M1 (or M2), and M3 (or M4) goes into a saturation region so that the drain voltage of M3 (or M4) decreases. As a result, additional current (I_{add}) created by the lowered gate voltage of M6 is added to the amplifier stage. Consequently, the dynamic current bias circuit does not generate additional current during the steady state but provides more current to increase the tail current of the error amplifier during slewing. Therefore, it operates in low power consumption during a steady state because a large amount of additional current is generated during slewing, and it can rapidly control the pass transistor of the LDO regulator by enhancing the slew rate through additional current [9].

Fig. 6 shows the final LDO regulator combined with the proposed CMOS rail-to-rail cascode amplifier as shown in Fig. 4 and the dynamic current bias circuit as proposed in Fig. 5.

III. Simulation and Measurement Results

Load transients for an LDO regulator employing dynamic current biasing werefirst simulated to comparewith load transients without dynamic current biasing. Fig. 7 demonstrates the simulated results. The load transient improved from 5 mV to 3 mV, and the settling time also improved from 1 μs to 0.5 μs. Results showed that the overall response from load variation was faster when dynamic current biasing was applied to the LDO regulator.

Line transients using 4.3–6 V input were also simulated for LDO regulators with and without dynamic current biasing. As shown in Fig. 8, the line transient improved from 100 mV to 90 mV, and settling time increased from 2 μs to 0.5 μs as expected.

The proposed LDO regulator was fabricated with Dongbu 0.35 μm BCDMOS technology. Fig. 9 shows a microphotograph of the proposed LDO regulator with an area of 840 μm × 850 μm. This LDO was mounted on a 100-pF capacitor loaded inside the chip.

The measured result of theline transient with a 100-pF output capacitor is shownin Fig. 10 and the perfornamce summary is providedin Table 1. The design concept of this proposed LDO regulator is for low-power consumption, but the measured current consumption was 4 mA, which is much larger than expected. Whereas an unnecessary large amount of current is consumed in the bias stage (shown in Fig. 6), which is contrary to the design goal, the error amplifier does not consume much current (less than 100 μA in simulation).

When the output voltage was 4 V, the input voltage had a

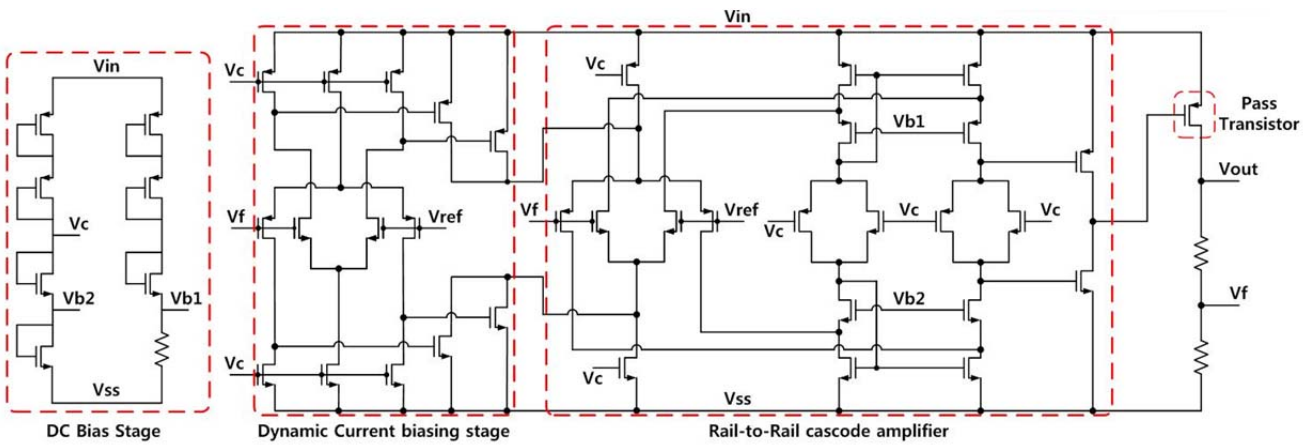
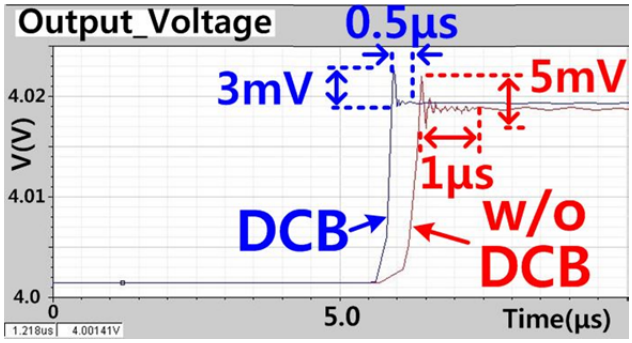
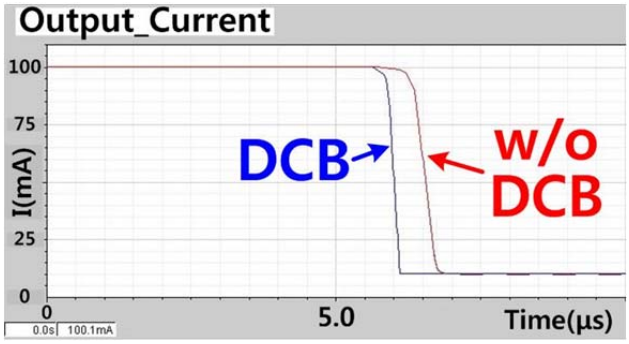


Fig. 6. Final circuit for the proposed low-dropout (LDO) regulator.



(a)



(b)

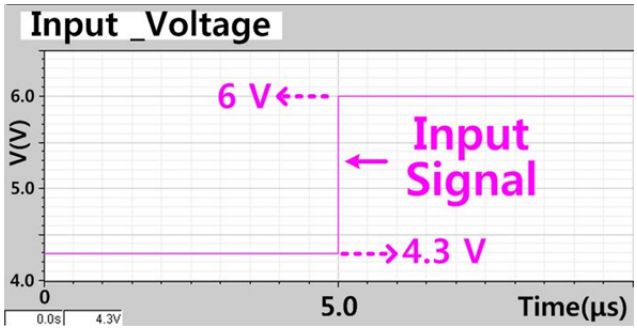
Fig. 7. Simulation results for load transients. (a) Output voltage, (b) output current.

wide range of about 4.3–7 V and the dropout voltage was about 300 mV. Power supply rejection ratio was obtained as 35 dB at 10 kHz. The overshoot of the LDO regulator was measured in terms of line transient at about 720 mV becausea large input voltge was used, as demonstrated in Fig. 10. Although a high-to-low transition was used for measurement, which is opposite to the simulation, the measured results were the same as those of the simulation. Settling time was obtained as 9 μs for an input voltage of 4.3–6 V, as illustrated in Fig. 10. This is a much faster settling time for a 1.7-V input variation compared to work by other researchers. More results are compared in Table 2. Except for current consumption, all other performances are comparable

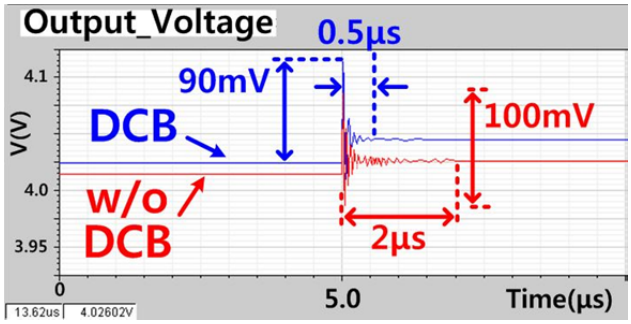
Table 1. Performance summary

V_{DD}	4.3–7 V
V_{DO}	0.3 V
Output current	0–212 mA
I_Q	
No load	3.37 mA@V_O = 4 V, V_{DD} = 4.3 V
Full load	4 mA@V_O = 4 V, V_{DD} = 4.3 V
Line regulation	20 μV/mV@V_O = 4 V, I_{OUT} = 100 mA, V_{DD} = 4.3–7 V
Load regulation	6.317 mV/mA@V_O = 4 V, V_{DD} = 4.3 V
PSRR	35 dB@10 kHz

PSRR = power supply rejection ratio.



(a)



(b)

Fig. 8. Simulation results for line transients. (a) Input voltage, (b) output voltage.

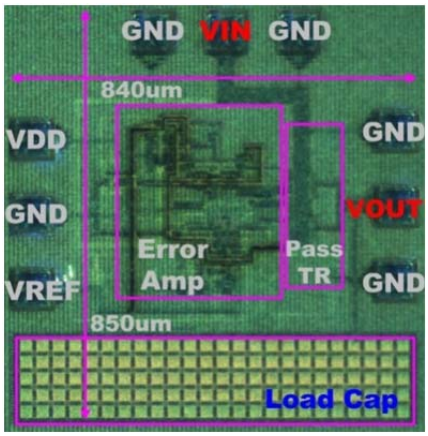


Fig. 9. Microphotograph of the proposed low-dropout (LDO) regulator.

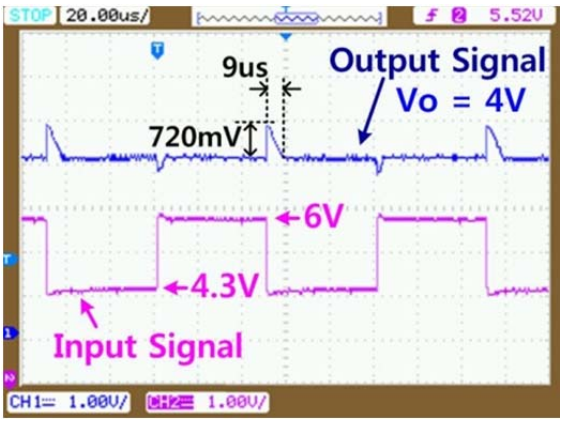


Fig. 10. Measurement results of line transients with 100-pF output capacitor.

Table 2. Comparison of low-dropout (LDO) regulators

	Ho and Mok [7]	Lovaraju et al. [10]	This work
Year	2010	2013	2014
Technology (μm)	0.35	0.18	0.35
V_{OUT} (V)	1.6	1	4
ΔV_{OUT} (mV)			
Load trans.	97	75	3 (sim.)
Line trans.	-	-	90 (sim.) 720 (meas.)
V_{DO} (mV)	200	200	300
I_{OUT} (mA)	100	100	212
I_Q	20 μA	3.7 μA	4 mA
C_{OUT} (pF)	100	100	100
Settling time (μs)	< 9	≈6	≈9

to others' previously pubished circuits.

IV. Conclusions

We proposed an LDO regulator with dynamic current biasing in order to enhance the slew rate. The dynamic current biasing is notturned on in the absence of slewing but acts to enhance the slew rate when slewing occurs. In addition, the input stage of the error amplifier with rail-to-rail structure has a wide range of 4.3–7 V. The linetransient can be recovered within 9 μs foran input voltage with a range of 4.3–6 V.

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References

[1] G. A. Rincon-Mora and P. E. Allen, "Optimized frequency-shaping circuit topologies for LDO's," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 6, pp. 703–708, Jun. 1998.

[2] K. N. Leung, and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.

[3] R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, "Full on-chip CMOS low-dropout voltage regulator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 9, pp. 1879–1890, Sep. 2007.

[4] W. J. Huang, S. H. Lu, and S. I. Liu, "A capacitor-free CMOS low dropout regulator with slew rate enhancement," in *Proceedings of the International Symposium on VLSI Design, Automation and Test*, Hsinchu, China, 2006, pp. 1–4.

[5] C. M. Chen and C. C. Hung, "A capacitor-free CMOS low-dropout voltage regulator," in *Proceedings of the International Symposium on Circuits and Systems (ISCAS2009)*, Taipei, Taiwan, 2009, pp. 2525–2528.

[6] X. Liu, S. Wang, S. Guo, and Y. Chang, "Design of off-chip capacitor-free CMOS low-dropout voltage regulator," in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS2008)*, Macao, China, 2008, pp. 1316–1319.

[7] E. N. Y. Ho and P. K. T. Mok, "A capacitor-less CMOS active feedback low-dropout regulator with slew-rate enhancement for portable on-chip application," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 2, pp. 80–84, Feb. 2010.

[8] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp. 1505–1513, Dec. 1994.

[9] J. Y. Choi, K. Y. Min, and C. S. Yoo, "High-speed and low-power analog source driver for TFT-LCD using dynamic current biased operational amplifier," *SID Symposium Digest of Technical Papers*, vol. 38, no. 1, pp. 1647–1650, May 2007.

[10] C. Lovaraju, A. Maity, and A. Patra, "A capacitor-less low drop-out (LDO) regulator with improved transient response for system-on-chip applications," in *Proceedings of the 26th International Conference on VLSI Design and the 12th International Conference on Embedded Systems,* Pune, India, 2013, pp. 130–135.

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