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Effect of Sputtering Power on the Change of Total Interfacial Trap States of SiZnSnO Thin Film Transistor

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Thin film transistors (TFTs) with an amorphous silicon zinc tin oxide (a-2SZTO) channel layer have been fabricated using an RF magnetron sputtering system. The effect of the change of excitation electron on the variation of the total interfacial trap states of a-2SZTO systems was investigated depending on sputtering power, since the interfacial state could be changed by changing sputtering power. It is well known that Si can effectively reduce the generation of the oxygen vacancies. However, The a-2SZTO systems of ZTO doped with 2 wt% Si could be degraded because the Si peripheral electron belonging to a p-orbital affects the amorphous zinc tin oxide (a-ZTO) TFTs of the s-orbital overlap structure. We fabricated amorphous 2 wt% Si-doped ZnSnO (a-2SZTO) TFTs using an RF magnetron sputtering system. The a-2SZTO TFTs show an improvement of the electrical property with increasing power. The a-2SZTO TFTs fabricated at a power of 30 W showed many of the total interfacial trap states. The a-2SZTO TFTs at a power of 30 W showed poor electrical property. However, at 50 W power, the total interfacial trap states showed improvement. In addition, the improved total interfacial states affected the thermal stress of a-2SZTO TFTs. Therefore, a-2SZTO TFTs fabricated at 50 W power showed a relatively small shift of threshold voltage. Similarly, the activation energy of a-2SZTO TFTs fabricated at 50 W power exhibits a relatively large falling rate (0.0475 eV/V) with a relatively high activation energy, which means that the a-2SZTO TFTs fabricated at 50 W power has a relatively lower trap density than other power cases. As a result, the electrical characteristics of a-2SZTO TFTs fabricated at a sputtering power of 50 W are enhanced. The TFTs fabricated by rf sputter should be carefully optimized to provide better stability for a-2SZTO in terms of the sputtering power, which is closely related to the interfacial trap states.

Keywords: RF magnetron sputtering, Activation energy, Total interfacial trap state, Sputtering power, Amorphous structure

1. INTRODUCTION

Amorphous oxide semiconductor thin film transistors are promising next generation materials for use as active channel layers to replace conventional amorphous silicon. Amorphous silicon TFTs have a low mobility of less than 1 cm^2/Vs. Amorphous oxide semiconductor (AOS) TFTs have shown high mobility due to their ns-orbital overlap structure. In addition, AOS thin films have advantages of low temperature in device fabrication and transparency in the visible range due to a large band gap [1-3]. However, the stability of AOS TFTs under thermal and bias stress has been an issue for practical applications.

It is well known that the total interfacial trap states have an effect on the behavior of the threshold voltage shift under the various stresses [4]. Recently, indium-gallium-zinc-oxide (IGZO) has been considered as one of the most promising channel materials of AOS TFTs because of its low processing temperature for flexible display panels, high carrier mobility for large display screens, and excellent transparency compared with a-Si based TFTs.

However, the IGZO channel has disadvantages such as high cost of indium. Thus, indium-free AOS channel materials such as zinc-tin-oxide (ZTO) have been studied [5]. However, the stability of ZTO TFTs needs to be improved for practical applications be-

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cause the threshold voltage changes after bias stress. This change induces a serious error in the electrical device. The instability of the ZTO TFTs is mainly attributed to the carrier trapping in the trap state on the interface of the active layer. Also, this behavior can cause low mobility and degradation of the subthreshold swing. A recent paper demonstrated that doping with a suppressor, such as Si, Hf, or Zr (which have high oxygen binding energy in ZTO semiconductor materials), can lead to enhanced stability under bias and temperature stress [6-8]. These elements are considered to have important roles in the reduction of oxygen vacancy by strongly binding with oxygen. In this study, we fabricated amorphous 2wt.% Si-doped ZnSnO(a-2SZTO) TFTs using a RF magnetron sputtering system. Since silicon is easily combined with oxygen, it can change carrier concentration in Zn-based TFTs. We used silicon as an oxygen vacancy suppressor in order to improve stability. However, 2wt.% Si-doped ZnSnO can degrade a-SZTO systems because Si peripheral electron belonging to p-orbital can degrade the property of the amorphous zinc tin oxide (a-ZTO) TFTs having an s-orbital overlap structure. In this study, we observed a number of total interfacial trap states of a-2SZTO thin film transistors, depending on the deposition power. We investigated the mechanism of temperature stress related to the change of the total interfacial trap states of a-2SZTO TFTs changed by deposition power, resulting in a change of the temperature stability.

2. EXPERIMENTS

We fabricated a-2SZTO TFTs on a SiO_2 gate insulator on highly doped Si. Fig.1 shows a schematic diagram of the bottom gate a-2SZTO TFTs. A highly doped p-type Si substrate served as the bottom-gate electrode. An RF magnetron sputtering system was used to deposit an a-2SZTO active layer at room temperature. The conditions for sputtering the 2SZTO target were a Ar/O_2 gas mixing ratio of 49:1 and a process pressure of 5 mTorr. A photolithography method and a wet-etching process were used to pattern the layers. A lift-off process was used to define the channel length (L) of 50 μm and width (W) of 250 μm. Au/Ti is used as source/drain electrodes. Ti was deposited using electron beam evaporation and Au was deposited using thermal evaporation. An annealing process was performed at 500℃ for 2 hours to improve the electrical property. In addition, to investigate the effect of sputtering power, we performed deposition at different power values ranging from 30 W to 50 W. The I-V characteristics of TFTs were measured at room temperature, using a semiconductor analyzer. In addition, we confirmed the structural properties of a-2SZTO thin film using X-ray diffraction (XRD) and the electrical stability of a-2SZTO TFTs using a vacuum probe station for a thermal stress test.

3. RESULTS AND DISCUSSION

Figure 2 shows the transfer curves of a-2SZTO TFTs with different sputtering power values deposited using the RF magnetron sputtering system. The measured electrical properties can be calculated as follows.

$$I_D = \frac{WC_i}{2L}\mu_{FE}(V_G - V_{TH})^2$$

W is the channel width, L is the channel length, and C_i is the

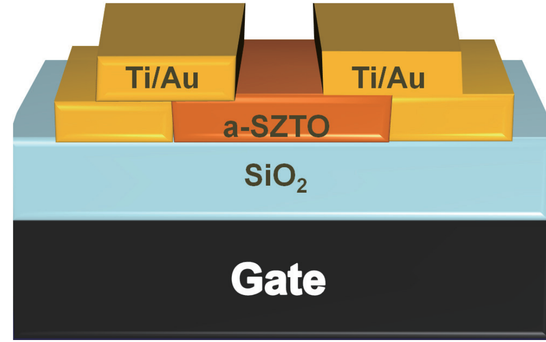

Fig. 1. Schematic view of an a-2SZTO (Si-Zn-Sn-O) thin film transistor.

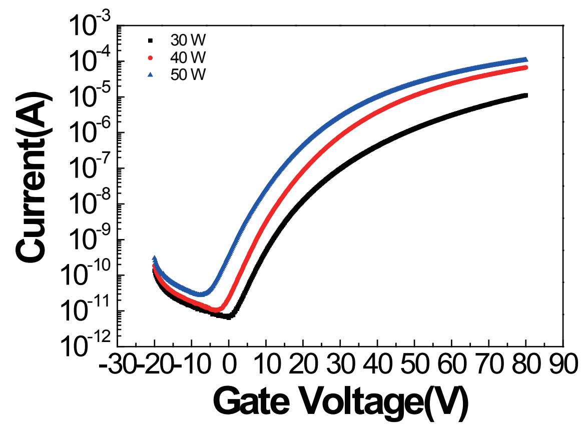

Fig. 2. Transfer curve of a-2SZTO TFTs according to the function of power .

capacitance per unit area of the gate-insulator. I_D is the measured drain current at V_D = 5.1 V and V_{TH} is the threshold voltage. Also, $N_{it.max}$ (total interfacial trap states) can be calculated as follows [9].

$$N_{it.\max} = \left(\frac{S.S\log(e)}{kT/q} - 1\right)\frac{C_i}{q}$$

S.S is the subthreshold swing, k is the Boltzmann constant, and kT/q is 0.0259 eV at 300K. The electrical properties, such as on/off current ratio, threshold voltage, field effect mobility, and total interfacial trap states are summarized in Table 1.

The total interfacial trap states ($N_{it.mat}$) of 1.02E+13/cm^2 of TFT fabricated at sputtering power of 30 W were much larger than those of 7.53E+12/cm^2 and 7.44E+12/cm^2 at 40 W and 50 W. The total interfacial trap states at 50 W are smaller than those of other power value cases. Apparently, when changing the deposition power of the rf magnetron sputtering system, the total interfacial trap states change because of the change of deposition power. This results in the channel film having different interfacial properties since the channel film can change at an early stage of the formation of thin films on a gate insulator. Therefore, the subthreshold swing and field effect mobility were higher at 50 W than at other deposition power value cases. The change in adatom mobility may offer a reasonable explanation. As sputtering power increases, the kinetic energies of the sputtered atoms

Table. 1. Total interfacial trap states of a-2SZTO thin film at different power values.

Deposition power	30 W	40 W	50 W
V_{th}	25.3	17.1	11.9
On/Off Current ratio	1.7E+6	6.5E+6	4.0E+6
mobility	0.550	3.113	4.340
S.S	5.71	4.23	4.18
$N_{it.max}$	1.02E+13	7.53E+12	7.44E+12

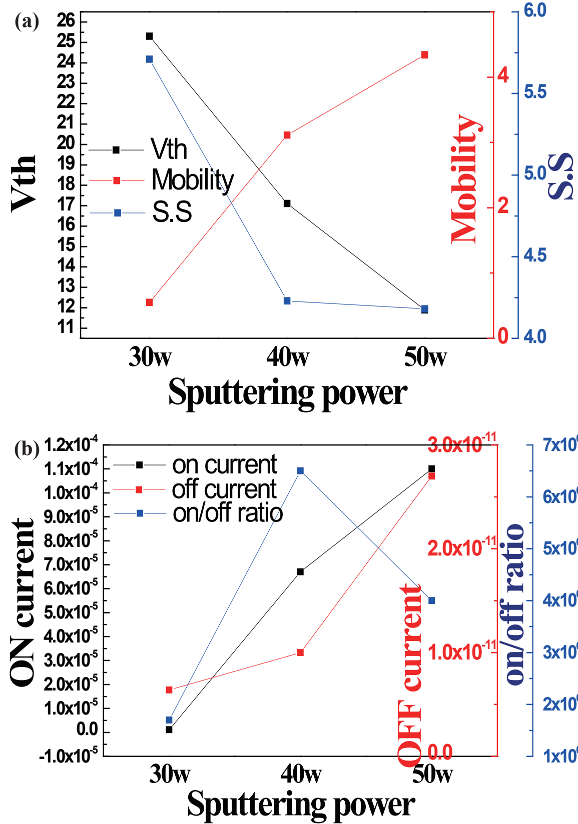

Fig. 3. Electrical property of a-2SZTO at various sputtering powers.

(Si, Zn, Sn, and O) increase. As kinetic energy increases, the adatom mobility increases. Therefore, the energetic bombardment of these adatoms might change the interfacial properties of the channel film and be affected by the interfacial quality at the channel/gate insulator [10]. Figure 3 shows the mobility, S.S, and on/off current ratio of a-2SZTO TFTs at various deposition power values. Figure 3 shows the poor electrical property in the case of a sputtering power of 30 W. However, power at 50 W showed improved electrical property. Since the trap state affects the deposition power, the bulk properties of a-SZTO film deposited at 30 W were improved more than those deposited at 40 W and 50 W. This result agreed well with that of the off current increase and the V_{TH} shifted negatively with increasing rf-power from 30 W to 50 W. Also, the interfacial properties of a-SZTO film deposited at 50 W improved by more than that deposited at 30 W and 40 W; this result well agreed with the subthreshold swing.

Therefore, the a-2SZTO TFTs at a power of 50 W showed a high on current. Therefore, the total interfacial trap states decrease as sputtering power for the a-2SZTO deposition increases, which could be considered to improve the electrical property of TFT.

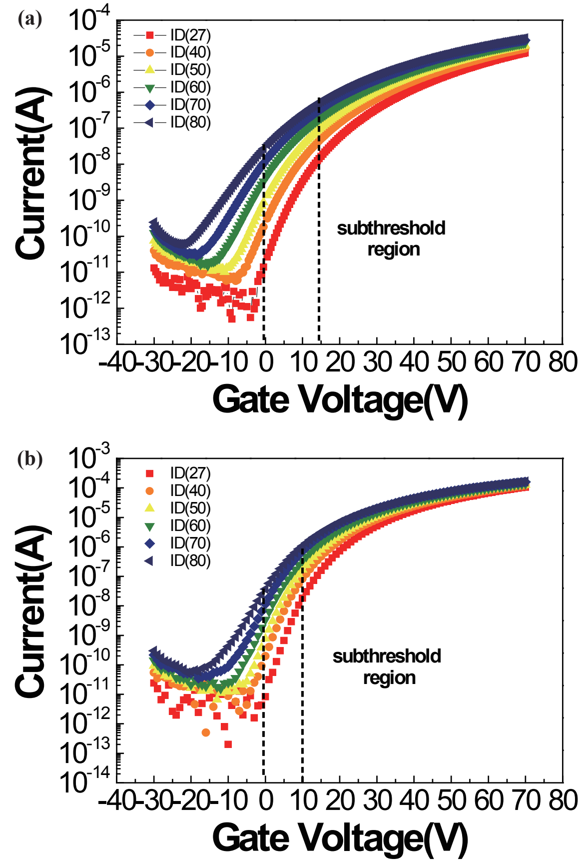

Fig. 4. TS test of a -2SZTO TFTs according to the function of power. (a) 30 W and (b) 50 W.

Figure 4 shows the shift of V_{TH} in a-2SZTO TFTs at 30 W and 50 W in deposition power under thermal stress from 27℃ to 80℃. the V_{TH} shifted negatively as increasing the temperature is mainly due to the generation of thermally activated carriers from traps in the band gap of a-2SZTO. Thermal stress that induced the shift of V_{TH} in the a-2SZTO TFTs was 15.9 V and 11.2 V for a-2SZTO sputtered at sputtering powers of 30 W and 50 W, respectively. Therefore, the total interfacial trap states decreases as the a-2SZTO deposition power increases, which agreed well with the result of thermal stress. The total interfacial trap states that decreased due to increasing deposition power improved the thermal stress stability of a-2SZTO TFTs [11].

Figure 5 shows the activation energy depending on gate voltage for a-2SZTO TFTs with different deposition power values in the subthreshold region. The drain current in the subthreshold region is given as

$$I_D \approx \alpha(V_G - V_{TH})\exp\left[\frac{-E_A(V_G)}{kT}\right]$$

where E_A is the activation energy, k is the Boltzmann constant, and does not rely on the drain current and the temperature. We computed the logarithm of the I_D (V_G-V_{TH}) vs 1/kT [12]. From the results, we evaluated the activation energy for all TFTs. Also, we derived the falling rate for all TFTs using the activation energy due to gate voltage. The values were 0.0178 eV/V and 0.0475 eV/V for the deposition power of 30 W and 50 W, respectively. The

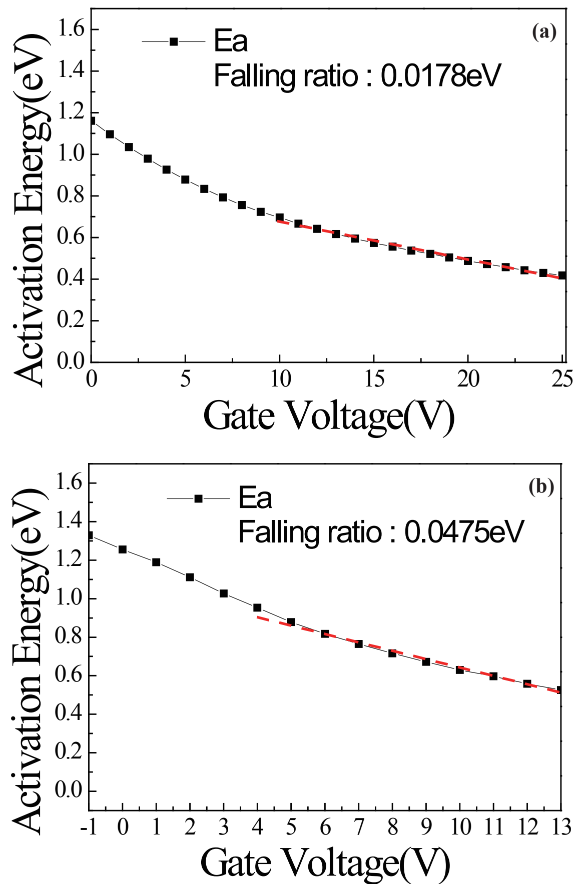

Fig. 5. Activation energy of a-2SZTO TFTs fabricated according to power. (a) 30 W and (b) 50 W.

steep falling rate implies a reduction of total trap density. Therefore, the total interfacial trap states can decrease as the deposition power increases; this also agrees well with the results of the falling rate of TFTs. From the results of falling rates of TFTs, we found that the total interfacial trap states reduce as the deposition power increases. Therefore, we suggest that ΔV_{TH} is mainly due to the variation in total interfacial trap states caused by changing the deposition power, which affects the number of carrier concentrations in a-2SZTO.

Figure 6 shows the XRD patterns of the a-2SZTO thin film with different deposition power values. Only silicon substrate peaks are detected. Therefore, the a-2SZTO thin film shows an amorphous structure, regardless of the deposition power. An amorphous 2SZTO thin film transistor with an amorphous channel layer shows the field effect mobility of 4.34 cm^2/Vs because the ZTO based system of the amorphous structure could generate a conduction path of the s-orbital overlap [13].

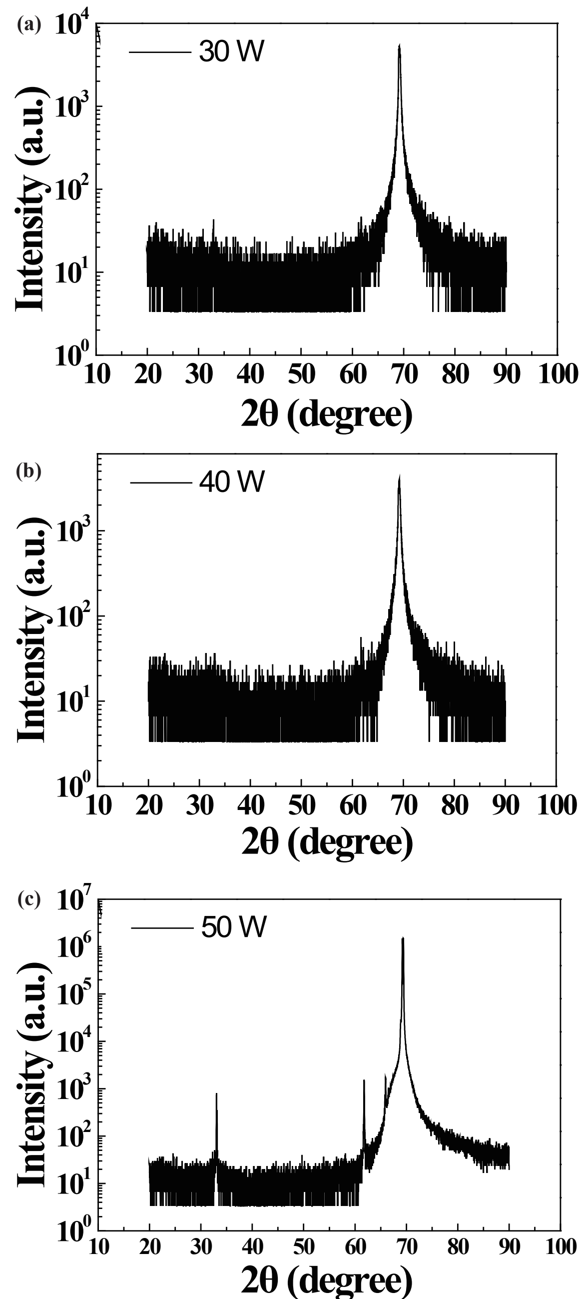

Fig. 6. XRD patterns of the a-2SZTO thin film fabricated according to power. (a) 30 W, (b) 40 W, and (c) 50 W.

4. CONCLUSIONS

In summary, we fabricated a-2SZTO using deposition power. By changing the deposition power of the rf magnetron sputtering system, the total interfacial trap states can be changed because of the change of deposition power resulting in the different interfacial properties of the channel film. We found that the total interfacial trap states are reduced with an increase in the deposition power. Therefore, the total interfacial trap states decrease as the a-2SZTO deposition power increases; this concurred with the result of thermal stress measurement. Reduced total interfacial trap states by increasing the deposition power improve the stability of thermal stress. The higher falling rate of the activation energy implies a reduction in the total interfacial trap states. From the results of falling rates, we found that the total interfacial trap states are reduced with increasing the deposition power. This confirms that the electrical characteristics a-2SZTO improve with deposition power. Also, the improvement of the total interfacial trap states improves the thermal stability of a-2SZTO TFTs. The electrical characteristics are therefore improved with deposition power and the TFTs fabricated by rf sputter should be carefully optimized to provide better stability for a-2SZTO in terms of power.

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