Gate All Around Metal Oxide Field Transistor: Surface Potential Calculation Method including Doping and Interface Trap Charge and the Effect of Interface Trap Charge on Subthreshold Slope

Faraz Najam, Sangsig Kim, and Yun Seop Yu

Abstract—**An explicit surface potential calculation method of gate-all-around MOSFET (GAAMOSFET) devices which takes into account both interface trap charge and varying doping levels is presented. The results of the method are extensively verified by numerical simulation. Results from the model are used to find qualitative and quantitative effect of interface trap charge on subthreshold slope (SS) of GAAMOSFET devices. Further, design constraints of GAAMOSFET devices with emphasis on the effect of interface trap charge on device SS performance are investigated.**

Index Terms—**Compact model, drain-source current, gate-all-around metal-oxide-semiconductor-field-effect-transistor (GAAMOSFET), interface trap distribution, scaling theory**

I. INTRODUCTION

With options running out to sustain the conventional planar MOSFET design at extremely scaled lengths affected by short channel effects (SCEs), alternate structures and materials are being tested including the FinFET and gate-all-around MOSFET (GAAMOSFET) design. GAAMOSFET has been labeled as the future building block of nanoelectronics [1].

The scaling theory presented in [2] investigates design constraints of GAAMOSFET devices. The study determines device dimensions including silicon channel radius R and dielectric thickness t_{ox} (essential in controlling the SCEs inherent in the device) necessary to maintain an acceptable subthreshold slope (SS) performance of the device. However, this scaling scheme is for ideal surrounding gate devices; the theory neglects the impact of interface trap charge on GAAMOSFET device SS performance. It is well documented that the interface trap density of states found at the silicon/dielectric boundary are responsible for SS degradation of the device [3].

Further, most available GAAMOSFET analytical models don't take channel doping into consideration and also ignore the critical interface trap charge parameter [4, 5]. In recent times however a few models have come up that do consider interface trap charge and/or channel doping concentration [6, 7]. Z. Chen et al. [6], for instance considers interface trap charge but ignores the important doping parameter, and Y. S. Yu et al. [7] considers interface trap charge as well as channel doping concentration but only considers one interface trap level in the bandgap. B. H. Hong et al. [8] used the same methodology as [7], i.e. empirical fitting of interface trap charge parameter using only one interface trap level in the bandgap, but undoped channel was considered in [8]. Practical MOSFETs exhibit a range of SS values in the

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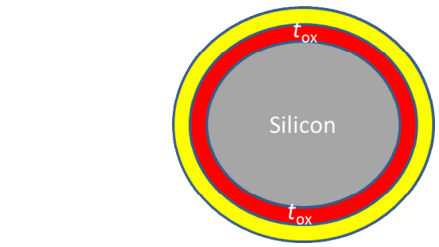
F. Najam and S. Kim are with School of Electrical Engineering, Korea University, Seoul 136-701, Korea.
Y. S. Yu is with the Department of Electrical, Electronic and Control Engineering and IITC, Hankyong National University, Anseong 456-749, Korea.
E-mail : ysyu@hknu.ac.kr

subthreshold region which equates to the presence of interface trap states distributed throughout the bandgap [9-11]. Therefore, for realistic modeling, it should not consider one interface trap level in the bandgap, but it should consider an interface trap distribution in the bandgap. Further, the channel doping concentration also affects the surface potential [12], although the GAAMOSFETs devices are generally low doped but there is inherently some unintentional channel doping concentration present owing to the fabrication process. It can thus be safely concluded that with the limitations mentioned above, the available GAAMOSFET compact models don't meet the requirements for realistic modeling. An analytical surface potential model that takes into account both interface trap charge parameter considering *interface trap distribution* and *channel doping concentration* is thus highly desirable.

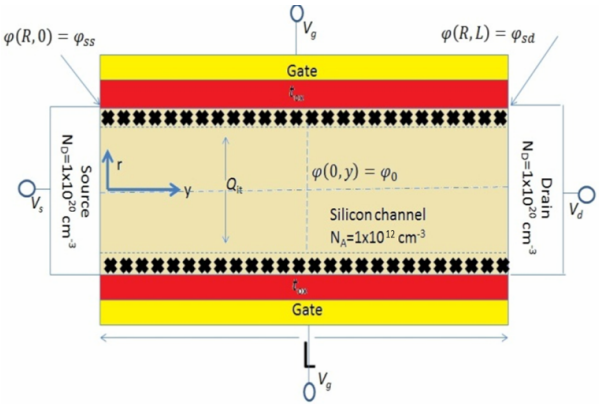
In our previous work [13] we introduced an implicit GAAMOSFET surface potential based drain current compact model that takes into account interface trap charge distribution. The model is iterative and does not consider channel doping concentration. In this study we present an explicit, non-iterative surface potential calculation-method that simultaneously takes into account interface trap states as well as channel-doping concentration in surface potential calculation of GAAMOSFET. The model is presented in section II and verified extensively by 3D numerical simulation. The results from the model are used to find the qualitative and quantitative impact of interface trap charge on *SS* degradation (Section III) (by using our previously reported extracted interface trap charge values) by employing the aforementioned scaling theory. Design constraints of GAAMOSFET device are investigated with emphasis on the effect of interface trap charge on device *SS* performance.

II. MODEL FORMULATION

Schematic of GAAMOSFET is shown in Fig. 1. Here r is the cylindrical coordinate along the radius, R is radius of silicon, t_{ox} is the gate oxide thickness, L is channel length along the y direction, source/drain doping considered is 1×10^{20} cm^{-3}, N_A is channel doping, interface trap charge Q_{it} is found at the silicon/gate-oxide interface throughout the channel, and gate, source, and drain bias



(a)



(b)

Fig. 1. (a) Schematic cross-section of the simulated GAAMOSFET device,(b) Side-on view of the simulated doped GAAMOSFET device.

are V_g, V_s, and V_d, respectively. φ is the potential, and φ_s and φ_o are the surface and center potentials, respectively. The standard doped 1D cylindrical coordinate Poisson-Boltzmann equation is given by

$$\frac{d^2\varphi}{dr^2}+\frac{1}{r}\frac{d\varphi}{dr}=\frac{qN_A}{\varepsilon_{si}}\left[1+\left(\frac{n_i}{N_A}\right)^2\exp(\frac{\varphi-V_{ch}}{v_{th}})\right], \quad (1)$$

$$n=\left(\frac{n_i^2}{N_A}\right)\exp(\frac{\varphi-V_{ch}}{v_{th}}), \quad (2)$$

where q is the electronic charge, ε_{si} is the permittivity of silicon, n and n_i are the induced electron concentration and intrinsic carrier concentration in cm^{-3}, respectively, V_{ch} is the drain-source bias, and v_{th} is the thermal voltage ($=kT/q$, k is the Boltzmann constant and T is temperature). The boundary conditions for (1) are given by

$$\left.\frac{d\varphi}{dr}\right|_{r=0}=0, \quad \varphi(r=R)=\varphi_s, \quad \varphi(r=0)=\varphi_0, \quad (3)$$

According to Gauss's law, the total charge Q_T is given by the following equation,

$$Q_T = C_{ox}\left(V_{gs} - \Delta\phi + \frac{Q_{it}}{C_{ox}} - \varphi_s\right) = \varepsilon_{si}\frac{d\varphi}{dr}, \qquad (4)$$

where V_{gs}, $\Delta\phi$, and C_{ox} are the gate-source bias, workfunction difference, and gate capacitance, respectively. No analytical solution exists for (1) using the normal integration routine due to the non-linear coupling effect between the induced charge and the depletion charge. However, for low doped silicon body, the coupling effect between the depletion charge and the inversion charge is not very strong, as the two parameters dominate different device operating regions. This ensures that the Poisson equation can be solved using the super-position principle. It must be pointed out that the super-position principle is only valid for low doping concentration and breaks down for a channel doping concentration exceeding 10^{18} cm^{-3}. This upper limit, however, is not of practical importance to GAAMOSFET devices in which the channel is undoped. The only doping present is unintentional doping which is process induced and lies well within the upper limit value [14-16].

After solving Poisson equation for induced carrier charge and depletion charge and using the super-position principle, the final solution is given by,

$$\varphi_s = \varphi_0 + \sqrt{\frac{qN_AR^2}{16\varepsilon_{si}}(\varphi_s - \varphi_0)} - 2v_{th}\ln\left(1 - \frac{R^2}{8L_D}\frac{n_o}{N_A}\right), \qquad (5)$$

where n_o is the induced electron concentration in the center of the channel and L_D is the Debye length of the silicon channel in cm. Total charge $Q_T = Q_{dep} + Q_{inv}$ is given by [17]

$$Q_T = \sqrt{q\varepsilon_{si}N_A(\varphi_s - \varphi_0)} + \frac{\varepsilon_{si}Rv_{th}}{2L_D^2}\frac{n_o/N_A}{1 - \frac{R^2}{8L_D}\frac{n_o}{N_A}}, \qquad (6)$$

Substituting (5) and (6) in (4), and using the Lambert W function we get a closed-form solution of surface potential φ_s as follows [18],

$$\varphi_s = V_{gs} - \Delta\phi + \frac{Q_{it}}{C_{ox}} - \frac{qN_AR}{2\varepsilon_{si}} - 2v_{th}W_0\left\{\frac{\varepsilon_{si}R}{4C_{ox}L_D^2}\left(\frac{n_i^2}{N_A}\right)\cdot \exp\left[\frac{1}{2v_{th}}\left(\varphi_0 - 2V_{ch} - \frac{qN_AR^2}{4\varepsilon_{si}} + V_{gs} - \Delta\phi + \frac{Q_{it}}{C_{ox}} - \frac{qN_AR}{2\varepsilon_{si}}\right)\right]\right\}, \qquad (7)$$

where W_0 is the principal branch of the Lambert-W function. Eq. (7) contains an additional interface trap charge term (Q_{it}) as compared to the surface potential equation given in [15]. For center potential, the following smoothing function is used.

$$\varphi_0 = \frac{1}{2}\left[(\varphi_{0\max} + \varphi_{0a}) - \sqrt{(\varphi_{0\max} + \varphi_{0a})^2 + \delta\varphi_{0\max}\varphi_{0a}}\right], \qquad (8)$$

$$\varphi_{0a} = V_{gs} - \Delta\phi + \frac{Q_{it}}{C_{ox}} - \frac{qN_AR^2}{4\varepsilon_{si}} - \frac{qN_AR}{2\varepsilon_{si}}, \qquad (9)$$

$$\varphi_{0\max} = V_{ch} + 2\phi_F + v_{th}\ln\left(\frac{8L_D^2}{R^2}\right), \qquad (10)$$

Interface trap charge Q_{it} is given by [19]

$$Q_{it} = (-q)\int_{\frac{E_g}{2}}^{E_c} D_{it}(i)F_{tA}(i)dE_{it}, \qquad (11)$$

$$F_{tA}(i) = \frac{c_{ns}n_s + e_{ps}}{c_{ns}n_s + e_{ns} + c_{ps}p_s + e_{ps}}, \qquad (12)$$

where $F_{tA}(i)$ is the probability of occupation of acceptor trap states which is evaluated for all of the k interface trap states each defined at ith energy level, $D_{it}(i)$ is the interface trap density (cm^{-2}eV^{-1}) defined at ith energy level, and c_{ns}, c_{ps}, e_{ns}, e_{ps}, n_s, and p_s are the electron capture coefficient and hole capture coefficient, electron emission coefficient, hole emission coefficient, surface electron carrier($=n_i\exp((\varphi_s-\varphi_{FN})/v_{th})$, where φ_{FN} is the electron quasi fermi level) and surface hole carrier concentration($=n_i\exp((\varphi_{FP}-\varphi_s)/v_{th})$, where φ_{FP} is the hole quasi fermi level), respectively.

Eq. (7) contains an additional interface trap charge term (Q_{it}) as compared to the surface potential equation given in [18]. From (12), Q_{it} is dependent on surface potential through the electron and hole surface carrier concentration terms n_s and p_s. Also, calculation of φ_s requires knowledge of Q_{it} (from (7)). Therefore, solution for Q_{it} and φ_s requires an exhaustive self-consistent calculation of both Q_{it} and φ_s terms. Any available

interface trap density D_{it} could be used in self-consistent calculation of Q_{it} and φ_s parameters. The self-consistent calculation procedure has been explained in our previous work [13]. By using this method, interface trap charge can be applied to compact models of MOSFET or multi-gate MOSFETs [2, 4, 5, 7, 20-22].

Fig. 2 shows the surface potential φ_s as a function of gate voltage V_{gs}. A standard numerical simulation tool [23] was used to compare the results of the analytical model (lines) with the 3D numerical simulation results (symbols) as shown in Fig. 2. Drift-Diffusion transport model, constant mobility model, Fermi-Dirac statistics, and *Shockley-Read-Hall* recombination model were used in the simulation. Fig. 1(b) shows the simulated cross-section of the GAAMOSFET. The numerical simulation and analytical model results are in excellent agreement. Our method includes both the interface trap state distribution and channel doping concentration parameters which is the main advantage of our method over [4-6] which either ignore one or the other or both parameters, and Ref. [7] which considers only one interface trap level whilst taking into account channel doping concentration. Further, our model has advantage over BSIM.CMG model as our model allows user definable input of interface trap density of states value through the D_{it} parameter in (11), whereas BSIM.CMG is an empirical model based on input of fixed, previously extracted interface trap capacitance (C_{it}) values [22, 24].

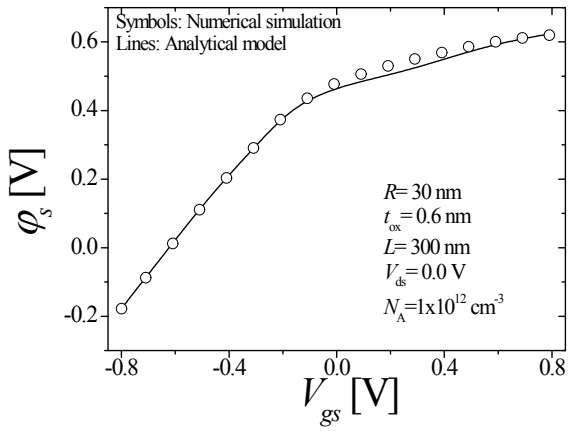


Fig. 2. Surface potential (φ_s) calculated from the analytic model compared with that extracted from numerical simulation, for N_A=1×10^{12} cm^{-3} shown for both source and drain sides (symbols: numerical simulation, lines: analytical model).

III. QUALITATIVE EFFECT OF INTERFACE TRAP STATES ON DEVICE SS PERFORMANCE

The scaling theory presented in [2] gives design constraints of GAAMOSFET devices. Device dimensions including silicon channel radius R and oxide thickness tox are isolated in a term called λ in the solution of poisson equation given by the following equation [25, 26].

$$\frac{d^2\varphi(y)}{dy^2} - \frac{\varphi(y) - V_{gs}}{\lambda^2} = \frac{qN_A}{\varepsilon_{si}}, \tag{13}$$

where λ is given by

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} \frac{R^2}{2} \ln\left(1 + \frac{t_{ox}}{R}\right) + \frac{R^2}{4}}. \tag{14}$$

The scaling factor α is expressed as

$$\alpha = \frac{L_{EFF}}{2\lambda}, \tag{15}$$

where L_{EFF} is device's channel length and λ term contains the short channel effects inherent in the device. According to the theory, in order to maintain a constant *SS* and drain induced barrier lowering (DIBL) value the scaling factor α needs to be maintained at a value > 2.3. With interface trap charge considered the *SS* increases. The increase in *SS* adds an extra dimension to the scaling requirements in addition to the usual scaling scheme employed.

The results of the original scaling scheme are shown in Fig. 3 and compared with the new scaling scheme including the effect of interface trap charge. Symbols and lines denote numerical simulation and analytical model results, respectively. Black squares (and solid line) represent results with no interface trap charge considered (original scaling theory results), red circles (and dotted line) include results with Q_{it} considered resulting in an increased *SS*, and blue triangles (and dashed line) show scaled devices to achieve an optimum *SS* value. Comparing black and blue symbols, it appears that α needs to be increased by approximately 31% to achieve a *SS* value close to 60 mV/dec to compensate for *SS*

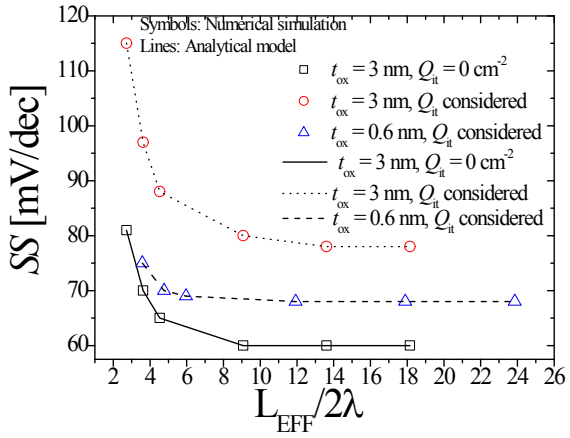


Fig. 3. Subthreshold slope (*SS*) versus scaling factor (α). Symbols and lines denote numerical simulation and analytical model, respectively. Black squares (solid line) and red circles (dotted line) denote the results of the original scaling theory with Q_{it}=0 cm^{-2} and Q_{it} considered for t_{ox}=3 nm, respectively, and blue triangles (dashed line) denote the results for the scaled devices with Q_{it} considered for t_{ox}=0.6 nm. Device parameters: R=30 nm and L_{EFF} =300 nm.

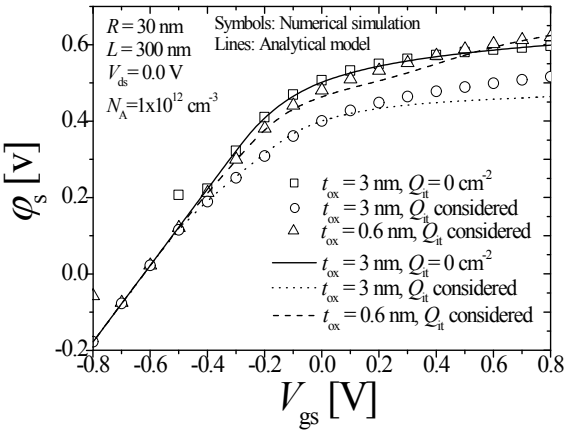


Fig. 4. Surface potential (φ_s) versus gate bias. Symbols and lines denote numerical simulation and analytical model, respectively. Squares and solid line: device with t_{ox}=3 nm and Q_{it}=0 /cm^2. Circles and dotted line: device with t_{ox}=3 nm and Q_{it} considered. Triangles and dashed line: device with t_{ox}=0.6 nm and Q_{it} considered.

degradation due to interface trap charge.

This optimization (decrease in *SS*) was achieved by scaling t_{ox} from 3 nm (red symbols and dotted line) to t_{ox} = 0.6 nm (blue symbols and dashed line) which results in an increase of the α value as shown in Fig. 3.

Decreasing t_{ox} increases the gate capacitance C_{ox} which in turn helps reduce the *SS* values according to the following equation [3].

$$SS = v_{th} \ln(10) \frac{C_{ox} + C_D + C_{it}}{C_{ox}}, \qquad (16)$$

where C_D is the depletion capacitance. Fig. 4 shows the surface potential φ_s as a function of gate voltage V_{gs} at different gate oxide thickness and interface trap charges. It shows the corresponding surface potential and total capacitance. Symbols and lines denote numerical simulation and analytical model, respectively. With t_{ox}=3 nm, the presence of Q_{it} severely degrades the surface potential (circles and dotted line). By scaling t_{ox} from 3 nm with Q_{it} considered (circles and dotted line) to t_{ox} = 0.6 nm with Q_{it} considered (triangles and dashed line) restores the surface potential as compared to the ideal (Q_{it} = 0) case (squares and solid line).

Device with a thinner t_{ox} clearly shows less effect of interface trap charge on device surface potential because of increased gate capacitance, according to the following expression.

$$\frac{1}{C_T} = \frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}}, \qquad (17)$$

where C_T is the absolute total capacitance, C_s is the semiconductor capacitance. Total capacitance C_T of 2 devices with equivalent Q_{it} but different t_{ox} is shown in Fig. 5. Symbols and lines denote numerical simulation and analytical model, respectively. The increased C_{ox} value due to thinner t_{ox}=0.6 nm (squares and solid line) then dominates the total capacitance value C_T, resulting in an increase in C_T value as shown in Fig. 5. The device with thicker t_{ox}=3 nm (circles and dashed line) shows lower C_T as compared to the device with thinner t_{ox} (squares and solid line). Equivalent interface trap charge parameter Q_{it} was considered for both the thin t_{ox} (=0.6 nm) and thick t_{ox} (=3 nm) cases.

For a given silicon channel radius R and channel length, the minimum oxide thickness to maintain a *SS* value of < 80 mV/dec was determined, shown in Fig. 6. Symbols and lines denote numerical simulation and analytical model, respectively. Scaling channel radius doesn't have a pronounced effect on device's *SS* performance as far as the impact of interface trap charge is concerned for a reasonably long channel device i.e. 300 nm (squares and solid line) as shown in Fig. 5, i.e. a

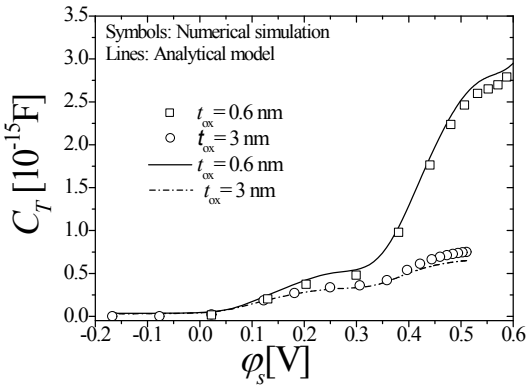


Fig. 5. Total capacitance C_T versus respective surface potentials for 0.6 nm and 3 nm of t_{ox} values, R=30 nm and L_{EFF}=300 nm, both with Q_{it} considered. Symbols and lines denote numerical simulation and analytical model, respectively. Device with thinner t_{ox} = 0.6 nm (squares and solid line) shows greater total capacitance despite the presence of equivalent interface trap states then device with t_{ox}=3 nm (circles and dashed line).

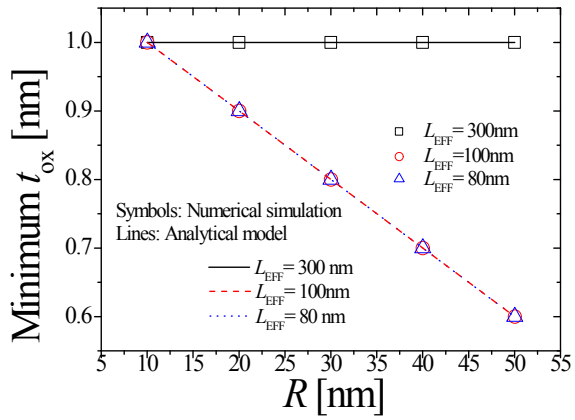


Fig. 6. Minimum t_{ox} needed to maintain a SS value of < 80 mV/dec as a function of channel radius R. Symbols and lines denote numerical simulation and analytical model, respectively.

constant t_{ox} of 1 nm is required to maintain a SS < 80 mV/dec for different R-values. However, in order to compensate both for the SCEs and the effect of interface trap states of shorter channel length devices t_{ox} needs to be scaled by a factor of about 10% (with 1 nm as the reference) for every 10 nm increase in R (red, blue symbols and dashed, dotted lines in Fig. 6 representing L_{EFF}=100 nm and 80 nm, respectively). For L_{EFF} < 80 nm, a t_{ox} < 0.6 nm was found to be required to maintain a SS < 80 mV/dec which would be impractical in realistic devices.

IV. CONCLUSIONS

Surface potential calculation method with the consideration of interface trap charge parameter and doped silicon channel was introduced. The model was found to be in excellent agreement with 3D numerical simulation results. Design constraints of GAAMOSFET device with emphasis on the impact of interface trap on devices' SS were discussed, by employing a GAAMOSFET scaling theory. It was found that the natural length needed to be increased by about 31 % to achieve a SS of close to 60 mV/dec and minimum oxide thickness needed to be approximately 1 nm to achieve a SS of <80 mV/dec for a relatively long channel device whereas, for shorter channel length devices i.e. up to 80 nm, t_{ox} needed to be scaled by 10 about 10 % for every 10 nm increase in R. Devices with channel lengths < 80 nm were found to require impractically small t_{ox} < 0.6 nm to achieve a SS < 80 mV/dec.

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Faraz Najam received M.S degree in Nanoelectronics from University of Southampton in 2008 and is currently in the process of completing his Ph.D. degree from Korea University. His main research interests include analytical modeling, process development, and process-device integration of multiple gate nano-devices. He is also interested in fabrication and characterization of emerging nano-devices including Tunnel FETs and alternate channel material devices including Germanium and Graphene

Sangsig Kim received the B.S. and M.S. degrees in physics from Korea University, Seoul, Korea, in 1985 and 1987, respectively, and the Ph. D. degree in applied physics from Columbia University, NY, USA, in 1996. From 1996 to 1998 he was a Postdoctoral Fellow with the Department of Electrical Engineering at University of Illinois at Urbana-Champaign (UIUC), IL, USA. Since 1999, he has been a Professor of Electrical Engineering at Korea University. He has focused his research on the synthesis of nanomaterials including nanowires and nanocrystals, and their optical and electrical characterization. In addition, he is also engaged in the fabrication of flexible nanodevices including thermal-electric devices, switching devices, nonvolatile memory devices, and logic circuits. He is the author and coauthor of more than 200 peer reviewed publications.

Yun Seop Yu received the B.S., M.S., and Ph. D. degrees in electronics engineering from Korea University, Seoul, Korea, in 1995, 1997, and 2001, respectively. From 2001 to 2002, he worked as a guest researcher at the Electronics and Electrical Engineering Laboratory in NIST, Gaithersburg, MD. He is now an Associate Professor with the Department of Information & Control Engineering at Hankyong National University, Anseong, Korea. His main research interests are in modeling various nano-devices for efficient circuit simulation, and future memory, logic, and sensor designs using those devices. He is also interested in the fabrication and characterization of various nano devices, as well as their future applications in memory, logic, and sensors. He has authored and coauthored more than 60 refereed international journal papers.