Monte Carlo Simulation Study: the effects of double-patterning versus single-patterning on the line-edge-roughness (LER) in FDSOI Tri-gate MOSFETs

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Abstract—**A Monte Carlo (MC) simulation study has been done in order to investigate the effects of line-edge-roughness (LER) induced by either 1P1E (single-patterning and single-etching) or 2P2E (double-patterning and double-etching) on fully-depleted silicon-on-insulator (FDSOI) tri-gate metal-oxide-semiconductor field-effect transistors (MOSFETs). Three parameters for characterizing the LER profile [*i.e.*, root-mean square deviation (σ), correlation length (ζ), and fractal dimension (D)] are extracted from the image-processed scanning electron microscopy (SEM) image for each photolithography method. It is experimentally verified that two parameters (*i.e.*, σ and D) are almost the same in each case, but the correlation length in the 2P2E case is longer than that in the 1P1E case. The 2P2E-LER-induced V_{TH} variation in FDSOI tri-gate MOSFETs is smaller than the 1P1E-LER-induced V_{TH} variation. The total random variation in V_{TH}, however, is very dependent on the other major random variation sources, such as random dopant fluctuation (RDF) and work-function variation (WFV).**

Index Terms—**Variability, line-edge-roughness, fully-depleted silicon-on-insulator, CMOS**

I. INTRODUCTION

In the past few decades, the sustainable development of electron devices (particularly, MOSFETs) has been successfully achieved with the steady miniaturization of their size. As transistors are scaled down below 100-nm, they suffer from various types of random/intrinsic variations such as random dopant fluctuation (RDF), work-function variation (WFV), and line-edge-roughness (LER) [1]. Moreover, it is challenging to implement the desired feature size for every new CMOS generation, due to the limited wavelength of the photolithography system that is currently used. In order to address these technical issues, non-planar transistor architectures such as Fully-Depleted Silicon-On-Insulator (FDSOI) or tri-gate MOSFETs are being seriously considered in industry for the 22/20-nm nodes and below [2, 3]. In addition, the double patterning technique will also be introduced in the production at the 22/20-nm nodes and below.

In this study, the effects of random variation (especially the LER) in FDSOI tri-gate MOSFETs using the 2P2E technique (*vs.* the 1P1E technique) are investigated. In Section II, the LER characterization method using the self-affine edge model will be described with the results of the extracted parameters. In Section III, using the parameters obtained in section II, the Monte Carlo (MC) simulations will be performed in order to investigate the difference between the 2P2E-LER-induced V_{TH} variation and the 1P1E-LER-induced V_{TH} variation.

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II. LER MODELING

1. LER Characterization

In this study, we used the self-affine edge model to characterize the LER profile [4]. Using the model, the LER profile can be characterized with three parameters: (i) the root mean square (RMS) deviation (σ), (ii) correlation length (ζ), and (iii) fractal dimension (D). The RMS deviation, σ, is defined in Eq. (1):

$$\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - x_{mean})^2} \tag{1}$$

where N is the total number of sampling points along the LER profile, x_{mean} is the mean value of x_i, and x_i is the edge deviation away from the line-edge. As shown in Fig. 1, the larger the RMS deviation is, the more the LER profile fluctuates.

The correlation length, ζ, represents the lateral dimension of the line edge, and it can be obtained using the auto-correlation function (ACF) of the LER profile. The ACF is defined in Eq. (2):

$$R(md) = \frac{1}{\sigma^2}\sum_{i=1}^{N-m}(x_{i+m} - x_{mean})(x_i - x_{mean}) \tag{2}$$

where m is an integer, d is the distance between adjacent sample points, and R(0) is 1. The typical auto-correlation function of the self-affine edge model is

$$R(r) = \exp\left(-\left(\frac{|r|}{\zeta}\right)^{2\alpha}\right) \tag{3}$$

where α is the roughness exponent and is generally between 0 and 1. From the aforementioned equations, it is understood that the correlation length is relevant to the spatial morphology of the LER profile, as shown in Fig. 1.

The fractal dimension, D, is the last parameter for characterizing the LER profile, which is related to the roughness exponent, D (= 2 – α). Fig. 2 shows a typical power spectrum of the self-affined line edge. The power spectrum is constant until the spatial frequency is equal to the inverse number of the correlation length. For a spatial frequency higher than the specified value (*i.e.,* f = 1/ζ), the power spectrum decreases with a constant slope, which is related to the fractal dimension, D. As D increases, the slope of the power spectrum becomes smaller, so that the high frequency component of the LER profile becomes larger, as shown in Fig. 1.

2. Extraction of the Parameters from SEM Images

Fig. 3 shows the image-processed scanning electron microscopy (SEM) image of the test structures which were obtained using 28nm CMOS technology. The double-patterning and double-etching (2P2E) technique [versus the single-patterning and single-etching (1P1E) technique] was used in order to investigate its impact on the LER profile. Using the SEM images, three parameters for the LER characterization were extracted:

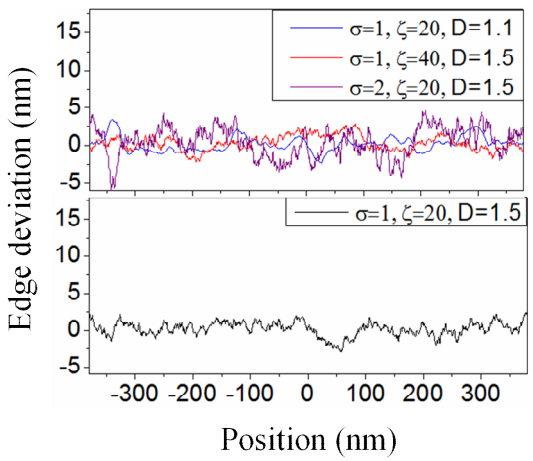

Fig. 1. As compared against a black-colored LER profile in the bottom box, three simulated LER profiles are shown in the top box, each of which is obtained when only RMS deviation (σ), or correlation length (ζ), or fractal dimension (D) is modified.

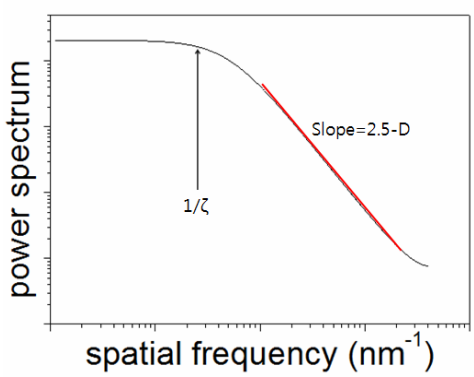

Fig. 2. Typical power spectrum obtained using the self-affine edge model.

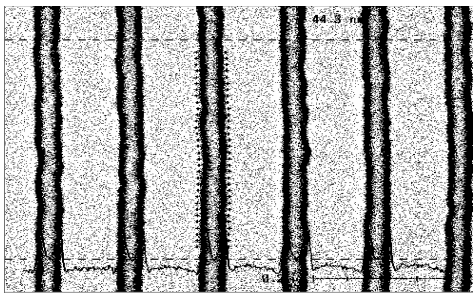

Fig. 3. The image-processed SEM image of the test structures which were used to extract the three parameters for the LER.

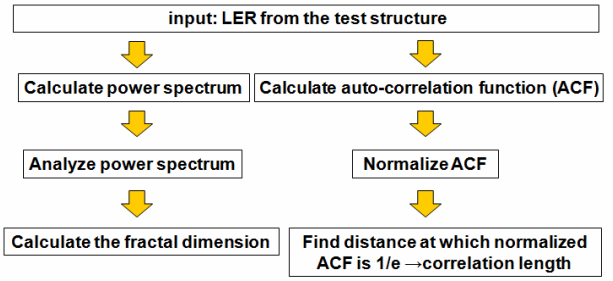

Fig. 4. The steps for extracting the fractal dimension (left part) and the correlation length (right part).

Table 1. The parameters from the 20 test structures [10]

Lithography	σ(nm)	ζ(nm)	D(unit-less)
2P2E	1~2	20~40	1.7~1.9
1P1E	1~2	<15	1.6~1.9

the RMS deviation (σ) is simply extracted by the typical definition of the standard deviation. Then, following the steps shown in Fig. 4, the correlation length (ζ) and the fractal dimension (D) are computed. We extracted the 2P2E-based LER parameters as well as the 1P1E-based LER parameters, in order to study the differences between them.

The extracted parameters are summarized in Table 1.

Two of the LER parameters (*i.e.*, the RMS deviation and the fractal dimension) that were extracted from the test structures are almost the same, regardless of the photolithography method. However, the correlation length of the 2P2E-based LER profile is longer than that of the 1P1E-based LER profile (*i.e.*, lower spatial frequency), because the exposed regions are different from each other during each photolithography process. This would minimize the effect of the 2P2E-LER-induced V_{TH} variation (*vs.* 1P1E-LER-induced V_{TH} variation), because the 2P2E-based LER profile along the channel width direction is more smoothened. This will be verified using the Monte Carlo (MC) simulation in the next section.

III. MONTE CARLO (MC) SIMULATION

1. Nominal Design of the FDSOI Tri-gate MOSFET

Fig. 5 shows the three-dimensional bird's-eye view of the nominal n-type FDSOI tri-gate MOSFET. The design parameters for this device are summarized in Table 2. The height of the source/drain regions is higher than the channel region [5] in order to minimize the impact of the series resistance on the circuits based on the FDSOI tri-gate MOSFETs. Note that the performance metrics to satisfy the LOP specification (*i.e.,* low operating power specifications in the International Technology Roadmap for Semiconductors [6]) are summarized in Table 3.

2. Monte Carlo (MC) Simulation in the FDSOI Tri-gate MOSFETs

Based on the experimental results summarized in

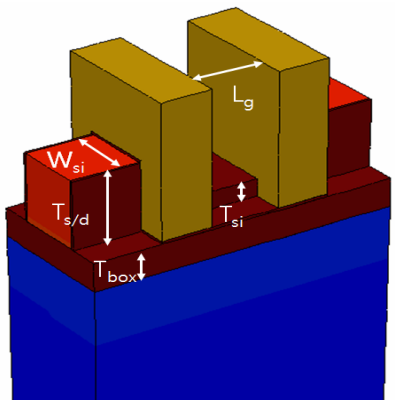

Fig. 5. Three-dimensional (3-D) bird's-eye view of the nominal n-type FDSOI tri-gate MOSFET without showing gate electrode and contacts. The density gradient model was used to take into account the quantum effects.

Table 2. Design parameters for the nominal device

L_g (nm)	20	physical gate length
T_{ox} (Å)	9	effective oxide thickness
ψ_M (eV)	4.5	metal-gate work function
L_{eff} (nm)	40	effective channel length
W_{si} (nm)	20	device width in layout
T_{si} (nm)	6	channel height
T_{box} (nm)	10	BOX thickness
$T_{s/d}$ (nm)	23	raised source/drain height

Table 3. Performance metrics for the nominal device

I_{ON} (μA/μm)	816	on-state current
I_{OFF} (nA/μm)	1.5	off-state current
$V_{TH, lin}$ (mV)	292	linear threshold voltage
$V_{TH, sat}$ (mV)	252	saturation threshold voltage
SS (mV/dec)	68.9	subthreshold swing
DIBL (mV/V)	53.3	drain-induced barrier lowering

Table 4. The parameters used in the MC simulations

Lithography	σ(nm)	ζ(nm)	D(unit-less)
2P2E	1, 1.3, 1.5, 1.7, 2	30	1.9
1P1E	1, 1.3, 1.5, 1.7, 2	15	1.9

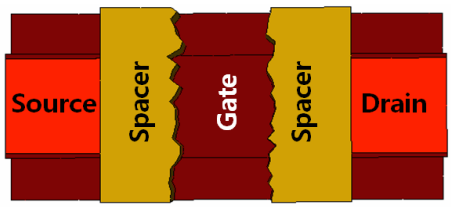

Fig. 6. Plan view of the n-type FDSOI tri-gate MOSFET with the 2P2E-LER profile without the gate electrode, in order to clearly depict the LER profiles.

Table 1, both the 1P1E-LER and 2P2E-LER profiles are utilized in generating each side line of the gate electrode in the FDSOI tri-gate MOSFET. The correlation length and the fractal dimension are chosen as in [10], but the RMS deviation is varied within the range in Table 1 (*i.e.*, 1, 1.3, 1.5, 1.7, and 2). Table 4 summarizes the selected values of the parameters for the MC simulations.

Fig. 6 shows the plan view of the FDSOI tri-gate MOSFET with a 2P2E-LER simulated profile. The left-side's LER profile is very different from the right-side's LER profile, because the spacer lithography was not used. If the spacer lithography were used, the LER profiles on both sides would be strongly correlated, so that the LER profiles are almost identical [7].

The 1,000 different samples were generated to estimate the V_{TH} variation caused by (i) the 2P2E-LER only, (ii) the 2P2E-LER + RDF, and (iii) the 2P2E-LER + RDF + WFV (*vs.* 1P1E cases). The V_{TH} variations induced by the RDF and the WFV are estimated by Sano's method [8] and the RGG method [9], respectively. The RGG method can simply estimate the V_{TH} variation induced by WFV (work-function variation), if the gate area and average grain size of the metal gate material are known. The MC simulation results are summarized in

Table 5. The MC simulation results

V_{TH} variation (mV)	2P2E-LER Only (1P1E-LER only)	2P2E-LER +RDF (1P1E-LER +RDF)	2P2E-LER + RDF + WFV (1P1E-LER + RDF + WFV)
$\sigma(V_{TH, sat})$	2.06 (2.91)	8.47 (8.72)	42.78 (42.83)
$\sigma(V_{TH, lin})$	0.88 (1.2)	4.85 (4.92)	42.21(42.22)

Table 5. It is verified that the V_{TH} variation induced by the 2P2E-LER is slightly smaller than that induced by the 1P1E-LER, as also shown in our previous study [10]. However, regardless of the photolithography method that is used, the total V_{TH} variation is not significantly affected, because the WFV-induced V_{TH} variation [11] is dominant in the variation. However, if the RMS value of the LER is not scaled down anymore, the LER would become dominant source in the total V_{TH} variation (as also shown in [12]). In this scenario (*i.e.,* the LER is the most dominant random variation source), the 2P2E technique could be a way to alleviate the V_{TH} variation. Moreover, it is possible to implement smaller feature sizes using the 2P2E technique.

IV. CONCLUSIONS

Using two different photolithography methods (*i.e.,* 2P2E or 1P1E), we have studied the effects of the LER-induced V_{TH} variation on the FDSOI tri-gate MOSFET. The image-processed SEM image was analyzed to extract three LER parameters for both the 1P1E and 2P2E cases. It is confirmed that the 2P2E-LER-induced V_{TH} variation is smaller than the 1P1E-LER-induced V_{TH} variation, due to the longer correlation length.

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