# A Channel Model of Scaled RC-dominant Wires for High-Speed Wireline Transceiver Design

Minsoo Choi, Jae-Yoon Sim, Hong-June Park, and Byungsub Kim

Abstract—This paper explains modeling and analysis of RC-dominant wires for high-speed wireline transceiver design. A closed form formula derived from telegrapher's equation accurately describes a frequency response of an RC-dominant wire, yet it is simple and intuitive for designers to easily understand design trade-offs without a complex numerical equation solver. This paper explains how the model is derived and how it can help designers in example transceiver designs.

*Index Terms*—Channel model, RC-dominant wires, wireline transceiver design, signaling modes

#### I. INTRODUCTION

Modern computing systems rely on parallelism through high speed interconnects. Since the power consumption of a single-core processor hits the power wall [1], computers utilize many cores to increase the system throughput. However, to efficiently synchronize distributed modules, systems require energy-efficient high-speed interconnection. Therefore, to continuously improve systems under a power constraint, industry must keep improving interconnect performance and energy efficiency to support more cores at the same power cost.

The promising solution most to improve interconnection is to scale wires: 1) to reduce wire length by closely integrating components; 2) to increase the number of wires by reducing wire pitch. We can improve performance and energy-efficiency of data communication by reducing wire length because wireline communication cost exponentially decreases as the distance shrinks. Additionally, increasing number of wires improves energy efficiency because many slow interconnects are more energy efficient than a few fast interconnects for the same aggregated data rate [2-4]. Therefore, as we scale wires, we improve both speed and power-efficiency.

Fig. 1 depicts interconnect scaling trend as integration technology evolves from system on printed-circuit-board (PCB) [5] through system-in-a-package (SiP) to systemon-a-chip (SoC) [6]. Distances between modules and thus the lengths of wires shrink as integration density increases. In general, wire pitches shrink faster than modules allowing more wires between modules. This trend of interconnect scaling is reported in many articles [2-4, 6-12]. Knickerbocker greatly scaled length and density of interconnects by densely populating chip dies on a silicon substrate package called "silicon carrier" instead of on a PCB [6]. This SiP technology leveraged a good thermal expansion match between dies and a package medium, and used back-end-of-line (BEOL) and through-silicon-vias (TSV) to reduce wire pitch and to increase input/output (I/O) density. Kim and Liu discussed high-speed wireline transceiver design for silicon carrier packages [7, 8]. Kang demonstrated a 3-D stacked DRAM chip in a single package using TSV technology [9]. This SiP technology improved latency, speed, and energy-efficiency of data communication

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**Fig. 1.** Trend of interconnect scaling and integration technology: a system on printed-circuit-board (PCB)  $\rightarrow$  a system-in-package (SiP)  $\rightarrow$  a system-on-a-chip (SoC) [18].

utilizing TSV wires which are much shorter than conventional 2-D buses. For micro-processor applications, many-core SoC systems used a network-on-achip (NoC) supported by on-chip wires even shorter and narrower than SiP interconnects [10]. Many articles claimed that the performance and energy efficiency can be greatly improved when these on-chip interconnects are leveraged by advanced circuit techniques [2-4, 11-13].

The characteristics of the scaled interconnects are different from those of conventional transmission line interconnects. Because scaled wires are narrow and tightly packed in general, their resistances and capacitances dominate their inductances. For this reason, typically, scaled wires are RC-dominant while conventional transmission lines are LC-dominant. The large resistances of scaled wires result in large channel losses and frequency-dependent characteristic impedances while the LC-dominant property of LCtransmission lines cause small channel losses and purely resistive characteristic impedances.

Due to the unique RC-dominant characteristics of scaled wires, designers of high speed links need a simple and accurate model of scaled wires different from the widely-known conventional interconnect models. A low-loss transmission line model is most widely-used in the high-speed data link design. However, this model is not suitable for scaled RC-dominant wires since it is derived assuming LC-dominant property [14]. Traditional Elmore delay model can nicely describe the delay of an RC-

dominant wire in a simple formula [15]. However, it cannot describe the wire's broadband response for highspeed transceiver design. By segmenting an RCdominant wire into many RC-ladders [16, 17], an RCladder model gives designers a polynomial formula of the channel's transfer function and impedance [17]. However, the formula becomes too complex for designers to intuitively understand and use it if the number of segments is large enough for reasonable accuracy.

This paper will explain a simple yet decently accurate channel model of RC-dominant wires for high-speed transceiver design [18]. The model is analytically derived by revisiting telegrapher's equation and approximated by assuming small impact of the receiver reflection. The result model is much simpler and more accurate than the RC-ladder model, but it is not widely known by integrated circuit (IC) designers because sophisticated high-speed signaling through an RC-dominant wire was not highly demanded in the IC history. As the demand increases today, this model is expected to be widely useful in the future in IC design.

The rest of this paper is organized as follows. Section II explains a transfer function of an RC-dominant interconnect and how to interpret the transfer function to help designers to easily digest the model. In addition, accuracy of the model is compared against to SPICE simulation. Section III explains how designers can easily understand the impacts of impedances and signaling modes on the channel's trade-offs using the channel model. Two example cases will be explained using the presented model. At the end, Section IV concludes this paper.

# II. A TRANSFER FUNCTION OF A TRANSMISSION LINE

A scaled wire can be modeled as an RC-dominant lossy transmission line [2-4]. Wires for data transfer typically have a uniform 2-D cross-sectional structure, having constant *RLGC* transmission line model parameters: resistance R, inductance L, conductance G, and capacitance C per unit length. Therefore, we can consider a scaled wire as a special case of a general transmission line whose behavior can be described by telegrapher's equations. The solution of these equations with proper boundary conditions gives us the transfer function and the characteristic impedance of the channel. In most practical scaled wires with the reasonably large loss and small impact of the receiver's reflection due to large resistance, we can approximate the solution into a simple and yet accurate form.

The channel model is derived by revisiting telegrapher's equation and approximating the solution. Fig. 2 depicts a schematic diagram of a general transmission line with a transmitter and a receiver. The transmitter is modeled as a data-controlled Théveninequivalent voltage source  $V_{Tx}(\omega)$  with a Thévenin impedance  $Z_{Tx}(\omega)$ , which is typically purely resistive. At the other end of the wire,  $Z_{Rr}(\omega)$  represents the receiver's input impedance which is typically either purely resistive (terminated by a resistor) or capacitive (not terminated and connected to the transistor's gate) depending on the receiver's circuit types. The wire is modeled as a RLGC transmission line whose length is l.  $V(z,\omega)$  and  $I(z,\omega)$ along the wire are the wire's voltage and current wave at distance z from the transmitter. By applying transmission line theory to Fig. 2, telegrapher's Eqs. (1)-(3) can be easily derived [18].

$$-\frac{\partial}{\partial z} \begin{bmatrix} V(z,\omega)\\ I(z,\omega) \end{bmatrix} = \begin{bmatrix} 0 & R+j\omega L\\ G+j\omega C & 0 \end{bmatrix} \begin{bmatrix} V(z,\omega)\\ I(z,\omega) \end{bmatrix},$$
(1)

 $V_{T_{\rm Y}}(\omega) = V(0,\omega) + Z_{T_{\rm Y}}(\omega)I(0,\omega), \tag{2}$ 

$$V(l,\omega) = Z_{Rx}(\omega)I(l,\omega).$$
(3)

Eq. (1) describes the behavior of the traveling voltage and current waves along the wire while (2) and (3) are boundary conditions set by the impedances of the transmitter and the receiver, respectively. By assuming large channel loss, we can approximate the solution of



**Fig. 2.** A schematic diagram of an interconnect to derive telegrapher's equations.

Eqs. (1)-(3) into (4) and (5).

$$\frac{V(l,\omega)}{V_{Tx}(\omega)} \approx \frac{Z_{c}(\omega)}{Z_{c}(\omega) + Z_{Tx}(\omega)} 2e^{-l\sqrt{(R+j\omega L)(G+j\omega C)}} \frac{Z_{Rx}(\omega)}{Z_{c}(\omega) + Z_{Rx}(\omega)},$$

$$(4)$$

$$Z_{c}(\omega) = \sqrt{(R+j\omega L)/(G+j\omega C)}.$$

$$(5)$$

Eq. (4) describes an approximate transfer function of the channel while  $Z_c(\omega)$  in Eq. (5) is the wire's characteristic impedance.

In certain frequency range, if wire's resistance R and capacitance C dominate wire's inductance L and conductance G ( $R >> |j\omega L|$  and  $|j\omega C| >> G$ ), we can approximate Eqs. (4) and (5) into Eqs. (6) and (7), respectively.

$$\frac{V(l,\omega)}{V_{T_{x}}(\omega)} \approx \frac{Z_{c}(\omega)}{Z_{c}(\omega) + Z_{T_{x}}(\omega)} 2e^{-l\sqrt{j\omega RC}} \frac{Z_{R_{x}}(\omega)}{Z_{c}(\omega) + Z_{R_{x}}(\omega)},$$

$$\frac{C(\omega)}{Z_{c}(\omega)} = \sqrt{R/j\omega C}.$$
(6)
(7)

By using Eqs. (6) and (7) in the frequency range satisfying wire's RC-dominant condition, designers can easily and intuitively analyze RC-dominant channels.

With simplicity of the channel transfer function in Eq. (6), designers can easily interpret a complex channel problem into three isolated parts: the transmitter, the wire, and the receiver. The first term  $Z_c(\omega)/(Z_c(\omega)+Z_{Tx}(\omega))$ represents how the impedances of the transmitter and the wire impact the overall channel transfer function. The second term  $2e^{-l\sqrt{j\omega RC}}$  describes the impact of the channel attenuation along the wire. The third term  $Z_{Rx}(\omega)/(Z_c(\omega)+Z_{Rx}(\omega))$  describes how the impedances of the receiver and the wire impact the overall channel's transfer function. Note that the transmitter's impedance  $Z_{Tx}(\omega)$  only appears in the first term while the receiver's impedance  $Z_{Rx}(\omega)$  only appears in the third term. Therefore, Eq. (6) allows designers to divide a channel design problem into isolated transmitter, receiver, and wire design problems. For example, a designer can optimize  $Z_{Tx}(\omega)$  with respect to the overall transfer function only considering the first term  $Z_c(\omega)/$  $(Z_c(\omega)+Z_{Tx}(\omega))$ . Similarly, a designer can optimize  $Z_{Rx}(\omega)$ using  $Z_{Rx}(\omega)/(Z_c(\omega)+Z_{Rx}(\omega))$  term. In the later section, we will explain how Eq. (6) and the three terms can help

designers to isolate and simplify design problems using detail examples.

The channel models in Eqs. (4) and (6) can accurately calculate the transfer functions of RC-dominant channels. To verify the accuracy of the channel model transfer functions of an interconnect computed from (4) and (6) are compared to the SPICE simulation. The interconnect parameters used in this example are *l*=10 mm, *R*=53.419 m $\Omega/\mu$ m, *L*=0.236 pH/ $\mu$ m, *C*=0.198 fF/ $\mu$ m, and *G*=0 mS/ $\mu$ m.

Fig. 3(a) shows the transfer function computed from Eq. (4) (RLC model) and the corresponding SPICE simulation using w-element model. Both match well in wide frequency range. At low frequency about 50 MHz, the relative error between Eq. (4) and SPICE simulation is large (about 15 %) because the large channel loss assumption is not valid. However, the relative error decreases as the frequency increases because the channel loss increases. The relative error drops below 10 % for frequency over 100 MHz, showing that Eq. (4) can accurately calculate the transfer function for this frequency region.

Fig. 3(a) shows that Eq. (6) (RC model) can describe the transfer function within an RC-dominant and highly lossy frequency region. The relative error between Eq. (6) and SPICE simulation is below 10 % between 100 MHz and 3 GHz where the assumptions of large channel loss and the RC-dominance ( $R >> |j\omega L|$ ,  $|j\omega C| >> G$ ) are valid, giving the rule of thumb for the RC-dominant approximation: if the impedance of the wire's inductance L is below 10 % of the wire's resistance R, then the relative errors between RLC and RC models are below about 10 %.

The channel model can also accurately calculate the characteristic impedance for RC-dominant channels. Fig. 3(b) shows the characteristic impedance  $Z_c(\omega)$  computed from Eq. (5) and SPICE simulation. Eq. (5) matches well with SPICE simulation in wide frequency range. The magnitude of  $Z_c(\omega)$  is approximately inversely proportional to the square-root of the frequency as shown in Eq. (8) while the phase is roughly proportional to the frequency because the small inductance *L* term linearly increases the phase as the frequency increases as Eq. (9) states. However, the frequency dependent term is small and thus the phase is about constant -45 degree in RC-dominant wires (about -8 degree in Fig. 3(b)). Therefore,



**Fig. 3.** An example transfer function computed from equation (4) and (6) against SPICE simulation and relative errors between them (a), and the characteristic impedance  $Z_c(\omega)$  (b).

 $Z_c(\omega)$  has a low pass filter (LPF) behavior while  $Y_c(\omega)$  is the opposite. Eqs. (8) and (9), which is derived from Eq. (5) with assumption of RC-dominant property  $(R > |j\omega L|$ and  $|j\omega C| >> G$ ), explain these magnitude and phase behavior well.

$$\begin{aligned} \left| Z_{c} \left( \omega \right) \right| &\approx \left| \sqrt{\frac{R + j\omega L}{j\omega C}} \right| = \sqrt[4]{\left( \frac{L}{C} \right)^{2}} + \left( \frac{R}{\omega C} \right)^{2} \approx \sqrt{\frac{R}{\omega C}}, \end{aligned}$$

$$\begin{aligned} & \swarrow Z_{c} \left( \omega \right) &\approx \angle \sqrt{\frac{R + j\omega L}{j\omega C}} = -\frac{\pi}{4} + \frac{1}{2} \tan^{-1} \left( \frac{\omega L}{R} \right) \end{aligned}$$

$$\begin{aligned} &\approx -\frac{\pi}{4} + \frac{\omega L}{2R} \approx -\frac{\pi}{4}. \end{aligned}$$

$$\end{aligned}$$

$$\end{aligned}$$

$$\end{aligned}$$

$$\end{aligned}$$

$$\end{aligned}$$

## III. TERMINATION IMPEDANCE AND SIGNALING MODES

The channel model can easily explain the trade-offs by signaling and termination strategies in RC-dominant interconnect design. These trade-offs are different from the ones of conventional transmission lines due to the frequency dependent characteristic impedance of RC-dominant wires.

Fig. 4 shows circuit diagrams of interconnects (length l) in voltage mode and current mode. The wire's inductance and conductance are ignored due to dominance of the wire's resistance and capacitance.  $R_{Tx}$  and  $R_{Rx}$  are the transmitter's output resistance and the receiver's input resistance, respectively.  $R_{Tx}$  is typically small for voltage mode and large for current mode while  $R_{Rx}$  is the opposite. From Fig. 4, designers can easily derive four transfer functions of interconnects with a transmitter in voltage mode or current mode and a receiver in voltage mode or current mode:

$$\begin{split} T_{vv}(\omega) &\approx \frac{V_{Rx}(\omega)}{V_{Tx}(\omega)} = \frac{Z_c(\omega)}{R_{Tx} + Z_c(\omega)} 2e^{-l\sqrt{j\omega RC}} \frac{R_{Rx}}{R_{Rx} + Z_c(\omega)}; \\ (10) \\ T_{vi}(\omega) &= \frac{I_{Rx}(\omega)}{V_{Tx}(\omega)} = \frac{Z_c(\omega)}{R_{Tx} + Z_c(\omega)} 2e^{-l\sqrt{j\omega RC}} \frac{1}{R_{Rx} + Z_c(\omega)}; \\ T_{iv}(\omega) &= \frac{V_{Rx}(\omega)}{I_{Tx}(\omega)} = \frac{R_{Tx}Z_c(\omega)}{R_{Tx} + Z_c(\omega)} 2e^{-l\sqrt{j\omega RC}} \frac{R_{Rx}}{R_{Rx} + Z_c(\omega)}; \\ (11) \\ T_{ii}(\omega) &= \frac{I_{Rx}(\omega)}{I_{Tx}(\omega)} = \frac{R_{Tx}Z_c(\omega)}{R_{Tx} + Z_c(\omega)} 2e^{-l\sqrt{j\omega RC}} \frac{1}{R_{Rx} + Z_c(\omega)}; \\ (12) \\ T_{ii}(\omega) &= \frac{I_{Rx}(\omega)}{I_{Tx}(\omega)} = \frac{R_{Tx}Z_c(\omega)}{R_{Tx} + Z_c(\omega)} 2e^{-l\sqrt{j\omega RC}} \frac{1}{R_{Rx} + Z_c(\omega)}. \\ (13) \end{split}$$

The accuracy of Eqs. (10)-(13) is shown in Fig. 5 by



**Fig. 4.** An interconnect with transmitters and receivers in various signaling modes: a voltage mode transmitter (a), a current mode transmitter (b), a voltage mode receiver (c), and a current mode receiver (d).



Fig. 5. Comparison between Eqs. (10)-(13) and SPICE simulations.

comparing transfer functions against SPICE simulations. The common term  $e^{-l\sqrt{j\omega RC}}$  in (10)-(13) describes the intrinsic exponential attenuation by the wire. The terms  $Z_{c}(\omega)/(R_{Tx}+Z_{c}(\omega)), R_{Tx}Z_{c}(\omega)/(R_{Tx}+Z_{c}(\omega)), R_{Rx}/(R_{Rx}+Z_{c}(\omega)),$ and  $1/(R_{Rx}+Z_c(\omega))$  describe interactions between the wire and the termination impedances of the voltage mode transmitter, current mode transmitter, voltage mode receiver, and current mode receiver, respectively. Because of these terms, termination and signaling strategies in RC-dominant interconnects result in quite different trade-offs than in conventional LC-dominant transmission lines. For example,  $Z_c(\omega)$  is constant 50 Ohm in conventional LC-dominant transmission lines, making these terms independent of frequency. Therefore, the bandwidth is constant in resistively terminated LCdominant transmission lines regardless of the termination resistances and signaling modes. However, in RCdominant interconnects, the termination resistance and signaling mode strongly affect the bandwidth because the four terms, which are derived from four different signaling modes and terminations, differently depend on the frequency and the termination resistance due to the frequency dependent  $Z_c(\omega)$  term. Therefore, Eqs. (10)-(13) are important guidelines for signaling and termination strategies in RC-dominant interconnect design. We will explain how designers can use Eqs. (10)-(13) to understand two example signaling and termination strategies [7, 8, 11, 12].

We can explain the transmitter termination strategy used in [7] by using Eqs. (10)-(13). To reduce hardware area and power consumption of a many-tap decision feedback equalization (DFE) receiver, Kim [7] reported a modified DFE receiver with an infinite impulse response filter (DFE-IIR). In [7], the transmitter can be modeled as a voltage mode transmitter in Fig. 4 (a), and  $R_{Tx}$  value is chosen small. The rationale of this design choice can be easily understood by (10)-(13). From (10)-(13), voltage transmit transfer functions  $(T_{vv}(\omega))$  and  $T_{vi}(\omega)$  and current transmit transfer functions  $(T_{iv}(\omega) \text{ and } T_{ii}(\omega))$  are proportional to  $Z_c(\omega)/(R_{Tx}+Z_c(\omega))$  and  $R_{Tx}Z_c(\omega)/(R_{Tx}+Z_c(\omega))$ , respectively. These two terms are identical except for the multiplicative factor  $R_{Tx}$  since the voltage mode transmitter and the current mode transmitter can be transformed to each other by Norton and Thévenin equivalence for the same Thévenin resistance  $R_{Tx}$ . However,  $R_{Tx}$  value is typically small in voltage mode

and large in current mode for large signal amplitude, resulting in difference between voltage mode and current mode. Fig. 6 shows the impacts of  $R_{Tx}$  on the two terms  $Z_c(\omega)/(R_{Tx}+Z_c(\omega))$  and  $R_{Tx}Z_c(\omega)/(R_{Tx}+Z_c(\omega))$  from the transfer functions (10)-(13) with voltage mode and current mode signal transmission.  $|Z_c(\omega)/(R_{Tx}+Z_c(\omega))|$ increases as  $R_{Tx}$  decreases in Fig. 6(a) while  $|R_{Tx}Z_c(\omega)|$  $(R_{Tx}+Z_c(\omega))$  changes in the opposite direction in Fig. 6(b). To obtain large signal amplitude, small  $R_{Tx}$  is preferred in voltage mode and large  $R_{Tx}$  is preferred in current mode. Different  $R_{Tx}$  values result in difference between bandwidths in voltage mode and current mode signal transmission. For example, in ideal cases,  $Z_c(\omega)/(R_{Tx}+Z_c(\omega))$  converges to 1 as shown in Fig. 6(a) and  $R_{Tx}Z_c(\omega)/(R_{Tx}+Z_c(\omega))$  converges to  $Z_c(\omega)$  as shown in Fig. 6(b) as  $R_{Tx}$  converges to the ideal impedances:  $R_{Tx}$ = 0 in voltage mode and  $R_{Tx} = \infty$  in current mode. Therefore,  $T_{vv}(\omega), T_{vi}(\omega) \propto Z_c(\omega)/(R_{Tx}+Z_c(\omega))$  converges to 1 and  $T_{i\nu}(\omega), T_{ii}(\omega) \propto R_{Tx} Z_c(\omega) / (R_{Tx} + Z_c(\omega))$  converges to  $Z_c(\omega)$ 



**Fig. 6.** The terms describing the impacts of the transmitter impedance  $R_{Tx}$  on the transfer functions:  $Z_c(\omega)/(R_{Tx}+Z_c(\omega))$  for a voltage mode transmitter (a),  $R_{Tx}Z_c(\omega)/(R_{Tx}+Z_c(\omega))$  for a current mode transmitter (b).

when ideally terminated. As discussed earlier,  $Z_c(\omega)$  is a low pass filter, and thus the current mode transmitter has poorer bandwidth than the that of voltage mode. This influence of the transmitter type on the bandwidth can be analyzed by Eqs. (10)-(13) without SPICE simulations. To compare the bandwidth, Fig. 7 shows the normalized transfer functions of  $T_{vv}(\omega)$  and  $T_{iv}(\omega)$  when ideal voltage mode and current mode transmitters are used. As Fig. 7 shows, the transfer functions computed from equations and SPICE simulations match well, and both results indicate that the channel with the voltage mode transmitter has wider bandwidth than that of the current mode transmitter. Therefore, a voltage mode transmitter with small  $R_{Tx}$  is preferred for high bandwidth in [7].

Receiver's termination and signaling mode also strongly affect the design trade-offs of RC-dominant interconnects [11, 12]. Channel models in (10)-(13) easily explain the trade-offs and how a simple transimpedance amplifier (TIA) circuit can greatly improve performance and power efficiency of a receiver for an RC-dominant wire [11, 12]. From (10)-(13), the transfer functions with a voltage mode receiver  $(T_{vv}(\omega), T_{iv}(\omega))$ are proportional to  $R_{Rx}/(R_{Rx}+Z_c(\omega))$  while the ones with a current mode receiver  $(T_{vi}(\omega), T_{ii}(\omega))$  are proportional to  $1/(R_{Rx}+Z_c(\omega))$ . For the same receiver impedance  $R_{Rx}$ value, both terms are identical except for the multiplicative factor  $R_{Rx}$  because  $V_{Rx}(\omega) = R_{Rx}I_{Rx}(\omega)$  in Fig. 4. Therefore, the receivers in voltage mode and current mode have the same bandwidth if they have the same receiver's impedance  $R_{Rx}$ . The difference is the



**Fig. 7.** Normalized transfer functions with ideally-terminated voltage mode and current mode transmitters are used:  $R_{Tx} = 0$  in a voltage mode transmitter and  $R_{Tx}=\infty$  in a current mode transmitter. The transfer functions are obtained from Eqs. (10), (12) and SPICE simulations.

amplitude of their transfer functions due to the different multiplicative factor  $R_{Rx}$ . However, as Fig. 8 shows, the magnitudes and bandwidths are differently coupled by  $R_{Rx}$  in voltage mode and current mode receivers, resulting in different trade-offs between them. By using Eqs. (10)-(13), designers can easily understand how a TIA receiver performs much better than voltage mode and current mode receivers by modifying the trade-offs by  $R_{Rx}$  [11, 12].

Fig. 9 depicts receivers with a resistor termination (a) and a TIA termination (b), and Fig. 10 shows their various metrics versus  $R_{Rx}$  in Fig. 9. To verify the accuracy of the equations, the metrics are also theoretically calculated using Eqs. (10)-(13) and compared against to SPICE simulations. Static current  $I_{static}$  is computed for a resistor-terminated receiver assuming that the transmitter's common mode voltage is half the supply voltage. Example design points of the TIA receiver are marked as " $\Box$ " in Fig. 10 while the



**Fig. 8.** The terms describing the impacts of the receiver impedance  $R_{Rx}$  on the transfer functions:  $R_{Rx}/(R_{Rx}+Z_c(\omega))$  for voltage mode receiver (a),  $1/(R_{Rx}+Z_c(\omega))$  for current mode receiver (b).



**Fig. 9.** A receiver with resistive termination (a) and transimpedance amplifier termination (b) [11].



Fig. 10. Various metrics of an interconnect versus receiver's termination impedance: data points of the resistively-terminated receiver in Fig. 9(a) are marked as "x"; data points of a transimpedance-amplifier-terminated receiver in Fig. 9(b) are marked as " $\Box$ ".

counterparts of the resistor-terminated receiver for the same bandwidth are marked as "x".

In a resistively terminated voltage mode receiver, the received signal voltage amplitude V at the Nyquist frequency (2 GHz) in Fig. 9(a) increases as  $R_{Rx}$  increases as shown in Fig. 10. However, V saturates because  $T_{vv}(\omega)$ ,  $T_{iv}(\omega) \propto R_{Rx}/(R_{Rx}+Z_c(\omega))$  converges to 1 as  $R_{Rx}$  becomes dominant as Fig. 8(a) shows. At the same time  $I_{static}$  decreases as the DC resistance to supply voltage, i.e.  $R_{Rx}$ , increases because  $T_{vv}(\omega)$ ,  $T_{iv}(\omega) \propto R_{Rx}/(R_{Rx}+Z_c(\omega)) \approx 1$  for large  $R_{Rx}$  while  $R_{Rx}/(R_{Rx}+Z_c(\omega)) \approx R_{Rx}/(R_{Rx}+Z_c(\omega)) \approx 1$  for small  $R_{Rx}$  as seen in Fig. 8(a) and  $Y_c(\omega)$  behaves as a high pass filter boosting the high frequency portion of the spectrum as discussed earlier.

In a resistively terminated current mode receiver, the signal amplitude and bandwidth are differently coupled by  $R_{Rx}$  causing a different trade-off than in a resistively terminated voltage mode receiver. By terminating the receiver with a small resistor, the received signal current amplitude *I* at 2 GHz (AC) increases as shown in Fig. 10

because the common denominator of  $T_{vi}(\omega)$  and  $T_{ii}(\omega)$ , i.e.  $(Z_c(\omega)+R_{Rx})$ , decreases as  $R_{Rx}$  decreases. Bandwidth also increases as  $R_{Rx}$  converges to 0 because  $T_{vi}(\omega)$ ,  $T_{ii}(\omega)$  $\propto 1/(Z_c(\omega)+R_{Rx})$  converges to  $1/Z_c(\omega)$  in Fig. 8(b) which is a high pass filter as discussed earlier. The cost of this improvement is a large DC static current due to the small resistance to supply, i.e. small  $R_{Rx}$ . Therefore, a designer can buy bandwidth and amplitude for static power in a current mode receiver [11].

A TIA at receiver front-end breaks the fundamental trade-offs in voltage mode and current mode signaling by separating the relation between the small signal input impedance and the static current to supply [11, 12]. A TIA in Fig. 9(b) provides a small-signal input resistance (~780 Ohm) to the channel but the static current is only about 80 µA due to the large gain resistor (~4.1 KOhm) of the TIA. The bandwidths of the TIA terminated receiver is roughly 530 MHz slightly smaller than theoretical value (545 MHz) of the resistively terminated receiver due to parasitic capacitance of the TIA. For the almost same bandwidth, the pure 780 Ohm resistorterminated receiver burns the static current five times as large as the TIA-terminated receiver does. After currentto-voltage conversion by the TIA, the converted voltage amplitude  $V_{tia}$  is about four times as large as the voltage received by the pure resistor termination. With the larger amplitude, the transmitter's driving amplitude can be smaller for the same eye opening at the receiver, saving transmitter energy. This benefit scales larger as the receiver's input impedance decreases and gain resistance increases. However, designers must consider other design concerns of TIA too. For example, a large gain resistance of TIA may cause a voltage headroom problem in low supply voltage process. Also, TIA's output voltage level must be suited to the common mode voltage level of the following circuit. In [11, 12] example, the TIA design was well suited to 90 nm technology with 1V supply voltage level and common mode voltage of ~0.78V of the following sampler circuit.

### **V. CONCLUSIONS**

In this paper, a simple yet decently accurate channel model for an RC-dominant wire is explained, and examples of its usage are presented. The model provides guidelines and intuitions to aid the design of high-speed transceiver circuits for the next generations of scaled RCdominant interconnects. As shown in the examples, the design trade-offs by termination strategies and voltage/current mode selections are important and can be easily understood with the model. The usefulness of this model is expected to grow in the future as the demand for sophisticated high-speed signaling over RC-dominant wires continually increases.

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#### REFERENCES

- T. Kuroda, "CMOS design challenges to power wall," *IEEE Int. Microprocesses and Nanotech*nology Conf., 2001, pp. 6-7.
- [2] B. Kim, "Equalized On-Chip Interconnect: Modeling Analysis and Design," Ph.D. dissertation, Dept. EECS, MIT, Cambridge, MA, 2010.
- [3] B. Kim and V. Stojanović, "Characterization of Equalized and Repeated Interconnects for NoC Applications," *IEEE J. Design and Test of Computers*, vol. 25, no. 5, pp. 430-439, Oct. 2008.
- [4] B. Kim and V. Stojanović, "Equalized Interconnect for On-Chip Network: Modeling and Optimization Framework," *IEEE/ACM Int. Computer- Aided Design Conf.*, Nov. 2007, pp.552-559.
- [5] S. Kwak, Y. Jo, J. Jo, and S. Kim, "Power Integrity and Shielding Effectiveness Modeling of Grid Structured Interconnects on PCBs," *Journal of Semiconductor Technology and Science*, vol. 12, no. 3, pp. 320-330, Sep. 2013.
- [6] J. U. Knickerbocker et al., "Development of nextgeneration system-on-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection," *IBM J. Research and Development*, vol. 49, no. 4/5 July/September 2005.
- [7] B. Kim et al., "A 10-Gb/s Compact Low-Power Serial I/O with DFE-IIR Equalization in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no.

12, pp. 3526-3538, Dec. 2011.

- [8] Y. Liu et al., "A 10Gb/s Compact Low-Power Serial I/O with DFE-IIR Equalization in 65nm CMOS," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 182-183.
- [9] U. Kang et al., "8 Gb 3-D DDR3 DRAM Using Through-Silicon-Via Technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 111-119, Jan. 2010.
- [10] S. Vangal et al., "An 80-Tile 1.28TFLOPS Network-on-Chip in 65nm CMOS," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2007, pp. 98-99, 589.
- [11] B. Kim and V. Stojanović, "An Energy-Efficient Equalized Transceiver for RC-Dominant Channels," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1186-1197, June 2010.
- [12] B. Kim and V. Stojanović, "A 4Gb/s/ch 356fJ/b 10mm Equalized On-chip Interconnect with Nonlinear Charge-Injecting Transmit Filter and Trans- impedance Receiver in 90nm CMOS," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, vol. 978, pp. 66-67, 978.
- [13] A. Joshi, B. Kim, and V. Stojanović, "Designing Energy-Efficient Low-Diameter On-chip Networks with Equalized Interconnects," *IEEE Symp. High-Performance Interconnects*, Aug. 2009, pp. 3-12.
- [14] M. N. O. Sadiku and L. C. Agba, "A simple introduction to the transmission-line modeling," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 37, no. 8, pp. 991-999, Aug. 1990.
- [15] W. C. Elmore, "The Transient Response of Damped Linear Networks with Particular Regard to Wideband Amplifiers", J. Applied Physics, pp. 55-63, Jan. 1948.
- [16] T. Kim, Y. Song, and Y. Eo, "Timing Analysis of Discontinuous RC Interconnect Lines," *Journal of Semiconductor Technology and Science*, vol. 9, no. 1, pp. 8-13, Mar. 2009.
- [17] E. N. Protonotarios, "Optimal transfer-function synthesis of RC ladders-lumped and distributed," *IEEE Trans. Circuits Systems*, vol. CAS-21, pp. 49-56, Jan. 1974.
- [18] B. Kim, "An Analytical Model of Scaled RCdominant Wires for High-Speed Wireline Transceiver Design," *IEEE Int. Midwest Symp. Circuits and Systems*, Aug. 2011, pp. 1-4.



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