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홀드 업 타임 보상회로를 가진 IT 기기용 Front-end PSFB DC/DC 컨버터

이강현†

Phase-Shifted Full Bridge(PSFB) DC/DC Converter with a Hold-up Time Compensation Circuit for Information Technology (IT) Devices

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Abstract - A hold-up time compensation circuit is proposed to get high efficiency of the front-end phase-shifted full bridge DC/DC converter. The proposed circuit can make the phase-shifted full bridge front-end DC/DC converter built with 0.5 duty ratio so that the conduction loss of the primary side and voltage stress across rectifier in the secondary side are reduced and the higher efficiency can be obtained. Furthermore, the requirement of an output filter significantly can diminish due to the perfect filtered waveform. A 12V/100A prototype has been made and experimental results are given to verify the theoretic analysis and detailed features.

Keywords: hold up time, efficiency, PSFB(phase-shifted full bridge) converter, front-end DC/DC converter

1. Introduction

Energy conversion efficiency is very important concern in a power supply for the information technology (IT) equipment such as personal computers, server computers or telecommunication equipments. As shown in Fig. 1, some consortiums have recommended higher efficiency every year. Therefore, the efficiency of the power system is the most critical part in IT devices.

The power system for the IT apparatus is generally distributed power system (DPS), which is composed of a power factor correction (PFC) AC/DC stage, a front-end DC/DC converter and point of load (POL) converters as shown in Fig. 2[1]. The front-end converter is important part to transfer huge energy from a link capacitor in the PFC stage to the system so that it is crucial part to get high energy conversion efficiency. The front-end converter has employed the pulse width modulation (PWM) converters such as an asymmetrical half bridge converter, an active clamped forward converter, and a phase-shifted full bridge (PSFB) converter to get reduced switching loss[2-6].

However, a hold up time satisfaction is special requirement, which the power supply is remaining the output voltage during 20ms after ac line is lost in the IT devices. As the link voltage of the PFC stage is decreased after ac line is lost, the front-end DC/DC converter has to be designed to coverage wide input range as shown in Fig. 3. So, when the ac line is live, the operation condition is poor with a small duty ratio, a small turn ratio of a transformer, high current stress in the primary side and high voltage stress of rectifiers in the secondary side. It can be an obstacle to get high energy conversion efficiency in the PWM front-end DC/DC converter.

In this paper, a strategy for the high efficiency of the front-end DC/DC converter will be discussed. The almost power loss in the DC/DC converter is the conduction loss and the switching loss. If the maximum duty cycle, 0.5, can be used, the conduction loss in the primary side of the isolation transformer

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Fig. 1 Required efficiency by Climate Savers Computing Initiative (CSCI)

Load(%)	20%	50%	100%
80 PLUS	80%	80%	80%
80 PLUS BRONZE	82%	85%	82%
80 PLUS SILVER	85%	88%	85%
80 PLUS GOLD	87%	90%	87%

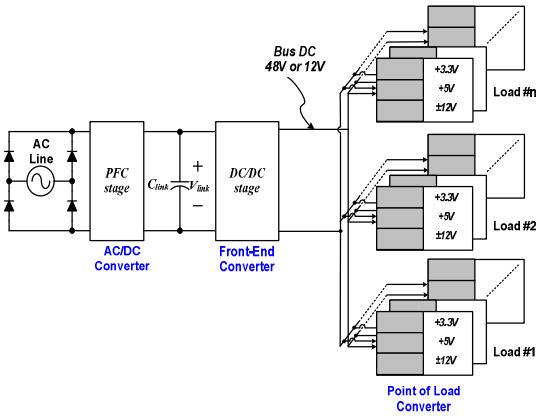


Fig. 2 Structure of the DPS

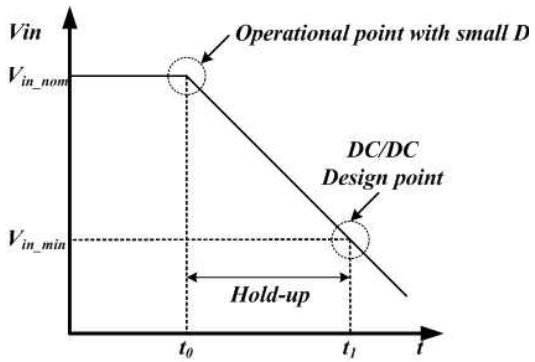


Fig. 3 Front-end DC/DC input voltage variation

will be minimized. If an additional circuit is operated only when the ac line is lost, the higher efficiency can be obtained when the ac line is live and the hold up time specification can be satisfied. In the prior approach, the secondary turn ratio of the isolation transformer is changed by additional switching devices in secondary side[7-8]. Another approach is applying auxiliary boost converter for extending hold up time[9]. The prior approaches use the high cost devices and apply additional power supply for the hold up time extension so the cost and the volume of the power supply are increased. Therefore, a hold up time compensation circuit is proposed to improve the power conversion efficiency in the normal operation state with simpler structure than that of prior approach in this paper. The proposed circuit can help the PWM converter to get high efficiency without considering the input range. When the ac line is lost, the hold up time extension circuit can shortly compensate the hold up time specification. In addition, this hold up time extension circuit can be adapted to other front-end DC/DC converter. To verify the advantages, the theoretical analysis and the experimental results with applying the proposed circuit in the PSFB converter will be shown with a 12V-100A prototype.

2. The proposed converter

Fig.4 shows circuit diagram and key waveform of the PSFB converter with the proposed hold up time compensation circuit. The hold up time extension circuit has two auxiliary switches and one transformer in the primary side of the isolation transformer. In the normal operation, ac line on, the hold up time

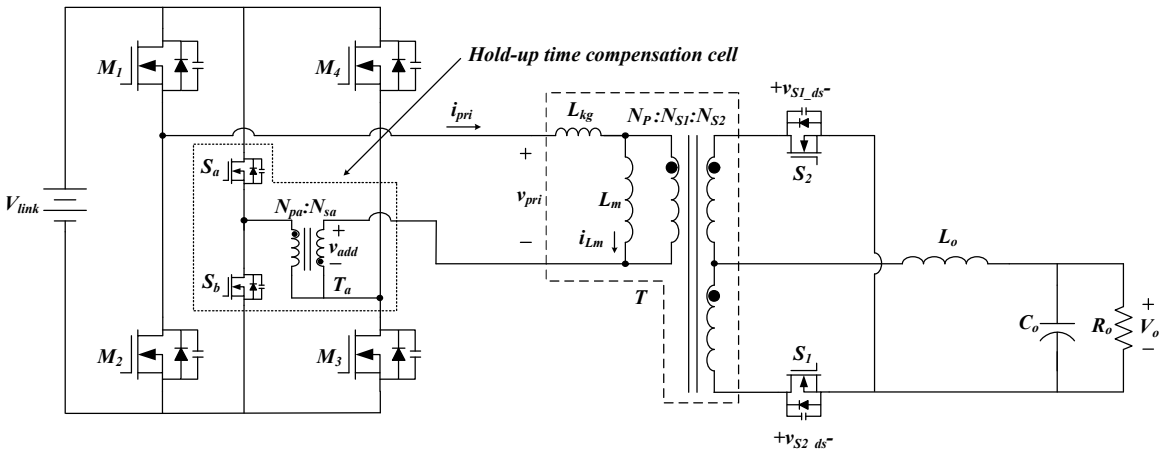
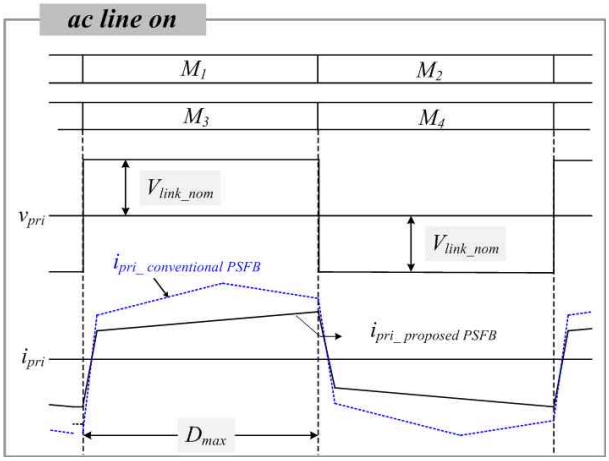


Fig. 4 Proposed PSFB with the hold up time extension circuit

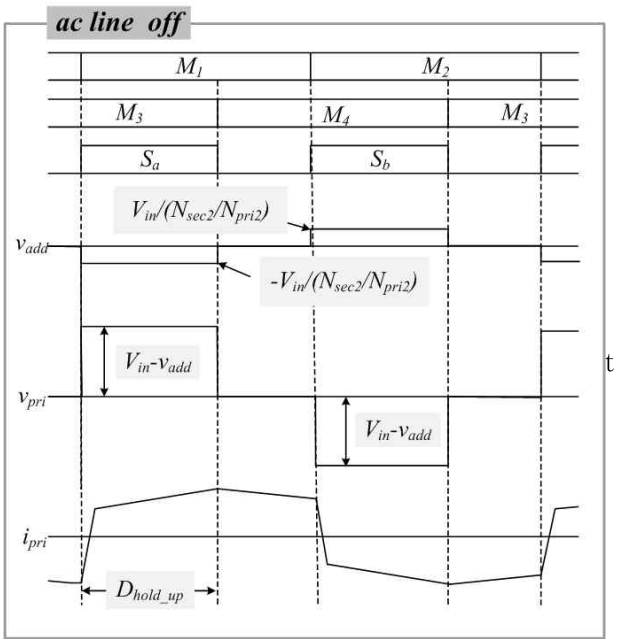
extension circuit is not operated so the operation of the proposed converter is same with the conventional PSFB converter which has the maximum duty ratio. The operation of the proposed converter will be considered in the ac line on and the ac line off each other.

2.1 AC line on

As mentioned above, the proposed PSFB converter is same with the conventional full bridge converter with 0.5 duty ratio in the ac line on. As shown in Fig.5 (a), the primary current is same with that of the conventional 0.5 duty ratio full bridge converter. Therefore, the peak value of the primary current



(a) AC line on



(b) AC line off

Fig. 5 Operational waveform of the proposed circuit

is smaller than that of the conventional PSFB converter without the hold up time extension circuit as shown in Fig. 5 (a). The hold up time extension circuit is not operated, which the S_a and S_b are turned off and the v_{add} of the auxiliary transformer is 0V. In the normal operation, there are small free wheeling current in the hold up time extension circuit.

2.2 AC line off

When the ac line is lost, the output voltage is sustained with the hold up time extension circuit. In this case, the proposed circuit is same with the conventional PSFB converter. The regulation of the output voltage is made by the difference of phase of the M_1~M_4. When the auxiliary switch, S_a, is turned on, the additional input voltage is enforced to the main transformer as shown Fig. 5 (b). Since the ac line is lost, the input voltage of the proposed

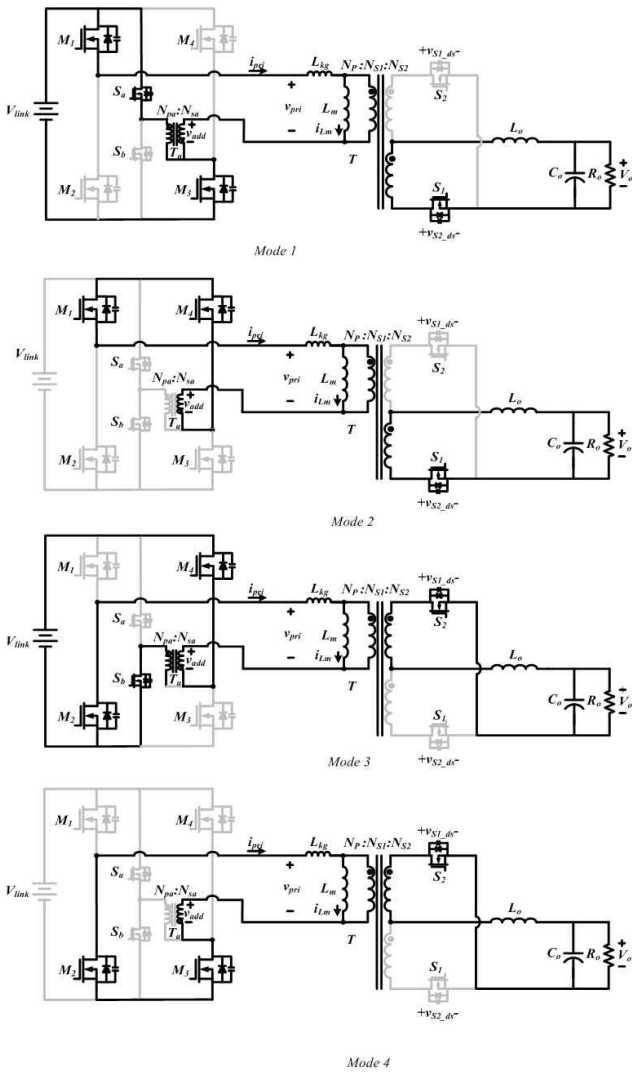


Fig. 6 Simplified conduction path of the proposed circuit in each mode

converter is decreased but the primary voltage of the main transformer is not decreased by the hold up time extension circuit. The turn ratio of the auxiliary transformer can be the design parameter to satisfy the hold up time specification and to get high efficiency. The turn on signal of the supplementary switches can be made by the logical AND gate with signal of the main switches.

3. Features of the Proposed Circuit

3.1 Reducing the link capacitance

The link capacitor is the energy storage element to transfer the PFC output to the front-end DC/DC converter. The PFC link capacitance can be reduced by using the hold up time extension circuit. Fig. 7 shows the minimum voltage of the link capacitor after it takes 20ms to lose the ac line according to the link capacitance. As the link capacitance is smaller, the conventional PSFB converter has to cover the wider voltage range. While we can use the larger link capacitors to shorten the input range of the front-end converter, it results in increasing the size and the cost. We can obtain the high efficiency and the hold up time satisfaction with the hold up time extension circuit and the front-end DC/DC converter has to cover the wide input range with the small link capacitor. It results from designing the turn ratio of the auxiliary transformer in the hold up time extension circuit. Fig. 8 shows the turn ratio of the supplementary transformer according to the link capacitance. So, the proposed converter can have th small link capacitance in the DPS so the low cost and the high power density can be obtained.

3.2 Reducing the current stress in the primary side and the voltage stresses on rectifiers

The proposed converter uses the maximum duty ratio with the smallest turn ratio of the main transformer so a peak and root mean square (RMS) values of the reflected output current in the primary side can be reduced. The peak value of the primary current can be obtained in the PSFB converter as follows

$$I_{pri_{pk}} = \left(I_o + \frac{V_{out}}{L_o}(0.5 - D_{nom})\frac{T_S}{4} \right) \times \frac{1}{n} \quad (1)$$

where D_{nom} is the duty ratio in the ac line on, V_{out} is output voltage, I_o is output current, T_s is switching period and $n=N_p/N_{s1}$ is the turn ratio of the main transformer. Fig. 9 shows the peak value of the primary current in the conventional PSFB converter and the proposed converter. Since the duty ratio of the conventional converter is small according to the minimum link voltage, the peak value of the primary current is larger. However, the hold up time extension circuit can cover the minimum link voltage, thus the peak primary current value can be reduced during the AC line on. It results in reducing the conduction loss in the primary side and core loss of the main transformer. Since the turn ratio of the transformer becomes small, the voltage stress of the rectifiers can be reduced the cost can be less.

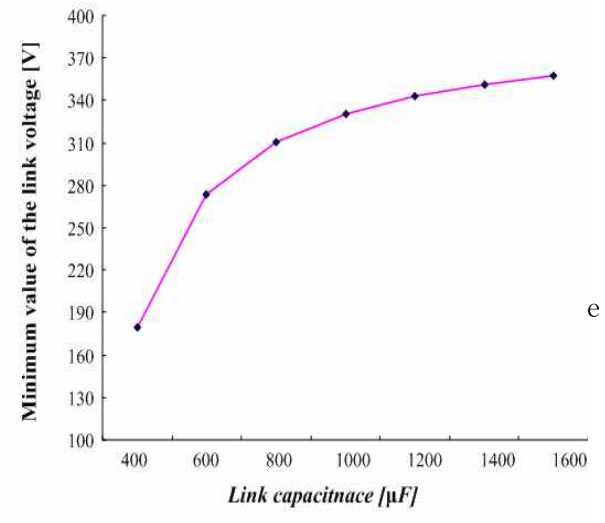


Fig. 7 The minimum voltage after 20ms according to the link capacitance

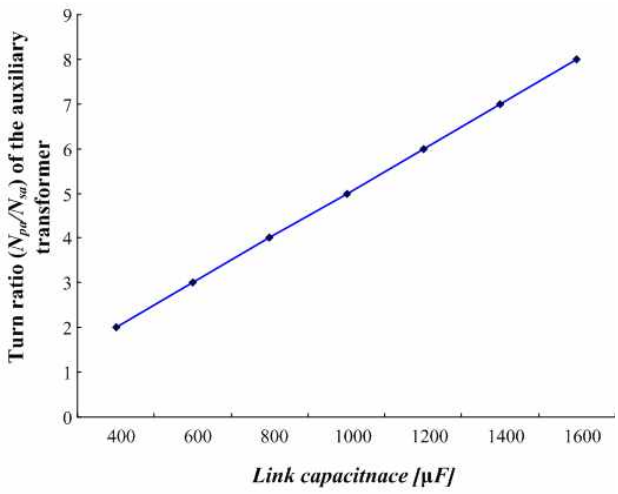


Fig. 8 The minimum voltage after 20ms according to the link capacitance

3.3. Reducing the requirement of an output filter

The output inductance design is an issue for satisfying the output voltage ripple. If the small output inductance is designed, the volume, the cost and the power consumption can be reduced. For example, the output inductance is designed in the PSFB converters as follows

$$I_{Lo\_ripple} = \frac{V_o(0.5 - D_{eff})T_S}{L_o} \quad (2)$$

where I_{Lo_ripple} is an output ripple current, V_o is an output voltage, D_{eff} is a effective duty ratio, L_o is an output inductance and T_s is a switching period. By the proposed hold up time circuit, D_{eff} can be large so the filter inductance can be reduced with the same output voltage ripple. It results in the less volume and the higher efficiency in the front-end DC/DC converter.

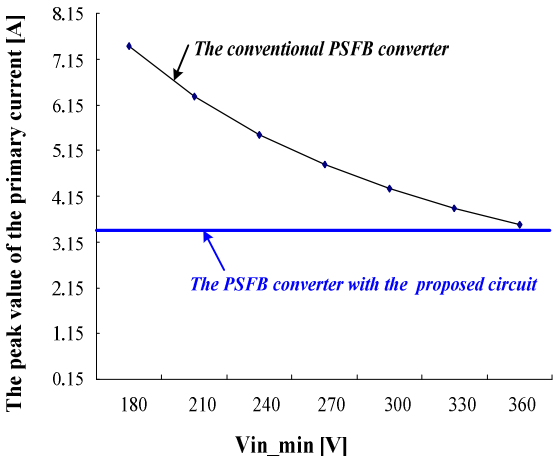


Fig. 9 Designed the turn ratio of the auxiliary transformer to satisfy the hold up time

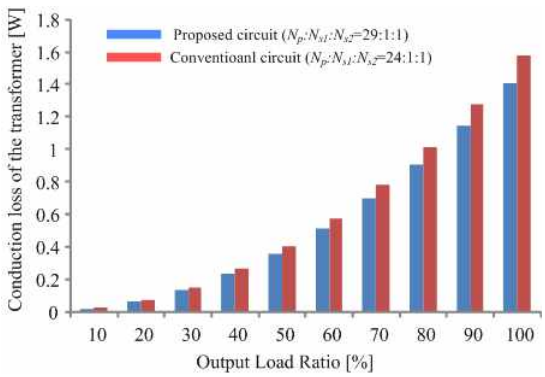
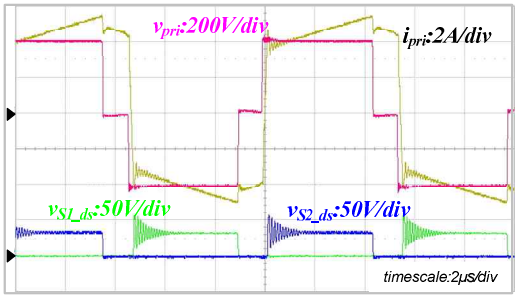


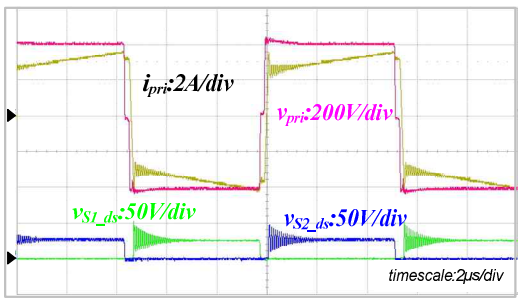
Fig. 10 Conduction loss comparison in the transformer with 12V/100A output

Table 1 Specific Components of a Prototype

Parameters	Symbol	Value/Part
Input voltage range	V_{in}	320V~400V
Output voltage	V_O	12V
Max. power rating	P_{max}	1200W
Turn ratio (T)	N_p:N_{s1}:N_{s2}	29:1:1
Turn ratio (T_a)	N_{pa}:N_{sa}	4:1
Main Switches	M_1~M_4	SPP20N60C
Auxiliary Switches	S_a, S_b	SPP20N60C
Resonant inductance	L_k	10uH
Output inductance	L_o	1.5uH
Synchronous rectifier	S_1, S_2	IRF3206 (6EA)
Transformer core	T	EI3026 (2EA)
Transformer core	T_a	EI3026 (1EA)



(a) The conventional PSFB



(b) The PSFB with the proposed circuit

Fig. 11 Experimental key waveform

3.4 Less power loss in the transformer

As the 0.5 duty can be designed in the proposed PSFB converter, the turn ratio, $n=N_{s1}/N_p$, can be designed small and the RMS value of the primary side is less. The transformer loss is consisted of conduction and core loss. Since the number of the primary turns is large, the core loss of the transformer comes low[10]. Also, the conduction loss or the transformer is low because the RMS value of the primary current is small. Therefore, the proposed circuit has less power loss in the transformer than the conventional circuit as shown in Fig. 10.

4. Experimental Results

Prototype is built to verify the operation and performance of the proposed circuit with the 12V/100A output. The conventional PSFB converter is

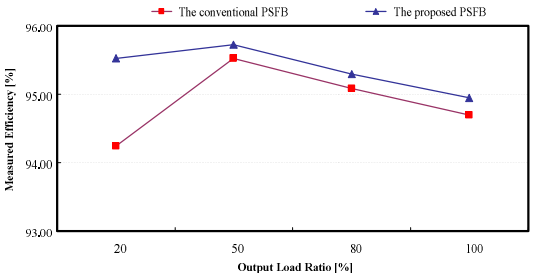


Fig. 12 The power conversion efficiency with the load variation

designed with 320V minimum voltage and 1000uF link capacitance and the proposed PSFB converter is done with 4:1 turn ratio of the auxiliary transformer to satisfy the hold up time in 320V input after the ac line is lost. Fig. 11 shows the key waveform of the conventional and proposed converter. As expected, the proposed circuit has about 0.5 duty ratio and smaller primary current. Also, the voltage stress of secondary rectifiers is less than that of the conventional PSFB converter. It results in the higher efficiency as shown in Fig. 12. The experimental results verify that the proposed circuit has the superiority in the performance and efficiency compared with the conventional converter.

5. Conclusion

The PSFB converter with the hold up time extension circuit is proposed in this paper. The proposed converter can be operated in the optimal point to get high efficiency and performance. It results in the reduced link capacitor, smaller peak value of the primary current and less output filter. Moreover, the proposed circuit has increased the power conversion efficiency which is most important in the power supply for the IT equipment. The proposed hold up time compensation circuit can easily be employed to other PWM front-end DC/DC converter. Therefore, it is expected that the proposed circuit is suitable for the front-end DC/DC converter for IT devices..

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