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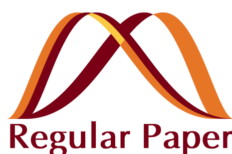

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Pillar Type Silicon-Oxide-Nitride-Oxide-Silicon Flash Memory Cells with Modulated Tunneling Oxide

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In this paper, we fabricated 3D pillar type silicon-oxide-nitride-oxide-silicon (SONOS) devices for high density flash applications. To solve the limitation between erase speed and data retention of the conventional SONOS devices, bandgap-engineered (BE) tunneling oxide of oxide-nitride-oxide configuration is integrated with the 3D structure. In addition, the tunneling oxide is modulated by another method of N_2 ion implantation (N_2 I/I). The measured data shows that the BE-SONOS device has better electrical characteristics, such as a lower threshold voltage (V_T) of 0.13 V, and a higher $g_{m.max}$ of 18.6 μA/V and mobility of 27.02 cm^2/Vs than the conventional and N_2 I/I SONOS devices. Memory characteristics show that the modulated tunneling oxide devices have fast erase speed. Among the devices, the BE-SONOS device has faster program/erase (P/E) speed, and more stable endurance characteristics, than conventional and N_2 I/I devices. From the flicker noise analysis, however, the BE-SONOS device seems to have more interface traps between the tunneling oxide and silicon substrate, which should be considered in designing the process conditions. Finally, 3D structures, such as the pillar type BE-SONOS device, are more suitable for next generation memory devices than other modulated tunneling oxide devices.

Keywords: Pillar type, SONOS, Tunneling oxide, N_2 ion implant, Bandgap engineering

1. INTRODUCTION

In the memory market, low cost, low power, high density and high performance are important factors of devices to be used in digital equipment as storage. As the potential solution for high density flash applications, many researchers have proposed the silicon-oxide-nitride-oxide-silicon (SONOS) flash memory device. The SONOS device has many benefits, such as low operating voltage, scalability, and high compatibility with conventional technologies [1,2]. In this device, to increase the date storage capacity, the multi level cell (MLC) scheme can be adopted, because with MLC, it is possible to store more than one bit in each cell, by programming the cell threshold voltage [3]. However, in the case of the MLC device, V_T fluctuations will cause a read failure, and become a prominent issue in designing a memory device. Another method is to reduce the cell size for high density memory implementation. But the limitation by reducing the device size cannot be avoided. For this, 3D devices with SONOS structure are applied to improve the electrical performances and storage capacity, such as the FiN and pillar type memory devices [4,5].

In this paper, we fabricated 3D pillar type SONOS devices for high density flash applications. It is well known that SONOS has fundamental limitations, such as slow erase speed and poor data retention characteristics at the tunneling oxide thickness of less than 2 nm. In order to solve these problems, modulated tunneling oxide schemes are integrated with the SONOS structure, such

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as N_2 ion implantation (N_2 I/I) [6], and the bandgap-engineering (BE) method [7]. In addition, flicker noise analysis is carried out, to compare each device characteristics, in particular, the interface properties.

2. EXPERIMENTS

To form the vertical silicon pillar, we used an 8-inch p-type (100) bulk wafer. Three-step chain implantation is applied for the source, channel and drain, respectively. The dopants are phosphorus (5×10^{14} cm^{-2}, 1 MeV, tilt 7°), boron (8×10^{13} cm^{-2}, 120 keV, tilt 7°) and arsenic (3×10^{15} cm^{-2}, 80 keV, tilt 7°). After implantation, these dopants are activated under 1,050℃ in nitrogen ambient for 12 second. Afterwards, the wafers are etched for the formation of a Si pillar, using *Cl_2* and *HBr* gas chemistry. Then, deposition and planarization of high density plasma silicon dioxide (SiO_2) are carried out. In the conventional and N_2 I/I devices, tunneling oxide of 5 nm is grown thermally, and a silicon nitride (Si_3N_4) charge trapping layer of 6 nm is deposited by low pressure chemical vapor deposition (LPCVD). N_2 I/I is carried out with 3×10^{15} cm^{-2} dose and 5 keV energy in the N_2 I/I device, to form a modulated tunneling oxide. In BE SONOS, the tunneling oxide consists of ONO layers, and the thickness of each layer is 2 nm. The charge trapping layer, Si_3N_4 is deposited with 6 nm, as in the conventaional and N_2 I/I devices. Then, 8 nm thick blocking oxide is deposited in each device, by LPCVD. Finally, n-type poly-Si of 180 nm thickness is deposited, to form the gate. The fabricated device structures of the conventional, N_2 I/I, and BE SONOS are shown in Figs. 1 (a), (b) and (c), respectively.

The insets of Fig. 1 show the cross-sectional diagram of the tunneling oxide/trapping layer/blocking oxide, sequentially. First, inset (a) is a cross-sectional diagram of the conventional SONOS device, and each thickness is 5/6/8 nm, respectively. Second, inset (b) is a cross-sectional diagram of the N_2 I/I SONOS device, and each thickness is the same as for the conventional device. The other point with the conventional device, is that the nitrogen atoms are arranged in a tunneling oxide. A portion of nitrogen is bonded with SiOx. This can lead to barrier height lowering, and cause band offset. Finally, inset (c) is a cross-sectional diagram of the BE-SONOS device, and each thickness is 6(2/2/2)/6/8 nm, respectively. In this case, the tunneling oxide consists of the $SiO_2/Si_3N_4/SiO_2$ layer. This also leads to the same results as the N_2 I/I device.

The electrical properties of the devices were measured at room temperature, using an Agilent 4156C analyzer.

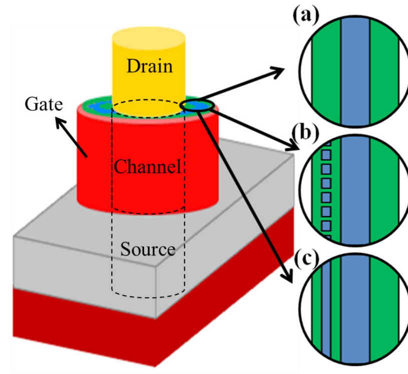

Fig. 1. The structure of pillar type SONOS memory devices, and the insets (a), (b) and (c) show cross-sections of the tunneling oxide of the conventional, N_2 I/I, and BE SONOS, respectively.

Table 1. The dc parameter extraction results of the fabricated pillar type conventional, N_2 I/I and BE-SONOS memory devices.

Pillar type SONOS	V_T (V)	SS (mV/decade)	gm.max (A/V)	Mobility (cm^2/Vs)
Conventional	0.66	140	1.42×10^{-5}	20.46
N_2 I/I	0.92	137	9.55×10^{-6}	13.76
BE	0.13	130	1.86×10^{-5}	27.02

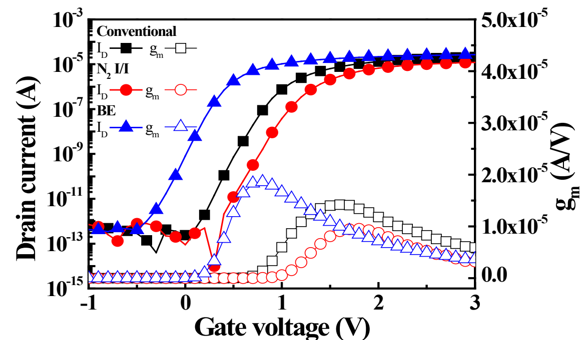

Fig. 2. Comparison of V_G-I_D and V_G-g_m characteristics of the pillar type SONOS memory devices.

3. RESULTS AND DISCUSSION

Figure 2 shows the transfer characteristic curves and transconductance (g_m) curves of each pillar type SONOS structure device. The measured sizes of pillar structure diameter and gate length are defined as 0.64 μm and 0.2 μm. The threshold voltage (V_T) values of 0.66 V, 0.92 V and 0.13 V are extracted from the conventional, N_2 I/I and BE-SONOS devices, respectively. The V_T determines the power consumption of the device. As V_T is small, a low power device can be made. The subthreshold slope (SS) that has 60 mV/decades at ideal states, $g_{m.max}$, which is defined as the change in drain current with respect to the corresponding change in gate voltage, and the mobility are also important parameters to check for device performance. Table 1 shows the dc parameter values of devices, which are extracted from the transfer characteristic curves.

The program and erase (P/E) characteristic are shown in Figs. 3(a) and (b) as a function of pulse width. First, Fig. 3(a) is the P/E characteristics at different gate voltage (V_G). In this case, the effect of modulated tunneling oxide can be known. It shows that the modulated tunneling oxide devices such as N_2 I/I and BE-SONOS have faster erase speed than the conventional device. In contrast to Fig. 3(a), Fig. 3(b) is the P/E characteristics at the same V_G. In this case, which is the more suitable device can be known. This shows that the program speed of BE-SONOS device is much faster than that of the other devices at 10 V of V_G. The erase speed is also much better than in other devices at -6 V of V_G. Therefore, the BE method is suitable to use for modulated tunneling oxide. The reason for the superior program/erase speed in BE SONOS is well known by the energy band offset [7].

In the case of the N_2 I/I device, it seems that the nitrogen bonds are implanted with SiO_x. According to a recent study, the P/E speed can be improved, using silicon oxynitride (SiON) to replace the oxygen of the tunneling oxide by nitrogen [8]. In other words, the SiON in the tunneling oxide can make a band offset, which increases the electron/hole tunneling. In this case, the barrier height of the energy band is lower, due to the energy

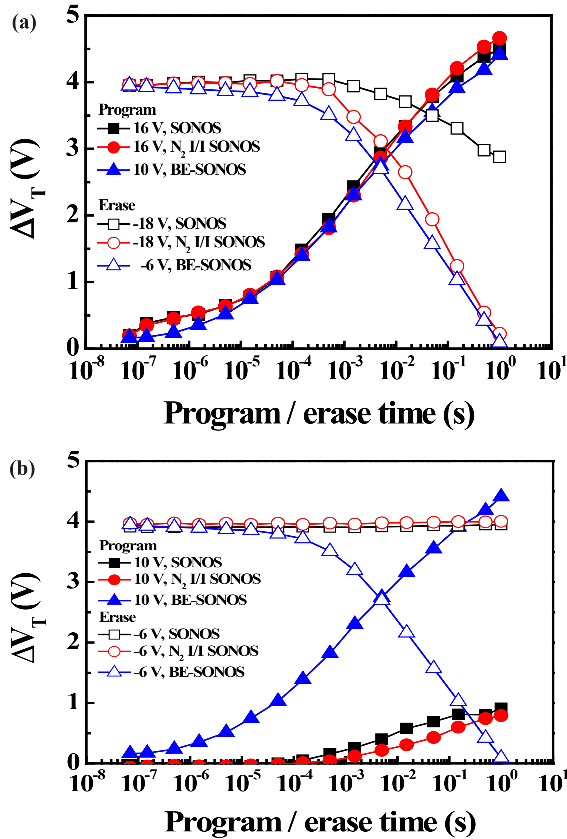

Fig. 3. Program/erase characteristic of each pillar type SONOS memory device. (a) In comparison with the BE-SONOS device, the larger program/erase gate voltage is forced to the conventional with the N_2 I/I device and (b) the same program/erase voltage is forced on each device.

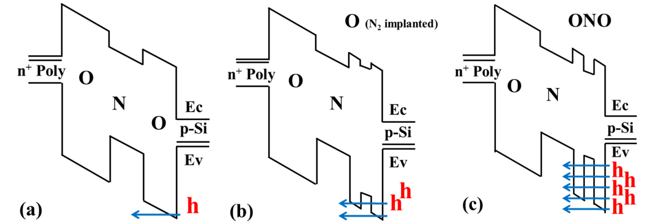

Fig. 4. Energy band diagram of each pillar type SONOS memory device. (a) conventional, (b) N_2 I/I, and (c) BE SONOS device. The bandgap of SiO_2 and Si_3N_4 is about 8.9, 5.1 eV, respectively. The SiON bandgap is between 5.1 and 8.9 eV.

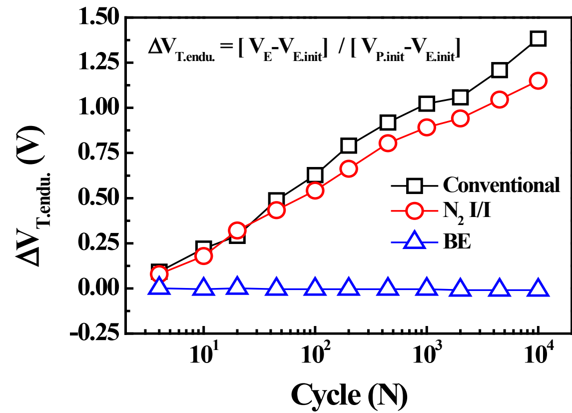

Fig. 5. Endurance characteristics of each pillar type SONOS memory device. The condition of program/erase voltages and times of the conventional, N_2 I/I and BE-SONOS are 16 V 100 ms / -19 V 100 ms, 15 V 10 ms / -19 V 100 ms and 12 V 1 ms / -9 V 60 ms, sequentially.

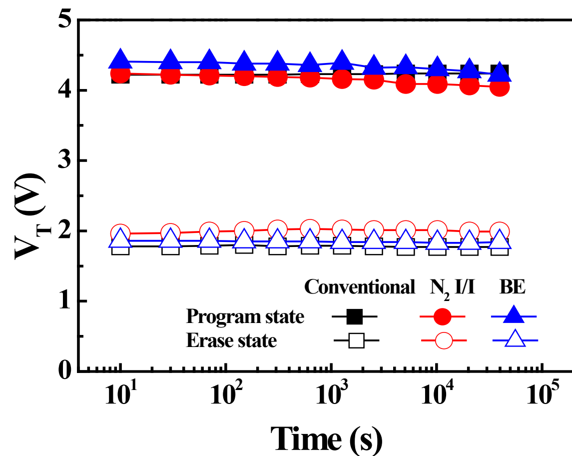

Fig. 6. Data retention characteristics of each pillar type SONOS memory device. Applied voltages at the program state are 17 V 5 ms, 17 V 50 ms and 12 V 10 ms in the conventional, N_2 I/I, and BE-SONOS, respectively. In the case of the erase state, the applied voltages are 12 V 2 ms, -19 V 100 ms and -9 V 20 ms, sequentially.

band gap of SiO_2 being 8.9 eV, and that of SiON being 5.1~8.9 eV. The barrier heights of conventional, N_2 I/I and BE devices are 3.05 eV, 2.7 eV and 0.35 eV for the electron, and 4.6 eV, 3.65 eV and 1.9 eV for the hole, respectively. The reason for increased electron/hole tunneling can be confirmed in Fig. 4. The band offset of the conventional device is 0, of the N_2 I/I device is approximately 0.95 eV, and of the BE device is 2.7 eV. In this case, the charges can move easily from band to band. As shown in Fig. 4, the larger the energy band offset becomes, the more easily charges can move, due to the reduction of thickness of the tunneling path while the voltage is applied.

The higher program/erase speed of the BE-SONOS device means that lower voltage operation is possible. When the program/erase voltage is lowered, the endurance characteristics can be improved. Fig. 5 shows the endurance properties of pillar type SONOS memory devices at different program/erase voltages, to adjust the program/erase speed. The $\Delta V_{T.endu.}$ equation is shown below.

$$\Delta V_{T.endu.} = \frac{V_E - V_{E.init.}}{V_{P.init.} - V_{E.init.}}$$

where, $V_{P.init.}$ and $V_{E.init.}$ are the V_T, when the P/E voltage is applied the first time. The V_E is the V_T when the erase voltage is applied at various times. The $\Delta V_{T.endu.}$ means that as the value increases, V_E nearly approaches $V_{P.init}$. In this case, it is explained that the device is degraded. From Fig. 5, it is known that the BE-SONOS device is more stable than other devices.

Figure 6 presents the data retention characteristics of each pillar type SONOS device, when the device is programmed and erased with V_T = 4 V and 2 V, respectively. This shows that all the devices have good data retention characteristics. The reason

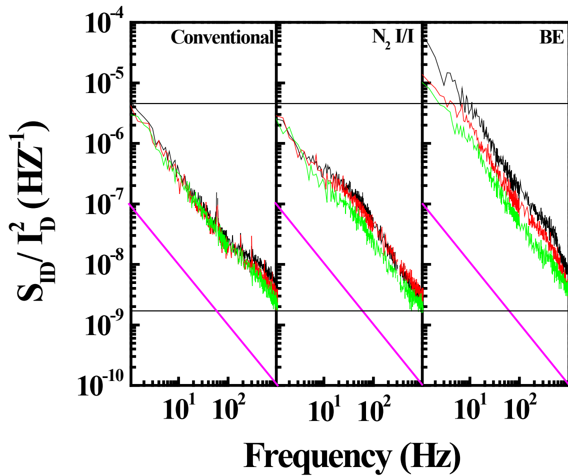

Fig. 7. Normalized drain current noise spectra density versus frequency of pillar type SONOS memory devices.

can be explained by the thick tunneling oxide thickness, and the trapping layer using Si_3N_4 has strong charge trapping properties [9]. In other words, the stored charge can leak less than 2 nm of tunneling oxide. However, the tunneling oxide thickness among the devices is thicker than 2 nm, as follows: the conventional, N_2 I/I and BE-SONOS device has 5 nm, 5 nm and 6 nm, respectively. In addition, before using Si_3N_4 as a trapping layer, poly-Si, which has a conductor characteristic, is widely used as a trapping layer. The Si_3N_4 has an insulator characteristic, so charge stored properties of Si_3N_4 are better than poly-Si. That is, under a high electric field, the band offset of an ultra-thin O1/N1/O_2 will block out the tunneling barrier of the N1 and O_2 layers, and the tunneling distance for holes can effectively be reduced to O1, which will induce a large hole current. The retention characteristics can also be improved, because the total thickness of O1/N1/O_2 will prohibit the direct tunneling of holes in a low electric field.

In order to evaluate the interface characteristic or tunneling oxide quality, flicker noise analysis is carried out [10]. As shown in Table 1, the three devices have similar SS values, and this means that interface comparison is difficult by SS value. Fig. 7 shows the normalized drain current noise spectra density (S_{ID}/I^2_D) of pillar type SONOS memory devices. The measured S_{ID}/I^2_D of pillar type devices is much higher than previously reported values in a SONOS device [11], but the S_{ID}/I^2_D is clearly in inverse proportion to the frequency. From the noise level, the interface characteristics or tunneling oxide quality of conventional and N_2 I/I devices are similar. That is, the implanted N_2 ions are located above the interface of at least 2 nm, and both the devices have similar interface characteristics or tunneling oxide qualities. The noise level of the BE-SONOS device, however, is larger than the conventional and N_2 I/I devices, by about 1 order. This analysis result can be explained by the BE-SONOS device having more traps or defects in tunneling oxide, due to the nitride layer of ONO as tunneling oxide, which should be considered in applying the BE-SONOS devices.

4. CONCLUSIONS

In this paper, we fabricated, characterized and compared the conventional pillar type, N_2 I/I and BE-SONOS memory devices. Compared with the conventional SONOS device, modulated tunneling oxide devices show improved erase speed, and seem to be proper for the next generation memory application. In particular, the BE-SONOS device shows higher P/E speed performance than other devices, due to the large energy band offset. Charges can easily move from band to band, when the bias is applied. The flicker noise, however, confirms that the BE-SONOS device has more traps or defects in the tunneling oxide, which should be considered carefully, in designing the process conditions.

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