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A CMOS Impulse Radio Ultra-Wideband Receiver for Inner/Inter-chip Wireless Interconnection

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Abstract

This paper presents a CMOS impulse radio ultra-wideband (IR-UWB) receiver implemented using IBM 0.13um CMOS technology for inner/inter-chip wireless interconnection. The IR-UWB receiver is based on the non-coherent architecture which removes the complexity of RF architecture (such as DLL or PLL)and reduces power consumption. The receiver consists of three blocks: a low noise amplifier (LNA) with active balun, a correlator, and a comparator. Simulation results show the die area of the IR-UWB receiver of 0.2mm2, a power gain (S21) of 12.5dB, a noise figure (NF) of 3.05dB, an input return loss (S11) of less than -16.5dB, a conversion gain of 18dB, a NFDSB of 22. The receiver exhibits a third order intercept point (IIP3) of -1.3dBm and consumes 22.9mW of power on the 1.4V power supply.

Keywords: UWB receiver, non-coherent receiver, inner/inter-chip communications.

Ⅰ. Introduction

Impulse radio ultra-wideband (IR-UWB) is an attractive wireless transmission technology which enables high band-width short distance communications. The UWB communications does not require expensive and complex components for modulation and demodulation and IF stages, and thus reducing cost, size, weight, and power consumption of the system [1-3]. In 2002, the Federal Communications Commission (FCC) released an unlicensed frequency range of 7.5GHz, from 3.1GHz to 10.6GHz, for the commercial short-range wireless communication applications [4]. In recent years, a number of research works focused on inner/inter-chip wireless interconnections by using IR-UWB communicationsdue to its low complexity and low power [5-17]. In IR-UWB systems, the receiver is an important component and is more complex than the transmitter. There are basically two different types of receivers employed in IR-UWB systems namely coherent receiver and non-coherent receiver. The coherent and non-coherent architectures have been reported in the literature [5-7]. Both coherent and non-coherent receivers correlate the received pulse first, such that the center frequency is down-converted to baseband. The difference is that in a coherent receiver, the received pulse correlates with a local template pulse and needs many timing synchronization circuit blocks which increases system complexity. In a noncoherent receiver, the received pulse correlates with itself andremoves the complexity of RF architecture (DLL or PLL)and reduces power consumption.

In this paper, an IR-UWB based non-coherent single chip CMOS receiver is presented. The on chip receiver is implemented using 0.13um CMOS technology. The receiver covers 6.0~10.6 GHz that is the high frequency band of the UWB system.

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II. IR-UWB Receiver Circuit Design

The proposed IR-UWB receiver employs the non-coherent receiver architecture. Figure 1 shows the block diagram of the fully integrated IR-UWB receiver.

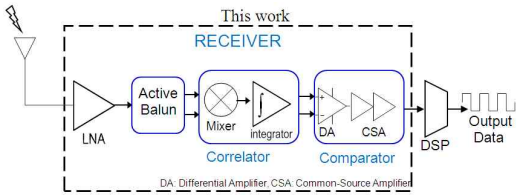

Figure 1. Block diagram of the fully integrated IR-UWB receiver

The received UWB signal is amplified through a low-noise amplifier (LNA) with an active balun. This amplifier provides a constant gain optimized around the operation frequency of 8.0 GHz. After first being amplified by the LNA, the received pulse is then self-correlated by a correlator, and then sent to a comparator for digital quantization.

A. LNA and Active Balun: The UWB LNA design uses resistive feedback current reuse technique. The design was implemented in the IBM 0.13um CMOS technology with appropriate impedance matching and noise/power optimizations. The LNA achieves up to 12.5dB power gain with a noise figure (NF) of 3.05dB over the UWB 3.1-10.6GHz frequency range. Figure 2 shows the schematic of LNA.

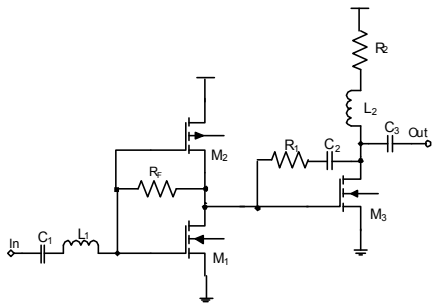

Figure 2. Schematic diagram of the LNA

The input inductor L_1 is added to compensate for the parasitic capacitors of M_1 and M_2 transistors at high frequencies. A resistive feedback buffer with peaking inductor load is coupled with the reuse UWB stage through capacitor C_3 to drive the 50Ohm output load. Besides, in the resistive feedback current reuse configuration (the first stage), loading the NMOS transistor M_1 with the PMOS transistor M_2 allows the circuit to operate under lower supply voltage than resistive load configuration.

A two-cascode stage active balun (Figure 3)is used to convert the single-ended output of the LNA to differential signals. The output of M4 connects to M6 and the input of the second cascode. Since $v_{gs5}=-v_{gs6}$, two balanced differential outputs can be achieved if $g_{m5}=g_{m6}$

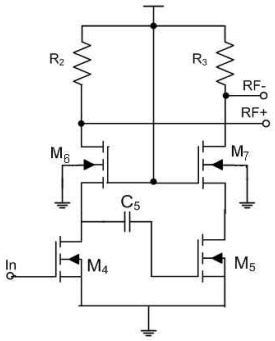

Figure 3. Schematic diagram of the active balun

B. Correlator: The output of the LNA must be correlated - multiplied and then integrated in order to detect the energy of the received signal. Figure 4 shows the block diagram of correlator. Equation (1) shows the output signal of correlator.

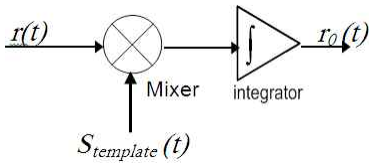

Figure 4. Block diagram of the correlator

$$r_0(t) = \int_{t_0-T}^{t_0} r(t).S_{template}(t)dt \quad (1)$$

where $r_0(t)$ is the output signal of the correlator,

$r(t)$ is the input signal of the correlator and $S_{template}(t)$ is the template signal.

Figure 5 shows the schematicof correlator. The correlator employs a Gilbertmixer topology, andthe integrator is realized by capacitors C1 and C2. After the pulse ismixed with itself, the integrator begins to integrate between the pulses intervals, the integrator discharges and is ready for the next integration. The capacitances of C1 and C2 should be large enough to hold the integrated voltage for the comparator and yet small enough to discharge between pulses intervals in order to be ready for the next integration. This speed can determine the transmission data rate.

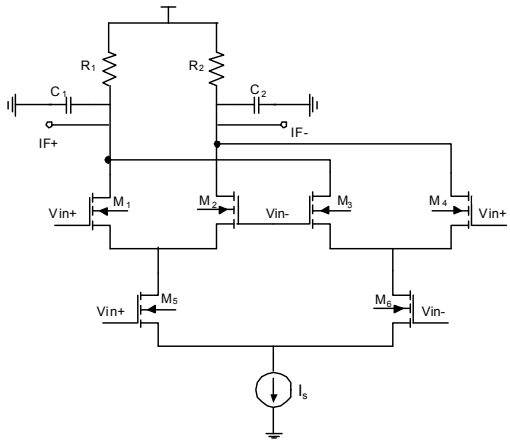

Figure 5. Schematic diagram of the correlator

C. Comparator: After the received signal is squared and integrated by the correlator, a comparator compares it with a reference voltage and performs digital quantization. However the comparator output is a return-to-zero (RZ) signal which needs to be converted to a non-return-to-zero (NRZ) signal that can synchronize with the baseband clock. In a coherent receiver, a DLL/PLL is usually introduced to perform synchronization between the received pulse and the local pulse, needing precision on the order of several tens of picoseconds. However, in a noncoherent receiver, the RZ signal quantized by the comparator exhibits a duty cycle on the order of nanoseconds. Therefore, a low jitter DLL/PLL is no longer necessary and a sliding correlator is employed. The technique reduces complexity of the receiver.

The topology of the comparator consists of differential amplifier with buffering inverter and common-source amplifier. The block diagram and the schematic diagram of the comparator are shown in Figure 6 and Figure 7, respectively.

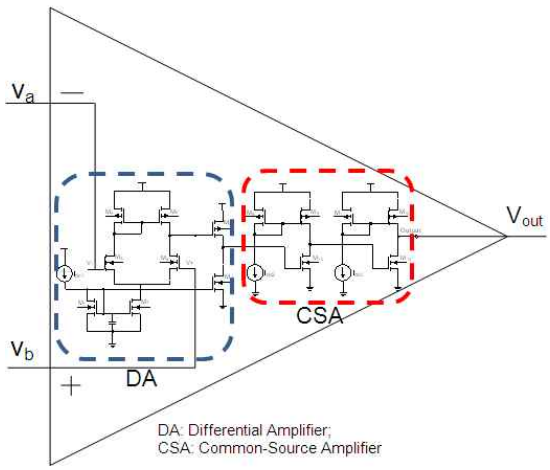

Figure 6. Block diagram of the comparator

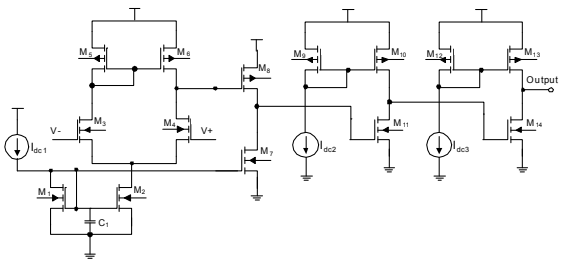

Figure 7. Schematic diagram of the comparator

The comparator is based on a differential amplifier with two differential inputs (v_a and v_b).

-The input voltage is in the differential-mode:

$$V_{ID} = v_a - v_b \tag{2}$$

-The input voltage is in the common-mode:

$$V_{IC} = \frac{v_a + v_b}{2} \tag{3}$$

From (2) and (3),

$$v_a = V_{IC} + \frac{V_{ID}}{2} \quad \text{and} \quad v_b = V_{IC} - \frac{V_{ID}}{2} \tag{4}$$

-The output voltage:

$$V_{out} = A_{VD}V_{ID} \pm A_{VC}V_{IC} = A_{VD}(v_a - v_b) \pm A_{VC}\left(\frac{v_a + v_b}{2}\right) \tag{5}$$

where

A_{VD} is amplification factor in the differential-mode.

A_{VC} is amplification factor in the common-mode

III. Simulation Results

The IR-UWB receiver was designed and simulated using Cadence tools applicable in IBM 0.13um CMOS technology. The simulation result of the IR-UWB waveforms is shown in Figure 8. The waveforms are listed as: A is the received signal from the antenna, B is the output of the LNA, C is the output of the correlator, and D is the output of the comparator.

The amplitude of output voltage of the correlator is different (e.g. at 6ns and 11ns or 26ns and 31ns) because they were affected by the amplitude of impulse radio UWB receiver. In the comparator we used the op-amps and a vdc (vpulse) with amplitude of 1.4V for UWB receiver. The op-amps can amplify almost all signals that the amplitude of output voltage of equal mico volt. The output signal of the comparator is the bit stream.

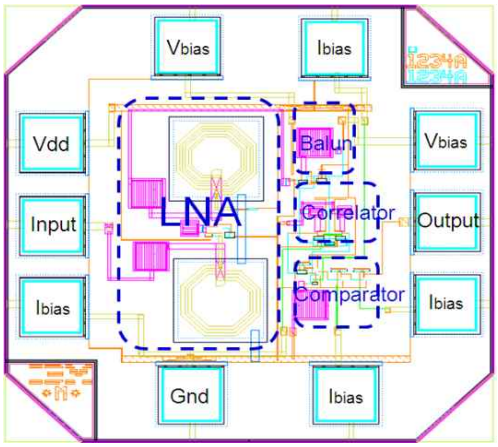

Figure 9. Layout of the IR-UWB receiver

Figure 9 shows the layout view of the IR-UWB receiver. The area of the receiver is about 0.2mm^2. The power consumption of the receiver is 22.9mW for the 1.4V supply voltage. Table 1 shows the parameters of the IR-UWB receiver.

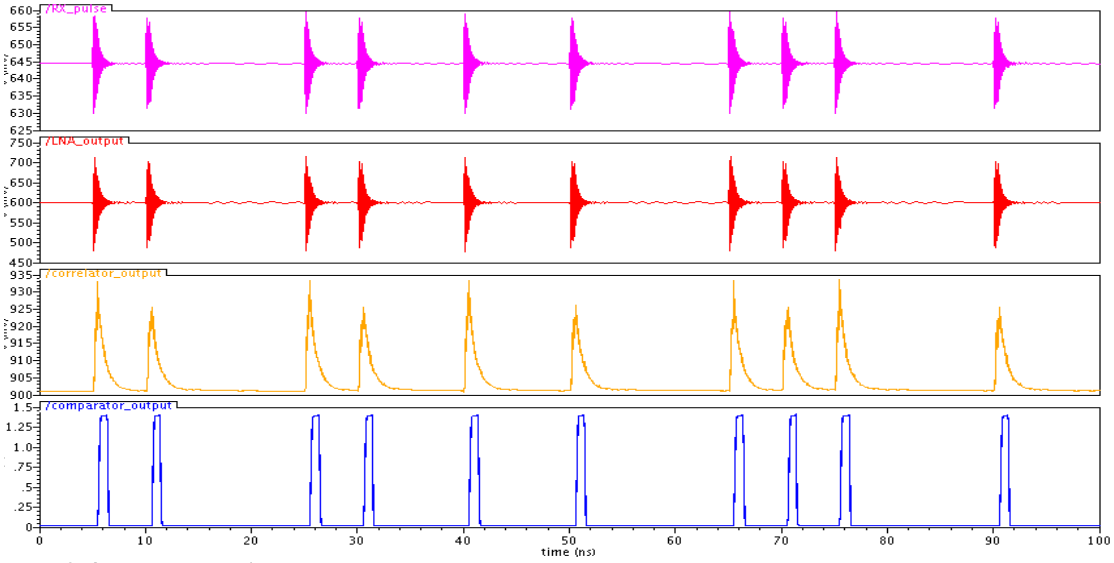

Figure 8. Simulation result of the IR-UWB receiver

Table 1: COMPARISON WITH PREVIOUSLY REPORTED IR-UWB RECEIVERS

Parameters	This work	[16]	[17]
Technology	0.13um CMOS	0.13um CMOS	0.18um CMOS
Bandwidth (GHz)	6.0-10.6	3.1-10.6	3.1-5.0
S11 (dB)	< -16.5	< -10	< -9.1
Gain Max(dB) (S21)	12.5	17	< 30
NF (dB)	3.05	4 to 5.1	4.3
Conversion Gain(dB)	18	29	-
IIP3 (dBm)	-1.3	-14	-
Power (mW)	22.9	31.5	21.9
Chip Area (mm^2)	0.2	-	1.8

Ⅴ. Conclusion

In this work, a CMOS non-coherent IR-UWB receiver was designed and simulated using Cadence tool with IBM 0.13um CMOS technology for inner/inter-chip wireless interconnection. The results show a promising design for 3-D chip wireless communications due to its low complexity and small chip area. Appropriate choices of the charge and discharge capacitance in the correlator will further more increase the system data rate.

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