JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.13, NO.6, DECEMBER, 2013 http://dx.doi.org/10.5573/JSTS.2013.13.6.655

Dependence of the 1/f Noise Characteristics of CMOSFETs on Body Bias in Sub-threshold and Strong Inversion Regions

Sung-Kyu Kwon*, Hyuk-Min Kwon*, Ho-Young Kwak*, Jae-Hyung Jang*, Jong-Kwan Shin*, Seon-Man Hwang*, Seung-Yong Sung*, Ga-Won Lee*, Song-Jae Lee*, In-Shik Han, Yi-Sun Chung**, Jung-Hwan Lee**, and Hi-Deok Lee*,†**

***Abstract*—In this paper, the 1/f noise characteristics of n-channel MOSFET (NMOSFET) and p-channel MOSFET (PMOSFET) are analyzed in depth as a function of body bias. The normalized drain current noise, S_{ID}/I_D^2 showed strong dependence on the body bias in the sub-threshold region for both NMOSFET and PMOSFET, and NMOSFET showed stronger dependence than PMOSFET on the body bias. On the contrary, both of NMOSFET and PMOSFET do not exhibit the dependence of S_{ID}/I_D^2 on body bias in strong inversion region, although the noise mechanisms of two MOSFETs are different from each other.**

***Index Terms*—CMOSFET, 1/f noise, NMOSFET, PMOSFET, body bias, sub-threshold region**

I. INTRODUCTION

Low frequency noise has become one of the major issues for analog/mixed signal and radio frequency (RF) circuits [1-4]. This is mainly due to the improvement of device performance by the continuous scaling down of the gate length of the metal oxide semiconductor field effect transistors (MOSFETs). Recently, the demand for low power consumption has increased due to the development of single battery mobile appliances. Therefore, to reduce the dynamic power consumption of complementary metal oxide semiconductor (CMOS) circuits the threshold voltage must be scaled down along with the supply voltage without degrading the circuit speed or the operating logic noise margins. Although the threshold voltage scaling is limited by the off-current and static power consumption constraints, a constant substrate biasing technique is used with standard CMOS technology to improve the performance of CMOS circuits [5]. Forward biasing the substrate reduces the threshold voltage of the MOSFET and increases the speed of the device in analog/mixed signal CMOS circuits. Reverse body biasing is attractive for low current CMOS applications as the device's active mode current decreases, and this means the signals become comparable with the low frequency noise (LFN) [6]. As this technique can be used in analog integrated circuits such as the current mirror and voltage controlled oscillator (VCO), the dependence of 1/f noise characteristics on body bias needs to be analyzed. However, there are few reports on the analysis of noise characteristics considering the body biases in the sub-threshold and strong inversion regions [7, 8].

Previous experiment showed 1/f noise characteristics with various body bias in sub-threshold region [9]. However, it showed NMOSFET's characteristics only and the analysis was not quite clear. Thus, in this study, the 1/f noise characteristics of both NMOSFETs and PMOSFETs were investigated concurrently and

Manuscript received Jun. 20, 2013; accepted Oct. 16, 2013
* Dept. of Electronics Engineering, Chungnam National University, Daejeon 305-764, Korea
** Magnachip Semiconductor, Cheongju, Chungbuk 361-725, Korea
† E-mail : hdlee@cnu.ac.kr, Tel : +82-42-821-6868

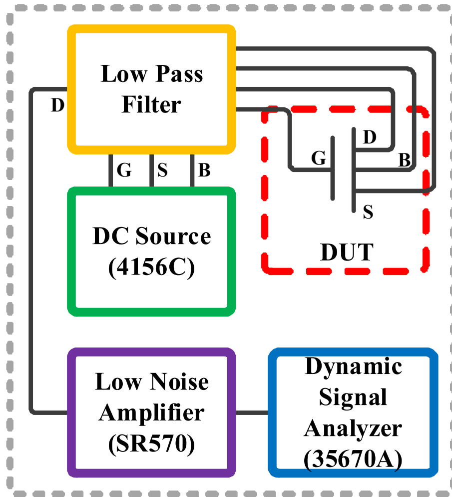


Fig. 1. Apparatus configuration to measure flicker (1/f) noise.

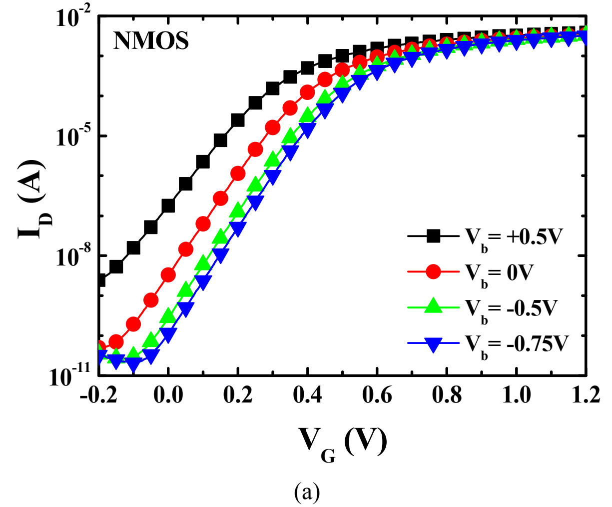
systematically for various body biases from the sub-threshold to strong inversion regions. Moreover, the noise characteristics were analyzed as a function of drain current with a variable of body bias for both NMOSFET and PMOSFET.

II. Experimental Details

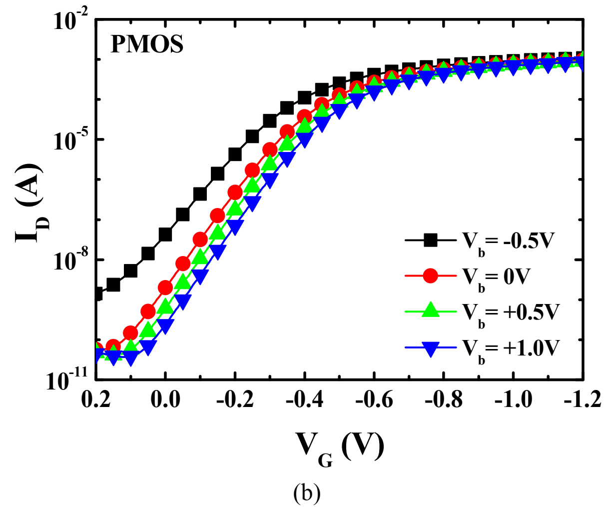
Conventional NMOSFET and PMOSFET with a gate width of 20 μm and length of 0.13 μm were used for the analysis of the low frequency noise (LFN) characteristics. The LFN measurements were performed in a shielded probe station. The device under test (DUT) was biased using an HP 4156C Parameter analyzer and the drain current noise was amplified with an SR 570 low noise current amplifier. The apparatus configuration is schematically shown in Fig. 1. The drain current noise power spectral density (PSD), S_{ID}, was measured using an HP 35670A dynamic signal analyzer in the frequency range of 1 Hz to 12.8 kHz. The DC characteristics of both NMOSFET and PMOSFET were measured prior to 1/f noise measurements. To observe the body bias dependence of 1/f noise, the constant body bias in the range of +0.5 V to –0.75 V for NMOSFETs and –0.5 V to +1 V for PMOSFETs was applied to the substrate during the LFN measurements.

III. Results and Discussion

Figs. 2(a) and (b) show the DC characteristics of



(a)



(b)

Fig. 2. Drain current versus gate bias characteristics with a body bias variable (a) NMOSFET [8], (b) PMOSFET.

NMOSFET and PMOSFET with a body bias variable. The depletion width increases under the reverse body bias and decreases under the forward body bias due to the change of potential difference between the source and the body junction. The depletion charge is expressed by

$$Q_D = -eN_{sub}X_d = -\sqrt{2q\varepsilon_{si}N_{sub}(2|\phi_{fb}|+V_{BS})} \quad (1)$$

where N_{sub} is the body doping density, X_d is the depletion width, ε_{si} is the dielectric constant for silicon, φ_{fb} is the flat band potential, and V_{BS} is the applied body bias. Under reverse body biasing, the drain saturation current decreases due to the increased threshold voltage. The forward body biasing causes the decrease of depletion

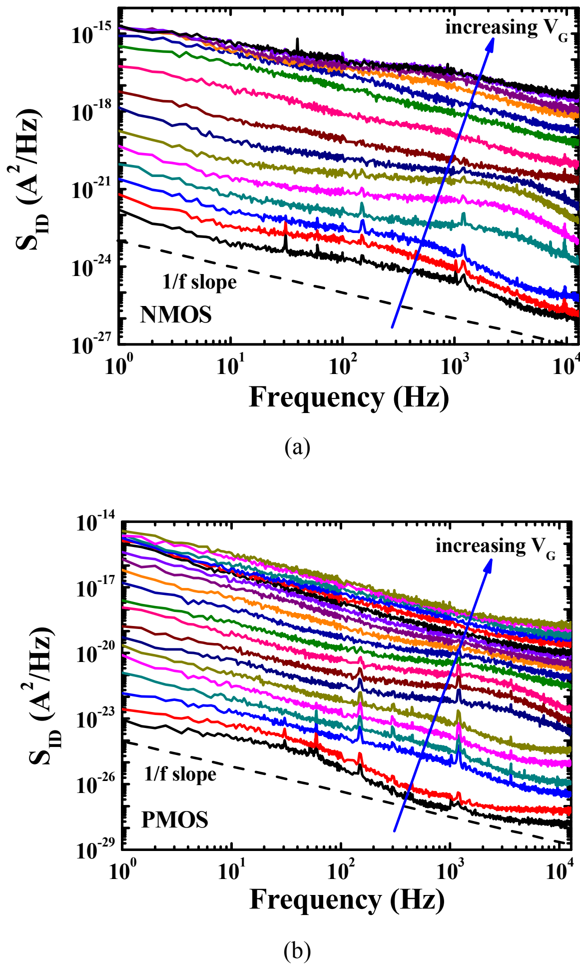


Fig. 3. Typical flicker noise slope with various gate voltages under zero body bias (a) NMOSFET, (b) PMOSFET.

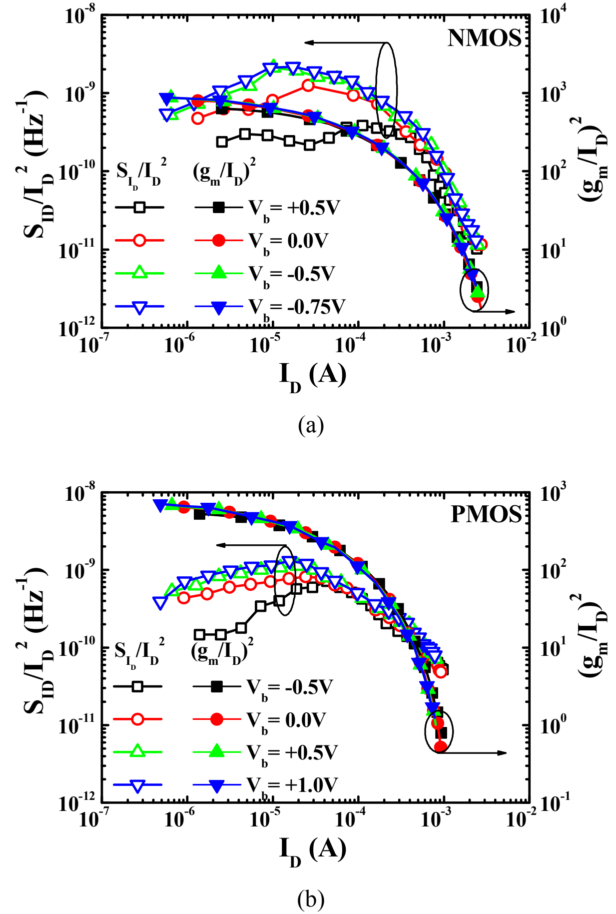


Fig. 4. Variation of a normalized drain current power spectral density versus a drain current with a body bias variable (a) NMOSFET [8], (b) PMOSFET.

charges and results in a decrease of the threshold voltage and an increase of the drain saturation current.

Figs. 3(a) and (b) shows the typical flicker noise shape of NMOSFET and PMOSFET under zero body bias. The drain current noise power spectral density level of NMOSFET and PMSOFET are increased with increasing gate bias as well known.

Fig. 4(a) shows the variation of the normalized drain current noise power spectral density, (S_{ID}/I_D^2) against the drain current (I_D) with the various body biases for NMOSFET. The normalized drain current noise shows similar trend with the square of the normalized transconductance $(g_m/I_D)^2$ in the strong inversion region, which implies the carrier number fluctuations [10].

Fig. 4(b) shows the noise power spectral density (S_{ID}/I_D^2) against the drain current (I_D) with various body biases for PMOSFET. The normalized drain current noise does not follow the trend of the square of the normalized transconductance $(g_m/I_D)^2$ from the sub-threshold to the strong inversion region, which means that the carrier mobility fluctuation is the dominant mechanism [10].

When the gate voltage is below the threshold voltage, the surface is in weak inversion and the current flow is dominated by diffusion. The normalized flicker noise expression [11] in weak inversion is given below,

$$\frac{S_{ID}}{I_D{}^2} = \frac{q^4 \lambda Nt}{kTWLf(C_{ox} + C_D + C_{it})^2} \tag{2}$$

where λ is the tunnel attenuation distance of the electron and hole in the oxide (λ is 0.1 nm), N_t is the oxide trap density, k is the Boltzman's constant, T is the absolute temperature, W and L are the width and the length of the channel, and C_{ox}, C_D, and C_{it} are the oxide, depletion, and

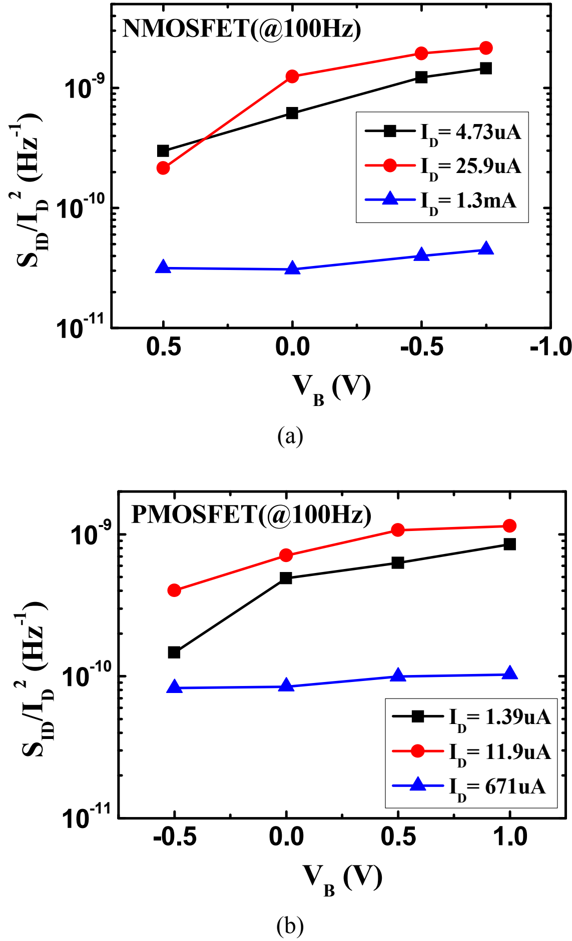


Fig. 5. Variation of normalized drain current power spectral density versus various body biases at 100 Hz (a) NMOSFET, (b) PMOSFET.

interface charge capacitance per unit area respectively.

From the equation, it can be seen that the normalized flicker noise is dependent on the depletion capacitance and the depletion capacitance is V_{BS} dependent. The depletion capacitance decreases with increasing reverse body bias and it causes increase of the normalized drain current in weak inversion region.

Fig. 5 shows the normalized drain current noise power spectral density of NMSOFET and PMOSFET as a function of body bias. As we can see in Figs. 5(a) and (b), the normalized drain current noise PSD increases with the increased reverse body bias in the sub-threshold region, mainly due to the decrease of the depletion capacitance (C_D) in both NMOSFET and PMOSFET.

As the reverse body bias increasing, the depletion region is increased for both NMOSFET and PMOSFET. Enlarged depletion area with reverse body bias results in decrease of the depletion capacitance. However, there is not much difference in the strong inversion region, and this can be explained by considering the charge conservation principle [6]. The variation of the inversion charge δQ_{inv} is given by

$$\delta Q_{inv} = \frac{-C_{inv}}{C_{ox} + C_D + C_{it} - C_{inv}} \delta Q_{ox} \quad (3)$$

where C_{inv}, C_{ox}, C_D and C_{it} are the inversion, oxide, depletion and interface charge capacitance per unit area respectively. Assuming that $C_{inv} \gg C_{ox}+C_D+C_{it}$ in the strong inversion region, the variation of the inversion charge is the same as the fluctuation of the oxide trapped charge that is, $\delta Q_{inv} \fallingdotseq \delta Q_{ox}$. Thus, the depletion layer becomes negligible in this region and the noise level will not be affected by the body bias V_{BS}. From that the normalized drain current noise PSD varies less in strong inversion region than that of in sub-threshold region with body bias.

IV. Conclusions

The dependence of the flicker noise characteristics of NMOSFET and PMOSFET from the sub-threshold region to strong inversion region has been investigated. NMOSFET follows the number fluctuation mechanism and in case of PMOSFET the mobility fluctuation mechanism dominates the flicker noise. The normalized drain current noise level increased as the reverse body bias increased in the sub-threshold region due to the decrease of the depletion capacitance for both NMOSFET and PMOSFET. On the contrary, both MOSFETs do not affected by the applied body bias in strong inversion region. This additional study of flicker noise characteristics from the sub-threshold to strong inversion region with various body biases is worthwhile, especially for the low power application of the CMOSFETs.

Acknowledgments

This work(research) is financially supported by the Ministry of Knowledge Economy(MKE) and Korea Institute for Advancement of Technology(KIAT) through the Workforce Development Program in Strategic Technology.

REFERENCES

[1] J.W. Wu, J.W. You, H.C. Ma, C.C. Cheng, C.F. Hsu, G.W. Huang, C.S. Chang and Tahui Wang, "Low Frequency Noise Degradation In Ultra-Thin Oxide(15Å)Analog n-MOSFETs Resulting From Valence-Band Tunneling," *Proceedings. IEEE International Reliability Physics Symposium*, pp. 260-264, Apr. 2005.

[2] H.M. Kwon, J.D. Bok, I.S. Han, S.U. Park, Y.J. Jung, J.H. Jang, S.Y. Ko, W.M. Lee, G.W. Lee and H.D. Lee, "Dependence of hot carrier reliability and low frequency noise on channel stress in nano-scale n-channel metal-oxide-semiconductor field-effect-transistors," *Japanese Journal of Applied Physics,* Vol.50, No.10, pp.10PB01(1-5), Oct. 2011.

[3] I.S. Han, H.M. Kwon, J.D. Bok, S.K. Kwon, Y.J. Jung, W.I. Choi, D.S. Choi, G. Lim, Y.S. Chung, J.H. Lee, G.W. Lee and H.D. Lee, "Effect of Nitrogen Concentration on Low-Frequency Noise and Negative Bias Temperature Instability of p-Channel Metal-Oxide-Semiconductor Field-Effect Transistors with Nitrided Gate Oxide," *Japanese Journal of Applied Physiscs,* Vol.50, No.10, pp.10PB03(1-4), Oct. 2011.

[4] J.H. Lee, S.Y. Kim, I. H. Cho, S. B. Hwang and J.H. Lee, "1/f noise Characteristics of Sub-100nm MOS Transistors," *Journal of Semiconducor Technology and Science*, Vol. 6, No.1, pp.38-42, Mar., 2006.

[5] Y.A. Allogo, M. Marin, M. de Murcia, P. Linares and D. Cottin, "1/f noise in 0.18um technology n-MOSFETs from Subthreshold to saturation," *Solid-State Electronics*, Vol.46, No.7, pp.977-983, Jul., 2002.

[6] M.J. Deen, and O. Marinov, "Effect of forward and reverse substrate biasing on low-frequency noise in silicon PMOSFETs," *IEEE Transactions on Electron Devices,* Vol.49, No.3, 409-413, Mar., 2002.

[7] G. Reimbold, "Modified 1/f trapping noise theory and experiments in MOS transistors biased from weak to strong inversion—Influence of interface states," *Electron Devices, IEEE Transactions on*, Vol.31, No.9, pp.1190-1198, Sep. 1984.

[8] N.K. Park and K.O. Kenneth, "Body bias dependence of 1/f noise in NMOS transistors from deep-subthreshold to strong inversion," *IEEE Transactions on Electron Devices,* Vol.48, No.5, pp.999-1001, May. 2001.

[9] S. K. Kwon, H.Y. Kwak, H.M. Kwon, J.H. Jang, Y.J. Jung, S.S. Kim, D.S. Lee, J.K. Lee, S.J. Lee, and H.D. Lee, "Dependence of 1/f noise characteristics of NMOSFETs on body bias and temperature in sub-threshold region," *Symposium on International Semiconductor Device Research (ISDRS),* pp.1-2, Dec. 2011.

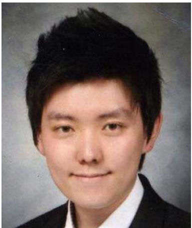
[10] L. K. J. Vandamme, X. Li and D. Rigaud, "1/f noise in MOS devices, mobility or number fluctuations?," *IEEE Transactions on Electron Devices,* Vol.41, No.11, pp.1936-1945, Nov. 1994.

[11] G. Ghibaudo, O. Roux, Ch. Nguyen-Duc, F. Balestra and J. Brini, "Improved Analysis of Low Frequency Noise in Field-Effect MOS Transistors," *Physica Status Solidi (a)*, Vol. 124, No.2, pp.571-581, Apr. 1991.

Sung-Kyu Kwon received the B.S. degree and M.S. degree in electronics engineering from the Chungnam National University, Daejeon, Korea in 2011 and 2013. Since 2013, he has been a Ph.D. student in electronics engineering from the Chungnam National University, Daejeon, Korea. His main research interests include reliability and low frequency noise characteristics of nano-CMOS devices for analog mixed signal application.

Hyuk-Min Kwon received the B.S. and M.S. degree in electronics engineering from the Chungnam National University, Daejeon, Korea in 2007 and 2009. Since 2009, he has been a Ph.D. student in electronics engineering from the Chungnam National University, Daejeon, Korea. His main research interests include characterization and reliability of nano-scale CMOS device and MIM capacitor for analog mixed signal applications, and he is currently focusing on characterization and reliability of high-k dielectric and Ge-MOSFET. His research interest also includes research of test pattern for matching and low frequency noise characteristics in analog mixed signal application.

Ho-Young Kwak received the B.S. degree in electronics engineering from the Chungnam National University, Daejeon, Korea in 2011. Since 2011, he has been a M.S. student in electronics engineering from the Chungnam National University, Daejeon, Korea. His main research interests include characterization and reliability of high-k dielectric of CMOS device for analog mixed signal applications



Jae-Hyung Jang received the B.S. degree in electronics engineering from the Chungnam National University, Daejeon, Korea in 2011. Since 2011, he has been a M.S. student in electronics engineering from the Chungnam National University, Daejeon, Korea. His main research interests include test pattern for matching characterization of CMOS device for analog mixed signal applications.

Jong-Kwan Shin received the B.S. degree in electronics engineering from the Chungnam National University, Daejeon, Korea in 2012. Since 2012, he has been a M.S. student in electronics engineering from the Chungnam National University, Daejeon, Korea. His main research interests include characterization of RF CMOS and modeling.

Seon-Man Hwang received the B.S. degree in electronics engineering from the Chungnam National University, Daejeon, Korea in 2012. Since 2012, he has been a M.S. student in electronics engineering from the Chungnam National University, Daejeon, Korea. His main research interests include test pattern for matching characterization of CMOS device for analog mixed signal applications.

Seung-Yong Sung received the B.S. degree in electronics engineering from the Chungnam National University, Daejeon, Korea in 2012. Since 2012, he has been a M.S. student in electronics engineering from the Chungnam National University, Daejeon, Korea. His main research interests include characterization and reliability of nano-scale CMOS device and EDMOS for analog mixed signal applications.

Song Jae Lee received his BS, MS, and PhD degrees from Seoul National University, Department of Electronics Engineering in 1980, Korea Advanced Science and Technology, Department of Electronics Engineering in 1982, and University of Florida, Department of Electrical Engineering in 1990, respectively. In 1992, after working as a senior engineer at Samsung Electronics, Compound Semiconductor Division, he joined the faculty of the Chungnam National University in the Electronics Engineering Department. Since then he has worked on developing high-brightness light-emitting diodes and developed a powerful Monte Carlo photon simulation program for the analysis and design of LED lamps, including chips, packages, and lenses. He recently extended his research activity to LCD backlight design, based on either LEDs or side-emitting twisted plastic optical fibers driven by visible laser diodes.

Ga-Won Lee received a B.S., M.S., and Ph.D. degrees in Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1994, 1996, and 1999, respectively. In 1999, she joined Hynix Semiconductor Ltd. (currently SK Hynix Semiconductor Ltd.) as a senior research engineer, where she was involved in the development of 0.115-μm, 0.09-μm DDRII DRAM technologies. Since 2005, she has been at Chungnam National University, Daejeon, Korea, as an Associate Professor with the Department of Electronics

Engineering. Her main research fields are flash memory, flexible display technology including fabrication, electrical analysis, and modeling.

In-Shik Han received the B.S. degree in semiconductor physics from Yeosu University, Yeosu, Korea, in 2003, and the M.S. and Ph.D degree in electronics engineering from Chungnam National University, Daejeon, Korea, in 2006 and 2010, respectively. Since 2010, he has been with MagnaChip Semiconductor Ltd. Chongju, Korea, as a senior research engineer, where he has been involved in developing mixed signal products of 0.18 CMOS technology. His research interests are in the areas of CMOS devices (including analog characteristics), low frequency noise, and wafer level reliability.

Yi-Sun Chung received the B.S. and M.S. degrees in metallurgy engineering from the Chonnam national university, Gwangju, Korea, in 1989, 1991, respectively. In 1996, he joined the Hyundai electronics, Ltd. (currently Hynix Semiconductor Ltd.), Icheon, Gyeonggi, Korea, where he has been involved in the process development of 0.5~0.18µm CMOS technologies. From 2001 to 2008, he developed 0.18µm RF technology and 0.13µm mixed signal technology in Hynix Semiconductor and Magnachip Semiconductor which was split from Hynix Semiconductor. Since 2009, he has been developing mixed signal products.

Jung-Hwan Lee received the B.S. degree from Hanyang University, Seoul, Korea, in 1983, the M.S. degree from the Korea Advanced Institute of Science and Technology, Seoul, Korea, in 1985, and the Ph.D. degree in chemical engineering from Drexel University, Philadelphia, PA, in 1996. From 1985 to 1988, he was a Device Researcher at Samsung Electronics, developing SRAM memories such as 16-, 64-, and 256-K SRAM. In 1989, he joined MagnaChip Semiconductor Ltd., Cheongjusi, Korea, a spinoff of Hynix Semiconductor Inc., in October 2004. He has been engaged in the development of 4-, 16-, and 64-M DRAM as a Device and Process Integration Engineer until 1996. Since 1996, he has been the Project Leader for the development of embedded memories such as embedded DRAM, Flash, and electrically erasable programmable ROM. His current research areas are high-voltage device, power device, Schottky diode, and 1 TRAM.

Hi-Deok Lee received a B.S., M.S., and Ph.D. degrees in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1990, 1992, and 1996, respectively. In 1993, he joined the LG Semicon Company, Ltd. (currently SK Hynix Semiconductor Ltd.), Chongju, Choongbuk, Korea, where he has been involved in the development of 0.35-µm, 0.25-µm, and 0.18-µm CMOS technologies, respectively. He was also responsible for the development of 0.15-µm and 0.13-µm CMOS technologies. Since 2001, he has been with Chungnam National University, Daejeon, Korea, with the Department of Electronics Engineering. From 2006 to 2008, he was with the University of Texas, Austin, and SEMATECH, Austin, as a Visiting Scholar. His research interests are in nanoscale CMOS technology and its reliability physics, silicide technology, and Test Element Group design. His research interests also include development of high performance analog and high voltage MOSFETs, and high efficient silicon solar cells. Dr. Lee is a member of the Institute of Electronics Engineers of Korea.