# Negative Differential Resistance Devices with Ultra-High Peak-to-Valley Current Ratio and Its Multiple Switching Characteristics

**Sunhae Shin, In Man Kang, and Kyung Rok Kim***

*Abstract*—**We propose a novel negative differential resistance (NDR) device with ultra-high peak-to-valley current ratio (PVCR) by combining *pn* junction diode with depletion mode nanowire (NW) transistor, which suppress the valley current with transistor off-leakage level. Band-to-band tunneling (BTBT) Esaki diode with degenerately doped *pn* junction can provide multiple switching behavior having multi-peak and valley currents. These multiple NDR characteristics can be controlled by doping concentration of tunnel diode and threshold voltage of NW transistor. By designing our NDR device, PVCR can be over $10^4$ at low operation voltage of 0.5 V in a single peak and valley current.**

*Index Terms*—**Negative differential resistance, peak-to-valley current ratio, band-to-band tunneling, multiple switching**

## I. INTRODUCTION

The negative differential resistance (NDR) devices are promising alternative device performing multifunctional operation. Since the first discover of NDR characteristics in Esaki tunnel diode with heavily doped *pn* junction based on germanium material [1], there have been in problem for practical applications owing to low peak-to-valley current ratio (PVCR) below 10 by the trap-assisted tunneling (TAT) current through forbidden band-gap [2, 3]. For the improvement of PVCR over 100, many research works have been reported focusing on the metal-oxide-semiconductor field-effect transistor (MOSFET) structure instead of simple tunnel diode. Enhanced surface generation in SiGe-based gated diode is exploited for PVCR of 300 around at 3 V [4, 5]. Other works show the PVCR of 1000 with breakdown mechanism of gated bipolar device in MOSFET structure [6, 7]. Recently, NDR device using both enhancement and depletion mode of MOSFETs, has been reported with high PVCR of $10^7$ at 1.6 V [8]. These previous reports based on MOSFET operation and structure with terminal reconfigurations demonstrated PVCR at relatively high operation voltage over 1.5 or 2.0 V [4-8]. For higher PVCR over $10^4$ at lower operation voltage below 1 V, simple *pn* diode combined with silicon (Si) nanowire (NW) structure has been presented with ultra-high PVCR of $10^8$ at low voltage of 1.0 V in our previous work [9]. Moreover, multiple NDR devices with multi-peak and valley below 1 V have not been reported yet.

In this paper, we propose novel NDR device with ultra-high PVCR having multi-peak and valley current based on *pn* tunnel junction and Si NW transistor. In section II, device operation principle and multiple switching characteristics will be presented. In section III, effects of device design parameters on multiple peaks and valleys will be investigated. In addition, single NDR characteristics with ultra-high PVCR over $10^4$ at low supply voltage of 0.5 V will be discussed.

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## II. DEVICE OPERATION PRINCIPLE AND MULTIPLE NDRS

Figs. 1(a) and (b) show a three-dimensional (3-D) bird's eye view and two-dimensional (2-D) cross-sectional schematic of the proposed NDR device, respectively, which is based on the simple combination of *pn* tunnel diode and *p*-type Si NW transistor. The circuit symbol of this NDR device can be represented as in Fig. 1(c). The *pn* tunnel diode was designed with both *n*-type and *p*-type doping concentrations of $3\times10^{20}$ $cm^{-3}$ and tunnel junction width of 10 nm. The NW transistor had channel radius ($R_{ch}$) of 5 nm, gate oxide thickness ($T_{ox}$) of 3.5 nm, and *p*-type doping concentration of $2\times10^{19}$ $cm^{-3}$.

The simulation was performed by using *Sentaurus*™ 3-D TCAD device simulator [10]. In order to describe band-to-band tunneling (BTBT) mechanism in forward bias of tunnel diode, our numerical BTBT model has been incorporated [11]. For the leakage current behaviors through a forbidden energy band-gap, conventional field-dependent TAT model is used [12]. Basic operation principle of our NDR device with ultra-high PVCR is that NW transistor can completely suppress the valley current creating NDR region. Single or multiple NDR curves can be observed by adjusting the threshold voltage of NW transistor.

Fig. 2 shows the simulation results of multiple NDR characteristics with multi- peak and valley currents

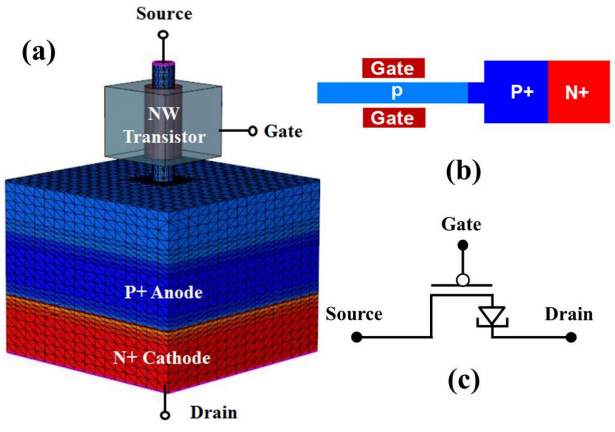


**Fig. 1.** Device schematics and circuit symbol of proposed NDR device combined *pn* tunnel junction with *p*-type Si NW transistor (a) 3-D bird's eye view, (b) 2-D cross-sectional device schematic, (c) circuit symbol. Si NW transistor controls the carrier (hole) injection from source to diode.

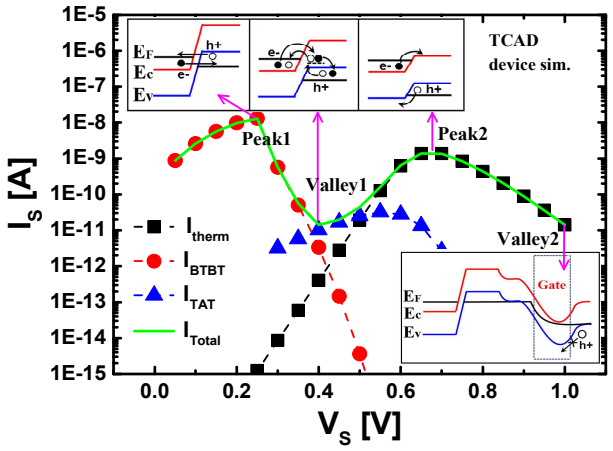


**Fig. 2.** Simulation results of multiple NDR characteristics with the respective current component and the corresponding energy band diagram: Peak1, valley1, and peak2 is caused by normal Esaki tunnel diode behaviors such as BTBT, TAT, and thermionic injection as shown in upper energy band diagrams. Valley2 is suppressed by the increase of potential barrier as shown in lower energy band diagram using faster sweep of gate bias from 0 to 1.5 V than that of source bias from 0 to 1 V.

and/or voltages referred to peak1, valley1, peak2, and valley2. As in the insets of Fig. 2, the corresponding energy band diagrams with each current component illustrate the operation principle of the multiple NDRs. At low gate bias (on-state) of NW transistor, source voltage can be transferred to *p*-region of tunnel diode. Then, the peak1 and valley1 are caused by BTBT and TAT current of tunnel junction, respectively, as a typical Esaki tunnel diode behavior. After thermal diode current over the barrier of forward-biased *pn* junction becomes dominant, the second peak2 and valley2 can be observed by the suppression of diode current owing to increase the gate potential barrier of NW transistor when the gate bias increases faster than source bias.

## III. RESULTS AND DISCUSSION

The multiple NDR characteristics can be controlled by design parameters such as doping concentration, junction area of diode, and threshold voltage of NW transistor. Figs. 3(a) and (b) show the effects of doping concentration and junction area on the NDR curves, respectively, based on 3-D device simulation. When doping concentrations of *pn* tunnel junction increase, BTBT current and voltage of peak1 increase by higher potential difference in tunnel junction diode. Valley1

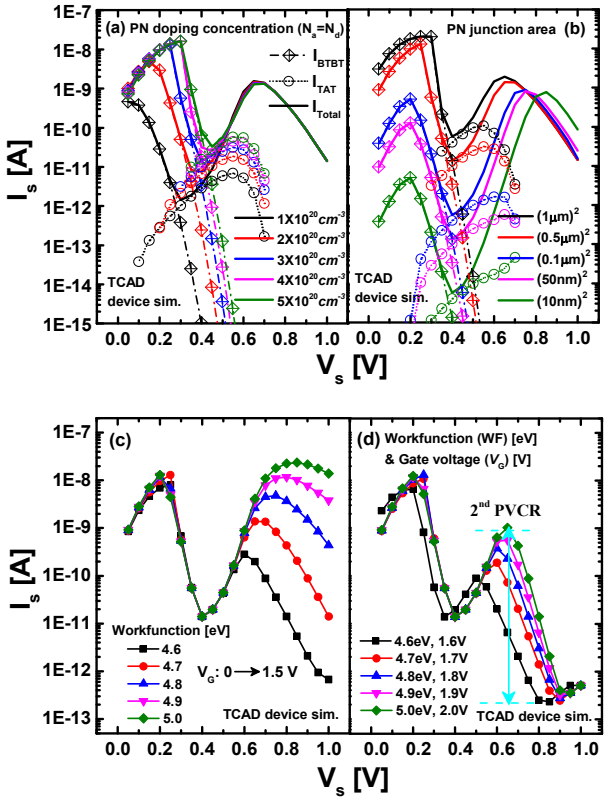


**Fig. 3.** The simulated $I_s$-$V_s$ characteristics with various design parameters (a) *pn* doping concentrations, (b) *pn* junction area of tunnel diode, (c) gate workfunction (WF), (d) both gate workfunction (WF) and bias ($V_G$) of Si NW transistor. Tunnel diode can control the current and voltage levels of peak1 and valley1 and NW transistor can control those of peak2 and valley2.

currents which are determined by TAT currents also increase by field enhancement according to the increase of doping level from $1\times10^{20}$ to $5\times10^{20}$ $cm^{-3}$, while thermal diode currents for peak2 remain constant in the degenerate doping range (Fig. 3(a)). When the junction area increases, BTBT (peak1), TAT (valley1), and thermal diode (peak2) currents increase as expected (Fig. 3(b)). On the other hand, current and voltage levels of valley2 are not affected by junction area and doping concentration since high gate bias (off-state) of NW transistor suppresses the carrier injection into diode region.

Figs. 3(c) and (d) represent that NW transistor can control the peak2 and valley2 with the threshold voltage ($V_{th}$), which can be designed by using the various gate workfunction, radius, and doping concentration of NW transistors [13]. In Fig. 3(c), when the gate workfunction increases, owing to $V_{th}$ shifts in the positive direction of

**Table 1.** 2nd peak and 2nd PVCR with various supply voltages ($V_G$) of inverter and workfunctions (WF) of NW transistor based on device simulation results

| $V_G$ [V] | WF [eV] | 2nd peak [A] | 2nd PVCR |
|---|---|---|---|
| 1.6 | 4.6 | $8.9\times10^{-11}$ | 380 |
| 1.7 | 4.7 | $1.9\times10^{-10}$ | 770 |
| 1.8 | 4.8 | $3.8\times10^{-10}$ | 1400 |
| 1.9 | 4.9 | $5.6\times10^{-10}$ | 1700 |
| 2.0 | 5.0 | $1.0\times10^{-9}$ | 2900 |

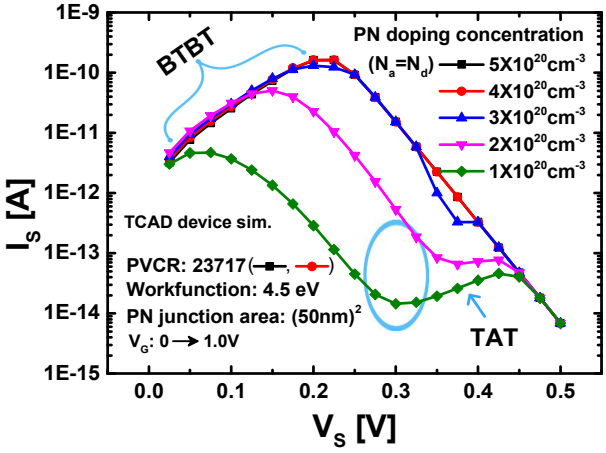


**Fig. 4.** Simulation results of single NDR characteristics with various doping concentrations of *pn* junction from $N_a$=$N_d$= $1\times10^{20}$ to $5\times10^{20}$ $cm^{-3}$ by using gate workfunction with WF= 4.5 eV of Si NW transistor. Single NDR curve with ultra-high PVCR over $10^4$ can be obtained at low supply voltage of 0.5 V.

*p*-type Si NW transistor. According to the positive $V_{th}$ shift, there is a trade-off between operation voltage of gate ($V_G$) and PVCR for second peak and valley. By applying high gate voltage for high peak2 current, higher (2nd) PVCR can be obtained as shown in Fig. 3(d) and Table 1. Therefore, we can design the multiple switching NDR devices with ultra-high PVCR by using device parameters of *pn* junction diode and NW transistor.

Moreover, as shown in simulated results of Fig. 4, single NDR curves can be obtained with ultra-high PVCR over $10^4$ at low supply voltage of 0.5 V by the suppression of valley current from turning-off NW transistor ($V_G$ from 0 to 1 V) with lower gate workfunction (WF= 4.5 eV). It should be noted that single peaks result from BTBT mechanism of tunnel diode since peak current levels can be enhanced by the increase of doping concentration. Higher PVCR over $10^5$ can be expected only by considering peak current enhancement (e.g. lower band-gap materials) since the valley current can be always suppressed as off-current of

NW transistor at lower operation voltage below 0.5 V.

## V. CONCLUSIONS

We proposed the novel NDR device with ultra-high PVCR having multiple switching characteristics based on *pn* tunnel diode and NW transistor for low-power and multi-functionality. Multiple NDR characteristics have been demonstrated with the analysis of each current component according to the device design parameters. Ultra-high PVCR over $10^4$ at low supply voltage of 0.5 V can be obtained by the successful suppression of valley current through the depletion of NW transistor.

## ACKNOWLEDGMENTS

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