Some Device Design Considerations to Enhance the Performance of DG-MOSFETs

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When subjected to a change in dimensions, the device performance decreases. Multi-gate SOI devices, viz. the Double Gate MOSFET (DG-MOSFET), are expected to make inroads into integrated circuit applications previously dominated exclusively by planar MOSFETs. The primary focus of attention is how channel engineering (i.e. Graded Channel (GC)) and gate engineering (i.e. Dual Insulator (DI)) as gate oxide) creates an effect on the device performance, specifically, leakage current (I_{off}), on current (I_{on}), and DIBL. This study examines the performance of the devices, by virtue of a simulation analysis, in conjunction with N-channel DG-MOSFETs. The important parameters for improvement in circuit speed and power consumption are discussed. From the analysis, DG-DI MOSFET is the most suitable candidate for high speed switching application, simultaneously providing better performance as an amplifier.

Keywords: DG, DG -DI and DG -GC-MOSFETs, DIBL, Leakage currents, Transconductance (g_m), High-k

1. INTRODUCTION

The improvement of device performance is a vital goal of the microelectronics community, and this can be done by scaling down the device dimensions [1]. However, as the technology scaling enters into the nanometer regime, the device exhibits various serious problems, such as low on current, increased leakage current, low reliability, and increase in manufacturing cost. To overcome these problems, various innovations in device structures have been researched and introduced. This has resulted in different structures with gate engineering, such as the Dual Material Gate (DM), Dual Insulator (DI) Gate, Gate Stack (GS), and channel engineering as graded channel (GC) [2,3]. Previously, Cheng et al. [4] have shown the impact of high-k gate dielectrics on the device short channel parameters. They have studied various short channel parameters, by taking gate stack engineering (i.e. one thick layer of high-k dielectric over one thin layer of low-k dielectric). Colinge [5] discussed the drive current

and short channel effects (SCEs) for a SOI Multiple Gate MOS-FET (MuGFET). From the simulation results, he concluded that SOI MuGFETs offer higher drive current, as well as better immunization to SCEs, than the conventional MOSFETs. Subramanian [6] presented a review paper on MuGFETs. He discussed the physics and technology of these devices, and their advantages and disadvantages. In Sharma et al. [3], different gate engineering and channel engineering under DG-MOSFET technology are discussed, and also a comparison of various parameters among DG-DM, DG-GC, DG-GS-DM and DG-GS-GC is highlighted. Aouaj et al. [7] and Bendib et al. [8] discussed the concept of GC and GS on the double gate platform. In this work, we presented three types of device structures, DG-FD, DG-GC and DG-DI, by keeping speed in mind, as well as power consumption. The important parameters, like sub threshold swing (SS), drain Induced Barrier Lowering (DIBL), on current (I_{on}), off current (I_{off}), transconductance (g_m), output conductance (g_d) and Gain (g_m/g_d) are extracted, and a comparison is made among these three devices.

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2. EXPERIMENTS

2.1 Device structures

The schematic structures of DG-FD, DG-GC, and DG-DI MOS-

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FETs are shown in Fig. 1. In all structures, the channel length (L) is fixed at 40 nm, as well as the Source/Drain length (L_S/L_D). The silicon thickness (t_{Si}) is 10nm, and a uniform density of ND as 10^{20} cm^{-3} is considered. The channel is doped (N_A) of 10^{18} cm^{-3} in DG-FD and DG-DI. Whereas for DG-GC, the high-low profile of doping is taken as 10^{18} cm^{-3} and 10^{17} cm^{-3}. The oxide thickness t_{ox} = 2 nm, for all structures. In all structures a low-k spacer (Si_3N_4) is considered, for improvement of the device performance. The work function for the gate materials is assumed to be 4.8 ev.

2.2 Simulation

To obtain accuracy of simulation, the mobility degradation that occurs inside inversion layers is accounted for. The degradation normally occurs as a result of higher surface scattering near the semiconductor-to-insulator interface. So in the simulation, the inversion-layer Lombardi constant voltage and temperature (CVT) mobility model is activated, which takes into account the effect of transverse fields, along with doping and temperature dependent parts of the mobility. These components are combined using Matthiessen's rule, as follows:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{Sr}^{-1} \qquad (1)$$

μ_{AC} is the surface mobility by scattering with acoustic phonons.

μ_{Sr} is the surface roughness factor.

μ_b is the mobility by scattering with optical inter valley phonons.

The Shockley-Read-Hall (SRH) model simulates the leakage currents that exist due to thermal generation. Auger recombination models for minority carrier recombination have been used. In SOI technology, the potential in the channel is commonly referred to as "floating". Furthermore, we chose Gummel's method (or the decoupled method), which performs Gummel iteration for the Newton solution [9].

3. RESULTS AND DISCUSSION

In Figs. 2 & 3, I_{DS}-V_{GS} transfer characteristics are shown on a linear scale and log scale (Inset Figures) for three different device structures, and are compared for V_{DS} = 10 mV and 1.2 V. The DG-DI MOSFET provides a larger drain current, as compared to the other two MOSFETs. This is because of the inclusion of higher dielectric material in the gate oxide, according to the relationship I_D α C_{ox} α $ε_{ox}$.

The Sub threshold Slope (SS) is the major parameter for calculating the off state current. Furthermore, SS is calculated as:

$$SS(mV / dec) = \frac{\partial V_{GS}}{\partial (\log I_D)} \qquad (2)$$

where, the logarithm is in base 10, I_D is the drain current, and V_{GS} is the gate voltage. The SS is always expressed in millivolts per decade. The typical value for the SS of Multigate MOSFET is 60 mV /decade, i.e. a 60 mV change in gate voltage brings about a tenfold change in drain current. The SS is extracted by calculating the inverse of maximum slope of V_{GS} versus log (I_D) curve, as shown in TABLE I. From the table, it is clear that the SS value is lower for DG-DI MOSFET, and again from equation (2)[10], the off state current is directly related to the SS. So, the off state current is also minimum for the DG-DI MOSFET, as compared to
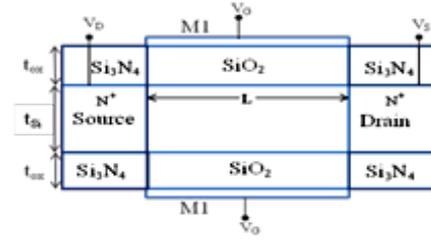

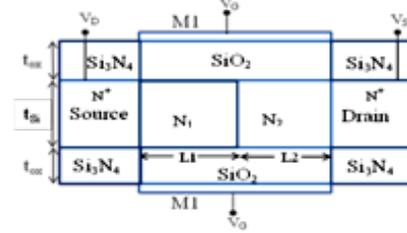Fig. 1(a). Schematic structure of DG-FD.
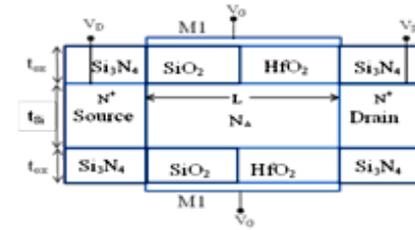

Fig. 1(b). Schematic structure of DG-GC.
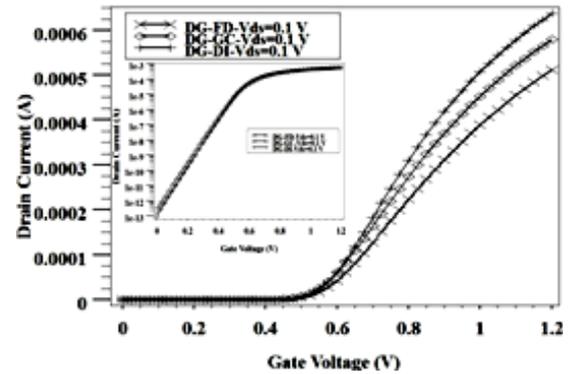

Fig. 1(c). Schematic structure of DG-DI.

Fig. 2. The drain current (I_D) as a function of the gate voltage (V_{GS}), on linear and log scales (inset) at V_{DS} = 10 mv, for the three structures.

the other MOSFETs, and as shown in Fig. 5.

$$I_{off} (nA) = 100 \bullet \frac{W}{L} \bullet 10^{-V_T / SS} \qquad (3)$$

Again, the off state current (I_{off}) is extracted, by calculating the drain current (I_D) at V_{GS} = 0 and V_{DS} = V_{DD}. The I_{off} for all the three device structures is summarized in Table 3. It is important to keep I_{off} very small, in order to minimize the static power dissipation when the device is in off state.
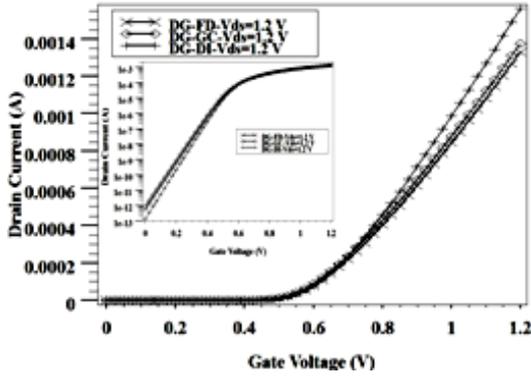
Fig 3. The drain current (I_D) as a function of the gate voltage (V_{GS}), on linear and log scales (inset) at V_{DS} = 1.2 V, for the three structures.

Fig. 4. Variation of the transconductance (g_m) with V_{GS} for the three different structures, at V_{DS} = 10 mV (inset figure) and 1.2 V.

$$I_{DS}(nA) = 100 \bullet \frac{W}{L} \bullet e^{q(V_{GS}-V_T)/\eta kT} \qquad (4)$$

where, W : width of the channel, L : Channel Length, Q : Electronic Charge, V_{GS} : Gate to Source Voltage, V_T : Threshold Voltage, K: Boltzman Constant, T: Temperature in Kelvin, SS: Sub threshold Slope, and η : Body factor, which is proportional to the change in gate voltage with a change in channel potential, i.e.

$$\eta = \frac{\partial V_{GS}}{\partial \phi_S} \qquad (5)$$

From equation (4)[10], the threshold voltage (V_{th}) is also a very important parameter for higher on state current, which improves the circuit speed. The V_{th} is extracted by calculating the maximum slope of the I_D-V_{GS} curve, finding the intercept with the x-axis, and then subtracting half of the applied drain bias, as given in Tables 1 and 2, for drain bias of 0.1 V & 1.2 V. The DG-GC shows a lower V_{th}, because of the high-low doping profile taken for the Graded Channel, and according to equation (6)[10], V_{th} is directly related to the doping profile. However, the doping profile being the same for DG-DI and DG-FD MOSFETs, the DG-DI MOSFET exhibits a lower V_{th} than DG-FD MOSFET, which enables its speed of operation.

$$V_t = V_{fb} + \phi_{st} + \frac{\sqrt{qN_{sub}2\varepsilon_s\phi_{st}}}{C_{ox}} \qquad (6)$$

The g_m versus V_{GS} characteristics are compared for all the three device structures in Fig. 4. The DG-DI MOSFET shows a higher value of transconductance, when compared with the other two MOSFETs. As we know:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \qquad (7)$$

So, the value of g_m is extracted by taking the derivative of the I_D-V_{GS} curve, the values of which are summarized in Table 1 and Table 2. From the extracted data, it can be examined that the DG-DI MOSFET gives a higher g_m value, and also a higher drain current. According to the relation in equation 7, g_m is directly related to the drain current (I_D). As far as analog circuits are concerned, g_m is the most important parameter, because the value of g_m is
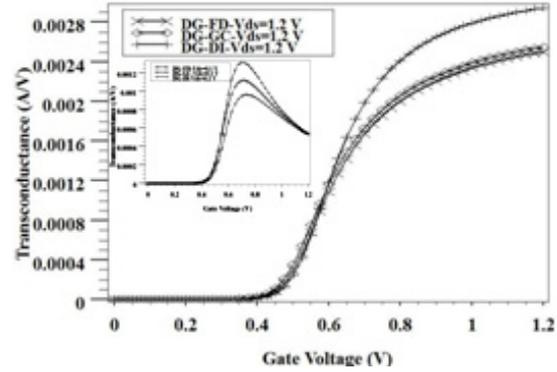
directly related to the gain of the device (g_m/g_d).

Figure 5 shows the output characteristics (I_{DS}-V_{DS}) and output conductance (inset figure) for various DG configurations, at a gate voltage of 1.2 V. The DG-DI MOSFET gives an almost flat characteristic in saturation, and also exhibits high drain current, in comparison with the other DG configurations. In order to demonstrate the SCEs, the simulated output conductance is given in the inset figure. In the saturation region, the DG-DI MOSFET exhibits the lowest value of g_d, but it exhibits the highest value of g_d in the linear region. The Ion/I_{off} ratio and DIBL are given in Table 3 for all of the three device structures. The value of DIBL is calculated as per the relation given in equation 8.

$$DIBL = \frac{\Delta V_{th}}{\Delta V_d} \qquad (8)$$

The DIBL calculation is taken for V_{th} at V_D = 0.1 V and V_D = 1.2 V. Both DG-GC and DG-DI MOSFETs give nearly equal values of DIBL, which is better, as compared to the DG-FD MOSFET. This is because of the high-low doping profile in GC, and the inclusion of high-k dielectric material in the DI structure. The I_{on}/I_{off} ratio is much higher for the DG-DI MOSFET than for the other two structures, which is a very important parameter for both speed and standby power consumption. For circuit speed application, I_{on} should be more, and for low power consumption application, I_{off} should be less. So, there is always a tradeoff between I_{off} and I_{on}.

The leakage current (I_{off}) is calculated by considering V_{GS} = 0 for all the device structures, and is plotted in Fig. 6. It can be noticed that the DI architecture exhibits a very low leakage current, in comparison with the other two architectures. This is because the

Table 1. Extracted parameters at V_D = 0.1 V.

plasma	V_t (V)	SS (mV/dec)	g_m (mA/V)	I_{on} (mA/um)
DG-FD	0.518	65.177	0.965	0.512
DG-GC	0.504	65.472	1.121	0.579
DG-DI	0.511	61.855	1.316	0.637

Table 2. Extracted parameters at V_D = 1.2 V.

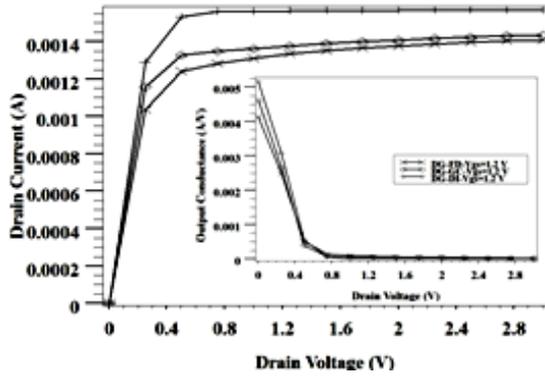| plasma	V_t (V)	SS (mV/dec)	g_m (mA/V)	I_{on} (mA/um)
DG-FD	0.067	65.701	2.493	1.329
DG-GC	0.060	66.307	2.544	1.374
DG-DI	0.068	62.014	2.938	1.562

Fig. 5. Variation of the drain current (I_D) and output conductance (g_d) (Inset) with V_{DS}, for the three different structures, at V_{GS} = 1.2 V.
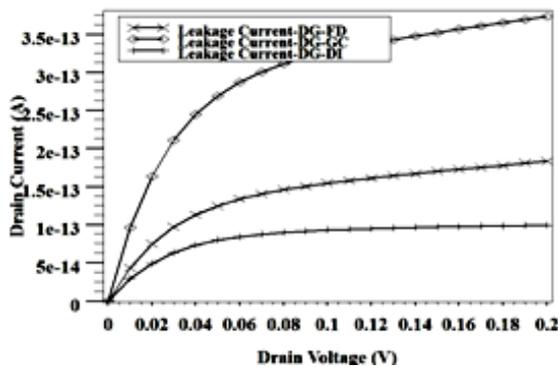

Fig. 6. I_D as a function of V_{DS} for the different structures, at V_{GS} = 0 V.

physical thickness of the gate dielectric is more, due to the high-k dielectric material used in the DI structure. On the other hand, from equation 3, I_{off} is related in the ratio of V_t and SS. The DG-DI architecture shows a higher value for the ratio of V_t and SS, as compared to the others, according to Table 1. Hence, it gives a lower I_{off}, due to the exponential decaying nature of equation 3.

4. CONCLUSIONS

According to the International Technology Roadmap for Semiconductors, the SOI MOSFETs allow reduction of short channel effects. In order to study these new structures, numerical simulations are carried out. This work gives a close comparison of various design engineering, namely the FD, GC and DI of the DG-SOI. In this paper, the performance comparison for all the structures is limited to DC analysis only. Furthermore, the AC analysis can be done by investigating the analog and RF performance of the devices. The DG-DI MOSFET shows a significant

Table 3. Extracted and calculated parameters.

Parameters	DG-FD	DG-GC	DG-DI
I_{off} (pA)	For V_g = 0 V, V_d = 0 V to 3 V		
	0.184	0.374	0.099
I_{on}/I_{off}	For V_g = 1.2 V, V_d = 1.2 V		
	7.2E + 09	3.7E + 09	1.6E + 10
DIBL (V/V)	For V_g = 1.2 V, V_d = 0.1 V and 1.2 V		
	0.410	0.403	0.403

improvement in device characteristics, such as on current (I_{on}), off current (I_{off}), g_m, SS and DIBL. Hence, DG-DI MOSFET is a suitable candidate for both high speed and low power consumption application. This paper verifies all the relations, through extractive data obtained from the simulation results.

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