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Fabrication and Challenges of Cu-to-Cu Wafer Bonding

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Abstract: The demand for 3D wafer level integration has been increasing significantly. Although many technical challenges of wafer stacking are still remaining, wafer stacking is a key technology for 3D integration due to a high volume manufacturing, smaller package size, low cost, and no need for known good die. Among several new process techniques Cu-to-Cu wafer bonding is the key process to be optimized for the high density and high performance IC manufacturing. In this study two main challenges for Cu-to-Cu wafer bonding were evaluated: misalignment and bond quality of bonded wafers. It is demonstrated that the misalignment in a bonded wafer was mainly due to a physical movement of spacer removal step and the bond quality was significantly dependent on Cu bump dishing and oxide erosion by Cu CMP.

Keywords: Wafer bonding, Misalignment, Cu bonding, CMP

1. Introduction

3D wafer level integration has been a key technology to microelectronic industries and it is the best for high density and high performance device applications.[1-4] Although many technical challenges of wafer stacking are still remaining, wafer stacking is a key technology for 3D integration compared to die-to-die, die-to-wafer, or package-to-package due to high volume manufacturing, smaller package size, and no need for known good die. Especially for the high density and high performance, the wafer stacking with a metallic bonding is necessary and Cu-to-Cu wafer bonding is without doubt a key process to be developed. The advantages of Cu as a bonding material are a mainstream CMOS material, low resistivity ($\rho = 1.7\ \mu\Omega$cm), high thermal conductivity ($K = 400$ W/mK), good resistance to electromigration, and no brittle intermetallic formation. Many studies for Cu-to-Cu wafer bonding have been explored by many researchers.[5-11] However, wafer warpage, coefficient of thermal expansion (CTE) mismatch with other layers in a stack, and inherent Cu process issues such as Cu oxidation, bonding surface uniformity, and Cu CMP (chemical mechanical polishing) have not been discussed in detail and it is still remained as the challenges to be resolved for Cu-to-Cu wafer bonding.

In this study the two main challenges for Cu-to-Cu wafer bonding are evaluated: misalignment and Cu bonding quality. Some report[12] stated that bond tool and wafer thinning process can introduce a misalignment of bonded wafers. According to our previous study[6], it was found that a thin film deposited wafer had a concave-up warpage and a maximum wafer bow became severe as the number of wafer stacks increased. Therefore, wafer warpage might contribute a misalignment of bonded wafer and it might be intensified as the number of wafer stacks increases. Also, the degree of planarization of Cu surface is very important for the best bond quality. Traditionally Cu CMP is not used in electronic packaging field due to a high cost, so other planarization method like a diamond bit cutting has been reported.[8] However, high density and high performance devices still require Cu CMP.

2. Experimental Procedure

The Cu bump patterned wafers were fabricated on 200 mm Si wafer of approximately 720 μm thick. Ti/Cu barrier and seed layers of 0.15 μm thick were deposited on a Si wafer by sputtering and then approximately 1.2 μm thick Cu was electroplated followed by Cu CMP. The process conditions of Cu CMP are summarized in Fig. 6(d).

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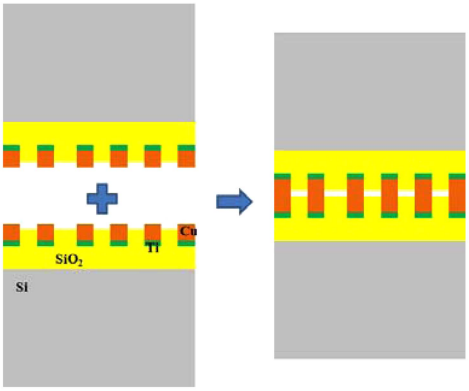
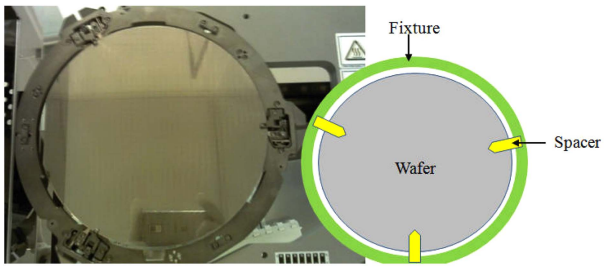


(a) Sample structure for Cu-to-Cu wafer bonding



(b) Spacer positions

Fig. 1. Schematics of Cu-to-Cu wafer bonding.

Then a thermo-compression wafer bonding was performed for wafer stacking and the schematic diagram of wafer stack is shown in Fig. 1. A pre-cleaning of Cu bump surface prior to a wafer bonding was done for 1 minute by H_2SO_4:DI (1:100) solution in order to remove any surface contamination and native oxide. Two Cu bump patterned wafers were aligned using Suss Microtec aligner (MA8-L) and then Cu-to-Cu wafer bonding was performed at 415°C under pressure of 8900mbar for 1 hour using Suss Microtec bonder (SB8e). A forming gas treatment was also performed just before bonding in a bond chamber to clean Cu bump surface. The aligning and bonding process steps are shown step by step in Fig. 2. A bond quality after Cu-to-Cu wafer bonding was investigated by focused ion beam (FIB), scanning electron microscope (SEM) and scanning acoustic microscope (SAM). To evaluate the degree of misalignment, glass-to-Si wafer pairs were used instead of Si wafer-to-Si wafer pairs. A misalignment after clamping (i.e. before bonding) and after bonding was inspected using a microscope.

3. Results and Discussion

In 3D wafer level packaging, wafer-to-wafer alignment is very important especially for narrow pitched high density devices, because it impacts both device performance and reliability of stacked wafers. The accuracy of alignment can

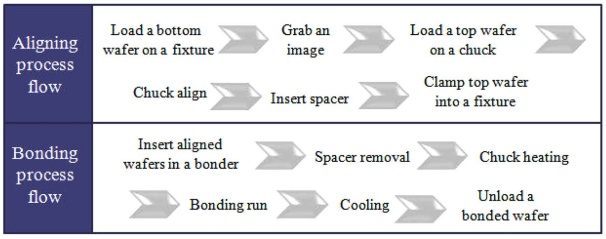
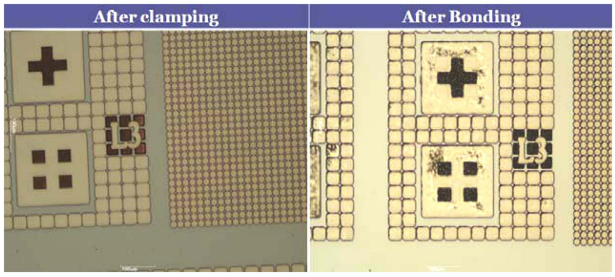
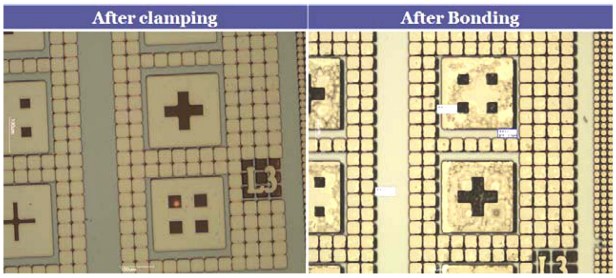


Fig. 2. Aligning and bonding process flow sequence.



(a) Left side of a bonded wafer



(b) Right sde of a bonded wafer

Fig. 3. Misalignment analysis with aspacer: after clamping (i.e. before bonding) vs. after bonding.

be dependent on both equipment (aligner and bonder) and process. In this study, glass-to-Si wafer pairs were prepared and inspected after a clamping step to verify any pre-bonding misalignment and after a bonding step to verify any post-bonding misalignment. Also, the misalignment with and without spacers were tested, because a spacer removal step is the only physical movement during a bonding process sequence.

Firstly the misalignment after a clamping step (i.e. after finishing all aligning steps) and after a bonding step is shown in Fig. 3. It is clearly shown that there was almost no misalignment during an aligning process sequence including inserting a spacer and loading aligned two wafers from an aligner to a bonder. But the misalignment after a bonding process sequence was markedly observed about 1 μm in the left side and about 6-7 μm in the right side of bonded wafer. The left side of bonded wafer had much better alignment accuracy compared to the right side of bonded wafer. The possible cause for this non-symmetric misalignment is supposedly an uneven spacer removal during a bonding

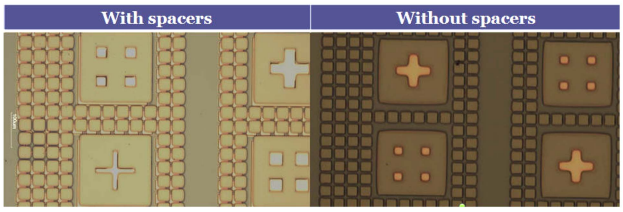


Fig. 4. Misalignment analysis after bonding: with spacers vs. without spacers.

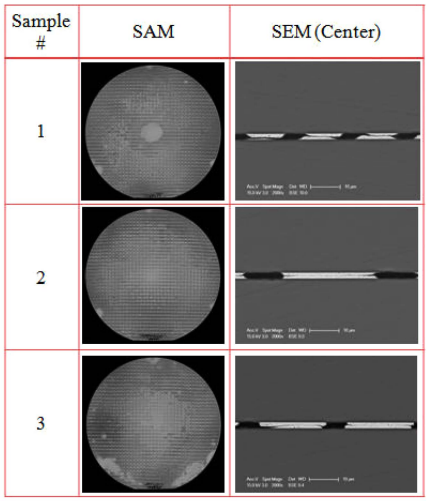
process, because this step is the only physical movement involved with wafers. It is suggested that the misalignment of bonded wafer was certainly more impacted by a bonding process than an aligning process. Secondly the effect of spacer removal in a bonding process was evaluated and the results are shown in Fig. 4. There was almost no misalignment after bonding without spacers, but the misalignment was clearly observed after bonding with spacers. It seemed that a physical movement of spacer removal from two aligned wafers was the main cause for a misalignment because a wafer has had a great chance to move when three spacers were removed.

To evaluate a bond quality the annealing after bonding was investigated in this study. As shown in Fig. 5(a) three cases were tested such as no annealing, annealing in N_2, and vaccum annealing. Since Cu oxidize so readily N_2 gas or vaccum was used to reduce oxygen availability during annealing. In these cases wafer bonding was done with spacers to make forming gas treatment be effective. The SAM images of bonded wafers are shown in Fig. 5(b) and indicated that all three cases were not bonded well since the color image of SAM appeared as an uneven gray color instead of a dark gray or black color which indicates a very weak bond quality. The sample #1 (no annealing) had a clearly unbonded area at the center, and the sample #3 (vaccum annealing) had an unbonded area at the bottom edge of bonded wafer. These unbonded interfaces are shown in the SEM images in Fig. 5(b). These poor bond quality seemed to be nothing to do with annealing conditions nor with a bonding process itself in this study, rather it was likely affected by a bonding layer uniformity. Although it was unable to evaluate the annealing effects on bonding due to the unbonded interface, it showed suggestively how important the planarity of bonding surface was for a good bond quality.

As shown in Fig. 6(a) Cu bump had Cu dishing problem due to Cu CMP process. For example, a structure of 10 μm metal width with 30 μm space had about 400Å Cu dishing and about 500Å oxide erosion as shown in Fig. 6(b) and (c). Due to Cu bump dishing by Cu CMP, Cu bumps were locally bonded at the edge of each bump causing a very weak bond interface. The previous study by Park *et al.*[13, 14] reported that HF and H_2SO_4 wet treatment of Cu bonding

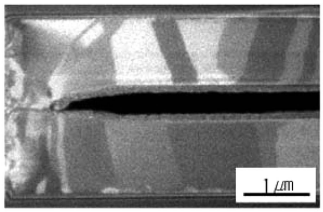
Sample #	Top wafer (Run date)	Bottom wafer (Run date)	Bonding Conditions		
			Pre-forming gas treatment	Bonding	Post-annealing
1	$Si/SiO_2/Ti/Cu$	$Si/SiO_2/Ti/Cu$	1 time	P: 8900mbar T: 415°C time: 1 hr	No
2	$Si/SiO_2/Ti/Cu$	$Si/SiO_2/Ti/Cu$			N_2, 450°C, 1hr
3	$Si/SiO_2/Ti/Cu$	$Si/SiO_2/Ti/Cu$			Vacuum, 450°C, 1hr

(a) Sample process conditions

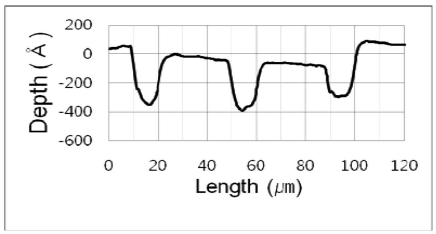


(b) SAM and SEM(center die) images of bonding interface

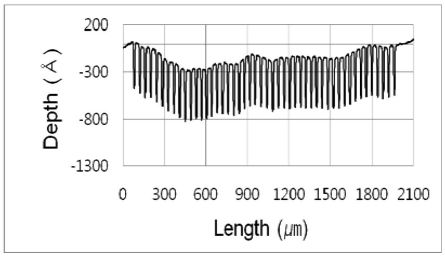
Fig. 5. Bonding inteface analysis after Cu-to-Cu wafer bonding.



(a) FIB image after Cu-to-Cu wafer bonding



(b) Cu dishing after Cu CMP (Line width: 10 μm, Space: 30 μm)



(c) Oxide erosion after Cu CMP (Line width: 10 μm, Space: 30 μm)

Polishing Parameters	Velocity	Platen: 73 rpm
		Head: 67 rpm
	Pressure	Wafer: 0.176 kgf/cm²
		R-Ring: 0.211 kgf/cm²
	Slurry Flow Rate	200 ml/min
Removal Rate		Approximately 6000 Å/min

(d) Cu CMP process conditions

Fig. 6. Cu bump dishing and oxide erosion after Cu CMP.

surface or $Ar+H_2$ plasma treatment before Cu-to-Cu bonding increased the interfacial adhesion energy and improved Cu-to-Cu bond quality. To improve Cu-to-Cu bonding quality the any oxide removal and contamination-free surface of Cu bonding layer are needed, but the minimization of both Cu bump dishing and oxide erosion is more important and essential to have a reliable and manufacturable wafer bonding.

4. Conclusions

In this study both misalignment and bond quality of Cu-to-Cu wafer bonding were investigated. Cu bumps were fabricated on a Si wafer and Cu bump patterned wafers were bonded by a thermo-compression bonding. A wet chemical treatment on Cu surface before bonding was done and a forming gas treatment was also performed prior to a bonding process. It has been demonstrated that the controlling of Cu dishing and oxide erosion by Cu CMP was significant to improve Cu-to-Cu wafer bonding quality in addition to pre-surface treatments. Any physical movement step in aligning and bonding processes may affect the accuracy of alignment significantly.

Acknowledgments

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