An Optimized Stacked Driver for Synchronous Buck Converter

Dong Keon Lee*, Sung-Chul Lee, and Hang-Geun Jeong***

Abstract—**Half-rail stacked drivers are used to reduce power consumption of the drivers for synchronous buck converters. In this paper, the stacked driver is optimized by matching the average charging and discharging currents used by high-side and low-side drivers. By matching the two currents, the average intermediate bias voltage can remain constant without the aid of the voltage regulator as long as the voltage ripple stays within the window defined by the hysteresis of the regulator. Thus the optimized driver in this paper can minimize the power consumption in the regulator. The current matching requirement yields the value for the intermediate bias voltage, which deviates from the half-rail voltage. Furthermore the required capacitance is also reduced in this design due to decreased charging current, which results in significantly reduced die area. The detailed analysis and design of the stacked driver is verified through simulations done using 5V MOSFET parameters of a typical 0.35- μm CMOS process. The difference in power loss between the conventional half-rail driver and the proposed driver is less than 1%. But the conventional half-rail driver has excess charge stored in the capacitor, which will be dissipated in the regulator unless reused by an external circuit. Due to the reduction in the required capacitance, the estimated saving in chip area is approximately 18.5% compared to the half-rail driver.**

Index Terms—**Synchronous, stacked, driver, buck, converter, low voltage**

I. INTRODUCTION

Recently, a synchronous rectifier buck converter (SRBC) is very popular for low-power buck converters. In the SRBC, a MOSFET is used instead of the diode, which causes high conduction loss. So the SRBC is a good solution for mobile devices to provide high efficiency and small size [1, 2].

One disadvantage of the SRBC is that a driver is required to turn on and off the MOSFET. Due to fairly large gate capacitance of the MOSFET, the power consumption of the driver becomes a significant portion of the total power consumption of the SRBC. So various techniques have been researched to reduce the switching power loss. Optimum width control (OWC) and pulse frequency modulation (PFM) techniques are representative of them [3, 4]. Using these techniques, the converter efficiency can be improved under light load condition. But, its efficiency is not increased under heavy load condition, because these techniques cannot be applied. Therefore a new technique must be developed to improve the maximum efficiency.

Fig. 1 shows the conventional power stage circuit of the SRBC. It consists of two switches and their drivers. The drivers swing rail-to-rail, which means the power loss of the driver is not optimized. The power loss of the driver can be reduced by decreasing the voltage swing of the driver. In [5], the voltage swings for both NMOS and PMOS gate drivers were optimized to minimize the power loss. It is implicitly assumed in [5] that two additional power supplies, one for the ground of the

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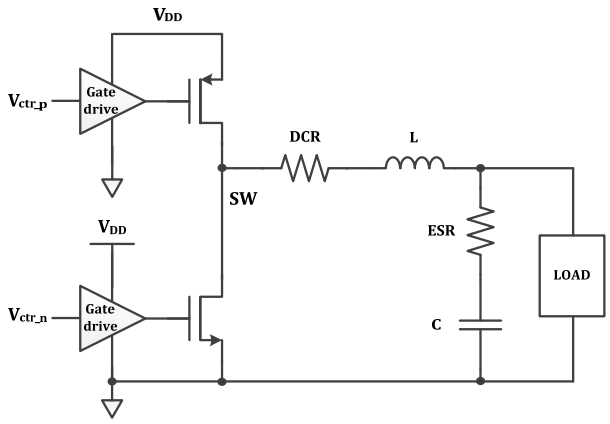


Fig. 1. Conventional power stage circuit of SRBC.

PMOS gate driver and the other for the power supply of the NMOS gate driver, are used. Otherwise the expressions in [5] for the energy dissipated in the PMOS and NMOS drivers would become invalid. If a single power supply were used with internal linear voltage regulators, the optimum swing would turn out to be full-swing, resulting in no power saving. Because, in this case, the dissipated energy would be proportional to the product of the voltage swing and the power supply voltage, not to the square of the voltage swing.

In recent literature, power supply stacking techniques have been incorporated into the low-voltage swing drivers [4, 6]. These drivers are called 'low-power stacked driver'. In [4], the power MOSFETs are also stacked to increase the maximum allowable power supply voltage. In [6], the half-rail bias node is tied to the common drain node of the power MOSFETs through two diode-connected NMOS transistors for recycling the excess charge stored at the half-rail bias node. Each driver chain employs reduced swing by swinging half-rail, between 0 and $V_{DD}/2$ or between $V_{DD}/2$ and V_{DD} for NMOS and PMOS, respectively. But the reduced drive of the MOSFET leads to the increased on-resistance, which can be alleviated by using a larger width for the MOSFET. The increased width of the MOSFET results in larger gate capacitance, which, in turn, increases the power dissipation. In addition, a capacitor is required to stabilize the half-rail bias voltage. For these reasons, larger chip area is required compared to the full-swing driver.

The optimized driver with the half-rail bias voltage causes a difference between the average charging current supplied by the high-side driver and the average discharging current supplied to the low-side driver. So, in this paper, the average charging and discharging currents are set equal to each other to find the intermediate bias voltage required for equal currents. By equating the two currents, equal amounts of charge enter and exit the capacitor for one clock period, which means that the voltage regulator does not have to charge or discharge the capacitor, on condition that the fluctuation of the intermediate bias voltage remain within the boundary set by the offset voltages in the regulator. So in this optimized driver, it is not necessary to connect an external load such as a digital circuit block to the intermediate bias voltage to use the excess stored charge in the capacitor.

In section II, power consumption is analyzed for a full-swing driver, a half-rail stacked driver, and an optimized stacked driver proposed in this paper. In section III, simulation results are shown for the three types of drivers discussed in section II. In addition, estimated area requirements are compared between the half-rail stacked driver and the new optimized stacked driver.

II. OPTIMIZED STACKED DRIVER

In the power stage of DC-DC buck converter, components of the power consumption has three terms, which are associated with MOSFETs, DC resistance (DCR) of the inductor, and equivalent series resistance (ESR) of the capacitor. The power loss related to ESR is usually neglected, which is much smaller than the others. In this paper, we focus on the MOSFET switch including the drivers, assuming equal load conditions.

1. Full-Swing Driver

In full-swing driver, the power loss caused by MOSFET is expressed as in Eq. (1) [7]. The power loss consists of switching and conduction power loss. To minimize the power loss, the width of MOSFET can be written as in Eq. (2), and the minimum power loss can be obtained as in Eq. (3). R_0 is determined by the process parameters and the supply voltage. The RMS current of the MOSFET is determined by the operating condition of the converter. E (which is energy loss associated with 1 μm transistor at every transition) must be controlled, because the switching energy is proportional to the

square of the voltage swing. As a result, the gate voltage swing must be controlled to minimize the power loss related to MOSFET.

$$P_{MOS} = \frac{R_0}{W} i_{rms}^{\ 2} + EWf_s \tag{1}$$

$$W_{opt} = \sqrt{\frac{R_0 i_{rms}^{\ 2}}{f_s E}} \tag{2}$$

$$P_{MOS}(\min) = 2\sqrt{R_0 i_{rms}^{\ 2} f_s E} \tag{3}$$

$$E \cong \frac{\alpha}{\alpha - 1}(C_{ox} + C_{gs} + 2C_{gd} + C_{db})V_{DD}^{\ 2} \tag{4}$$

Where :

- R_0 equivalent series resistance of a 1 μm-wide transistor;
- E energy loss per 1 μm-wide transistor;
- α tapering factor of gate drive chain.

2. Half-Rail Stacked Driver

Fig. 2 shows the half-rail stacked driver. The structure consists of an internal voltage regulator and a capacitor. In the initial condition, the half-rail bias voltage is regulated to be close to $V_{DD}/2$ by the internal voltage regulator. So each gate driver employs a low-voltage swing to reduce the switching energy at every transition. The high-side driver swings between V_{DD} and $V_{DD}/2$, and the low-side driver swings between $V_{DD}/2$ and ground. When the power PMOS turns on, the charge used by the high-side driver is supplied to the capacitor. When the power NMOS turns on, the charge stored in the capacitor is reused by the low-side driver. Therefore this structure can reduce the switching power loss, using low-voltage swing drivers and supply stacking techniques. In [4, 6], to optimize the conduction loss, the PMOS transistor has twice the width of the NMOS transistor. So the excess charge exists in the capacitor, and must be reused by digital blocks or removed by the internal voltage regulator in order to maintain the half-rail bias voltage.

In this structure, the power loss caused by MOSFET is

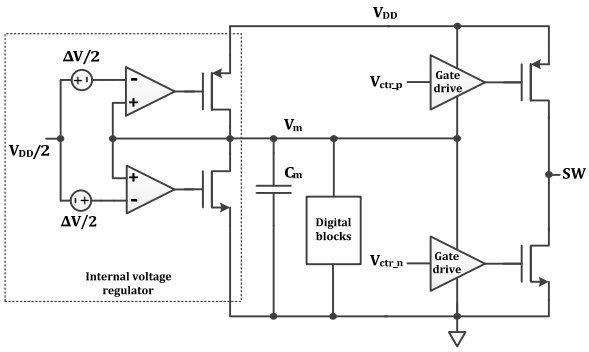


Fig. 2. Half-rail stacked driver.

described as in Eq. (5). This equation consists of the conduction loss and the switching loss (caused by gate drive and drain switching). The total power loss is described as in Eq. (6). This equation is composed of the conduction loss of MOSFETs and the supplied power for gate driver. In half-rail stacked driver, excess energy exists in the capacitor, and can be described as in Eq. (7).

$$P_{MOS} = \frac{R_H}{W} i_{rms}^{\ 2} + Wf_s \left\{ \begin{array}{l} (0.5V_{DD})^2 \left(\dfrac{C_{INV}}{\alpha - 1} + C_{G0} \right) \\ +0.5C_{D0}V_{DD}^{\ 2} \end{array} \right\} \tag{5}$$

$$P_{TOT} = \frac{R_{H-PMOS}}{W_P} i_{rms-PMOS}^{\ 2} + \frac{R_{H-NMOS}}{W_N} i_{rms-NMOS}^{\ 2} + 0.5(W_P C_{D0-PMOS} + W_N C_{D0-NMOS})V_{DD}^{\ 2} f_s + 0.5W_P V_{DD}^{\ 2} f_S \left(\frac{C_{INV}}{\alpha - 1} + C_{G0-PMOS} \right) \tag{6}$$

$$E_{stored} = 0.5^2 V_{DD}^{\ 2} \left\{ \begin{array}{l} \left(\dfrac{C_{INV}}{\alpha - 1} \right)(W_P - W_N) \\ +W_P C_{G0-PMOS} - W_N C_{G0-NMOS} \end{array} \right\} \tag{7}$$

Where, for a 1 μm-wide transistor :

- R_H equivalent series resistance when the gate-voltage swing is $V_{DD}/2$;
- C_{G0} equivalent gate capacitance;
- C_{D0} equivalent drain capacitance;
- C_{INV} sum of input and output capacitances when the sum of inverter transistor widths is 1 μm.

3. Optimized Stacked Driver

According to [8], to find the optimum voltage swing of driver, the gate voltage swing of MOSFET is normalized by the threshold voltage. Therefore the power loss of MOSFET is written as in Eq. (8). As a result, the optimum voltage swing is equal to 2 times the threshold voltage. But the results have some problems. First, even when the gate voltage swing is controlled, the voltage swing at the output node (which is connected to the inductor) is not changed and is always equal to the supply voltage. Second, the charge used by the high-side gate driver is reused by the low-side gate driver. Therefore the total power loss is not likely to be affected directly by the power related to the low-side gate driver, because the switching energy of the PMOS driver is usually larger than that of the NMOS driver. So Eq. (8) is not suitable for the design of the stacked driver. In addition, it is disadvantageous in terms of total chip area to use two regulators and two capacitors. So, in this paper, the structure of the half-rail stacked driver is utilized.

In a half-rail stacked driver, to optimize the conduction loss, the width ratio of PMOS and NMOS transistors is determined by the mobility difference. So the excess charge exists in the capacitor C_m. And the charge stored in C_m can be supplied to digital blocks. If the intermediate bias voltage falls below the lower limit or rises above the upper limit, the internal regulator will charge or discharge the capacitor to stabilize the intermediate bias voltage. When this occurs, the power consumption increases in the regulator. So the activation of the voltage regulator must be minimized.

$$P_{MOS} = \frac{R_\beta}{\beta W} i_{rms}^{\ 2} + \frac{\alpha}{\alpha - 1}(C_{G0} + C_{D0}) W (\beta + 1)^2 V_{TH}^{\ 2} f_s \tag{8}$$

Where :

- R_β equivalent series resistance of a 1 μm-wide transistor when the overdrive voltage is equal to V_{TH} ;
- β overdrive voltage divided by V_{TH}.

In this work, the stacked driver is optimized to minimize the required capacitance and the power consumption. To eliminate the excess stored charge in the capacitor, the amount of the charge delivered by the high-side driver, as in Eq. (9), must be set equal to the amount of the charge supplied to the low-side driver, as in Eq. (10), for one clock period. The intermediate bias voltage can be described as in Eq. (11). As a result, the total power loss of the driver is obtained as in Eq. (12). Both the width of MOSFETs and the intermediate bias voltage can be calculated using Eqs. (11, 12).

$$Q_{high-side} = W_P \left(\frac{C_{INV}}{\alpha - 1} + C_{G0-PMOS} \right) (V_{DD} - V_m) \tag{9}$$

$$Q_{low-side} = W_N \left(\frac{C_{INV}}{\alpha - 1} + C_{G0-NMOS} \right) V_M \tag{10}$$

$$V_M \approx \frac{V_{DD}}{1 + \frac{W_N}{W_P}} \tag{11}$$

$$P_{TOT} = \frac{R_{\beta-PMOS}}{W_P \left(\frac{V_{DD} - V_m}{|V_{THp}|} - 1 \right)} i_{rms-PMOS}^{\ 2} + \frac{R_{\beta-NMOS}}{W_N \left(\frac{V_m}{V_{THn}} - 1 \right)} i_{rms-NMOS}^{\ 2} + 0.5(W_P C_{D0-PMOS} + W_N C_{D0-NMOS}) V_{DD}^{\ 2} f_s + W_P f_s V_{DD} (V_{DD} - V_m) \left(\frac{C_{INV}}{\alpha - 1} + C_{G0-PMOS} \right) \tag{12}$$

III. SIMULATION RESULTS

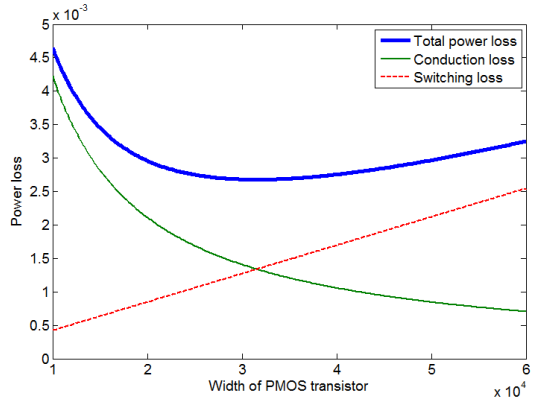
Simulation results were obtained by using 5 V MOSFET parameters of a 0.35 μm CMOS process. The simulation parameters are summarized in Table 1. The supply voltage is 3.7 V, which is the nominal voltage of a single-cell lithium-ion battery.

First, to compare the power loss among the three drivers, the width of MOSFETs must be determined. In full-swing driver, the width of MOSFETs is calculated using Eq. (2), and the power loss of MOSFETs is

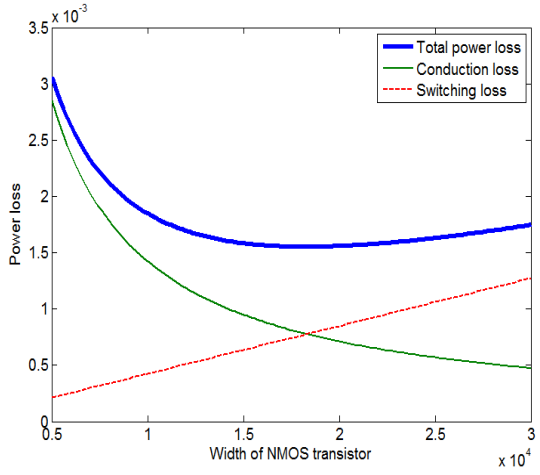
Table 1. Simulation parameters

Process	0.35 μm CMOS
Supply Voltage	3.7 V
Operation Duty	50%
Load Current	100 mA
Inductor Current Ripple (peak to peak)	100 mA
Switching Frequency	1 MHz
Tapering Factor (α)	5

calculated by using Eq. (1) or Eq. (3). Fig. 3 shows the power loss of the MOSFETs. The total power loss, the switching loss, and the conduction loss are indicated by the bold line, the dashed line, and the solid line, respectively. The widths of the PMOS and the NMOS are 31,400 μm and 18,200 μm, respectively. The switching loss is equal to the conduction loss when the power loss is the minimum, as shown in Fig. 3. The minimum power loss is 4.2330 mW.



(a)



(b)

Fig. 3. Power loss of the full-swing driver (a) PMOS, (b) NMOS.

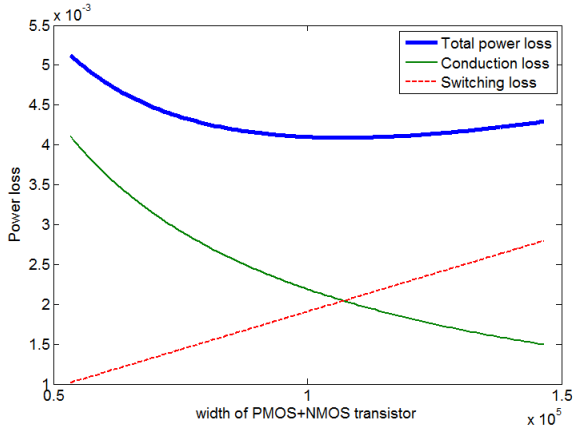


Fig. 4. Power loss of the half-rail driver.

In half-rail driver, the ratio of PMOS and NMOS is determined by the mobility difference in the devices. Fig. 4 shows the power loss of the half-rail driver. Using this result, the widths of PMOS and NMOS are determined. The widths of the PMOS and the NMOS are 80,475 μm and 26,825 μm, respectively. The total power loss is 4.0920 mW. But, in this case, excess energy is stored in the capacitor. The excess energy is described as in Eq. (7). The excess power is 0.4339 mW. So the real power loss of the driver is 3.6581 mW.

In case of the proposed driver, the intermediate bias voltage is determined by the width ratio between PMOS and NMOS, as written in Eq. (11). Fig. 5 shows the power loss of the proposed driver using Eq. (12). The minimum power loss is 3.6460 mW. The widths of PMOS and NMOS are 49,000 μm and 75,400 μm, respectively. The intermediate bias voltage is equal to about 0.446 times input voltage.

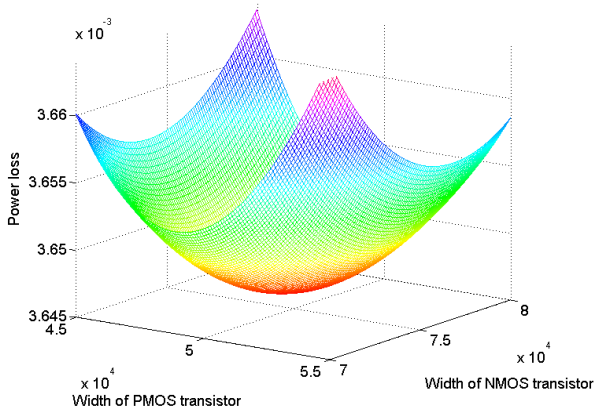


Fig. 5. Power loss as a function of the widths of PMOS and NMOS using the proposed method.

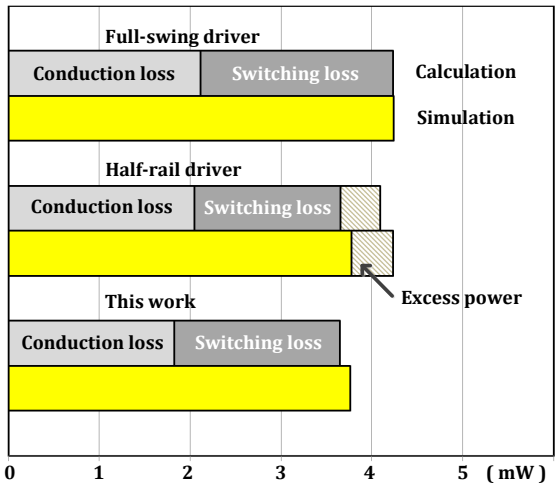


Fig. 6. Comparison among the three different drivers.

Table 2. Performance summary (simulation results)

	Full-swing	Half-rail	This work
PMOS width	31,600 μm	80,475 μm	49,000 μm
NMOS width	18,400 μm	26,825 μm	75,400 μm
Total width (with buffer)	62,500 μm	134,125 μm	155,500 μm
Total power loss	4.2410 mW	4.2309 mW	3.7615 mW
Excess power		0.4542 mW	
Real power loss	4.2410 mW	3.7767 mW	3.7615 mW
ΔV		100 mV	100 mV
Capacitor (Cm)		2.7 nF	2 nF
Total area (estimated)	0.12460 mm^2	1.5061 mm^2	1.2276 mm^2

Fig. 6 shows the comparison among the three different drivers. The difference between the half-rail driver and the proposed driver is less than 1%. But the required capacitance of the half-rail driver is 2.7 nF, while that of the proposed driver is only 2 nF. A regulation window ΔV of 100 mV is chosen in this work. Although the power loss is almost equal, the required capacitance is reduced by as much as 26%.

The simulated performance is summarized in Table 2.

IV. CONCLUSIONS

A stacked driver for synchronous buck converter was optimized based on the analysis of the power loss. To achieve the matching between charging and discharging current of the drivers, the equations associated with the charge and the power loss were obtained. Using those equations, the width of MOSFETs and optimum intermediate bias voltage could be calculated to minimize the total power loss and the chip area. The optimized stacked driver was verified through simulations done using 5 V MOSFET parameters of a typical 0.35-μm CMOS process. The difference in power loss between the conventional half-rail driver and the proposed driver was less than 1%. The estimated saving in chip area was approximately 18.5% compared to the half-rail driver.

ACKNOWLEDGMENTS

This work was supported by the Center for IT Convergence Agricultural Machinery(ITAM) grant(No. R10-3) funded by the Ministry of Knowledge Economy (MKE, Korea). The CAD tools were supported by the IC Design Education Center (IDEC), Korea.

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