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A New High-Efficiency CMOS Darlington-Pair Type Bridge Rectifier for Driving RFID Tag Chips

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RFID 태그 칩 구동을 위한 새로운 고효율 CMOS 달링턴쌍형 브리지 정류기

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Abstract In this paper, a new high-efficiency CMOS bridge rectifier for driving RFID tag chips is designed and analyzed. The input stage of the proposed rectifier is designed as a cascade structure connected with two NMOSs for reducing the gate capacitance by circuitry method, which is the main path of the leakage current that is increased when the operating frequency is increased. This gate capacitance reduction technique using the cascade input stage for reducing the gate leakage current is presented theoretically. The output characteristics of the proposed rectifier are derived analytically using its high frequency small-signal equivalent circuit. For the general load resistance of 50㏀, the proposed rectifier shows better power conversion efficiencies of 28.9% for 915㎒ UHF (for ISO 18000 -6) and 15.3% for 2.45㎓ microwave (for ISO 18000-4) than those of 26.3% and 26.8% for 915㎒, and 13.2% and 12.6% for 2.45㎓ of compared other two existing rectifiers. Therefore, the proposed rectifier may be used as a general purpose rectifier to drive tag chips for various RFID systems.

요 약 본 논문에서는 RFID 태그 칩 구동을 위한 새로운 고효율 CMOS 브리지 정류기를 설계하고 해석하였다. 동작 주파수가 높아짐에 따라 증가하는 게이트 누설전류의 주 통로가 되는 게이트 커패시턴스를 회로적인 방법으로 감소시키기 위해 제안한 정류기의 입력단을 두 개의 NMOS로 종속접속형으로 연결하여 설계하였으며, 이러한 종속접속형 입력단을 이용한 게이트 커패시턴스 감소 기법을 이론적으로 제시하였다. 또한 제안한 정류기의 출력특성은 고주파 소신호 등가회로를 이용하여 해석적으로 유도하였다. 일반적인 경우의 50㏀ 부하저항에 대해, 제안한 정류기는 915㎒의 UHF(for ISO 18000-6)에서는 28.9%, 2.45㎓의 마이크로파 대역 (for ISO 18000-4)에서는 15.3%의 전력변환효율을 보여, 915㎒에서 26.3%와 26.8%, 2.45㎓에서 13.2%와 12.6%의 전력변환효율을 보인 비교된 기존의 두 정류기에 비해 보다 개선된 전력변환효율을 보였다. 따라서 제안한 정류기는 다양한 종류의 RFID 시스템의 태그 칩 구동을 위한 범용 정류기로 사용될 수 있을 것이다.

Key Words : RFID, Darlington-pair, Gate leakage current, Power conversion efficiency

1. Introduction

Recently, RFID leads the innovative progress in many manufacturing and service industries such as transportation, security, purchasing and distribution logistics, medical services, and so on.

Now, it becomes one of the top technologies for this century and has revolutionized the human life style[1-4].

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In RFID systems, the rectifier converts the received RF signal into the DC voltage required to operate the tag chip. Therefore, the rectifier is the essential part in the passive RFID tags.

To obtain a high DC output voltage and a high power conversion efficiency, various type rectifiers were developed [5-7] and many researches were performed for improving the output characteristics [8-12]. Among these rectifiers, the CMOS gate cross-connected rectifier is of considerable interest because its minimum input voltage required for obtaining effective DC voltage is lower, its converted DC voltage is higher than other type rectifiers, and its power conversion efficiency is over 60% for an input signal frequency of 13.56㎒[5, 6].

However, its power conversion efficiency decreases rapidly in frequency ranges over UHF because of the increased leakage current through the gate capacitance.

For reducing the gate leakage current in high frequencies, a recipe for increasing the impedance by reducing the gate capacitance will be considered. One solution for reducing the gate capacitance is to increase the gate oxide thickness. However, this solution may not be a good one because of the variation of threshold voltage and the problems on manufacturing process. Another solution is to reduce the gate capacitance by the circuitry method. This solution was introduced in our previous paper published in J. of IEEK[8]. In the previous paper, designing its input stage as the current-mirror type with series-parallel connected three NMOSs, the gate capacitance, which is the main path of the leakage current, was reduced by the circuitry method. In addition, the input voltage between antennas was distributed to each gate capacitance. Therefore, the gate leakage current is decreased considerably by both the increased impedance of gate capacitance and the reduced gate voltage.

However, this previous current-mirror type rectifier has some demerits such as; the number of transistors on the input stage is increased, therefore, the structure of the input stage is somewhat complicated, and the rectified DC voltage is reduced slightly due to the voltage drop effect in bi-level structure of the input stage.

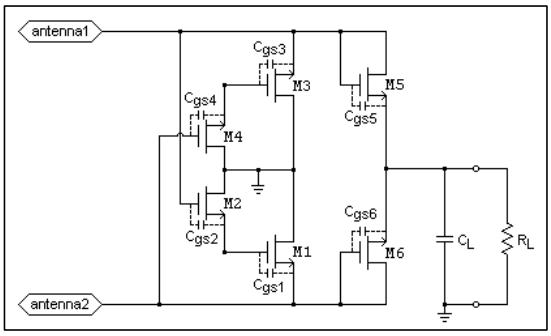
To improve these demerits, in this paper, the input stage of the rectifier is designed as a cascade structure connected with two NMOSs. The output characteristics of the proposed rectifier are derived analytically using its high frequency small-signal equivalent circuit. Then, the gate capacitance reduction technique to decrease the gate leakage current which is increased with the operating frequency is presented theoretically by the circuitry method. The proposed rectifier is designed with the MOSIS T28M TSMC 0.18㎛1Poly-6Metal CMOS process (Technology: SCN018) and verified by comparing its output characteristics with those of existing rectifiers.

2. Proposed Darlington-Pair Type Rectifier

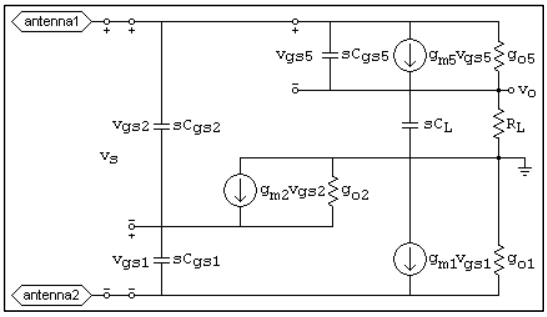
For decreasing the gate leakage current due to the increasing of operating frequency, the gate impedance has to be increased by reducing the gate capacitance which is the main path of the leakage current. To reduce the gate capacitance, the new bridge rectifier whose input stage is designed as a cascade structure connected with two NMOSs is presented in Fig. 1. This cascade input stage is more simple than the current-mirror type structure which is designed with series- parallel connected three NMOSs.. In this cascade structure, the gate capacitances of two NMOSs are connected in series. Therefore, if two NMOSs are matched, the whole gate capacitance of the input stage is reduced in half, which is less than that of the current-mirror type structure. This cascade structure looks like a Darlington-pair. So, we named this new rectifier as ‘a CMOS Darlington-pair type Bridge Rectifier' based on the structural type.

The operating principle of the proposed rectifier for (+) half period of RF input source as follow:

When the peak-to-peak RF input voltage V_p is applied onto two antenna ports, it is distributed to M1 and M2. If M1 and M2 are same, V_{gs1} equals to V_{gs2} ($= V_p/2$). And since the source of M2 is connected to the gate of M1, the channel current of M2 does not flow. Then the gate potential of M1 equals to the drain potential of M2, which is connected to ground. It means V_{gs1} equals to V_{ds1}. Thus M1 always operates in saturation region as like as M5, which may work as a diode. Therefore, the proposed rectifier operates, in principle, like a general diode connected bridge rectifier.



[Fig. 1] Proposed CMOS Darlington-pair type bridge rectifier



[Fig. 2] High frequency equivalent circuit for (+) half period

2.1 Analysis of Output Characteristics

The high frequency small-signal equivalent circuit for (+) half period of the proposed Darlington-pair type rectifier is presented in Fig. 2. The gate-drain capacitance and other parasitic capacitances except the gate-source capacitance which is the main path of the leakage current are not included in Fig. 2 for simplifying the circuit analysis. From this high frequency small-signal equivalent circuit shown in Fig. 2, the output voltage of the designed rectifier is obtained as eq. (1) by node analysis.

$$v_o = \frac{g_{m1} + g_{o1} + s\,C_{gs1}(1 - \frac{g_a}{g_b})}{g_L + (1 + \frac{g_L}{g_c})(g_{o1} + g_{o2}\frac{g_a}{g_b})} v_s \qquad (1)$$

where,

$$g_a = g_{m1} + s\,C_{gs1} + s\,C_{gs2},$$
$$g_b = g_{m2} + g_{o2} + s\,C_{gs1} + s\,C_{gs2},$$
$$g_c = g_{m5} + g_{o5} + s\,C_{gs5}, \qquad (2)$$
$$g_L = s\,C_L + \frac{1}{R_L}$$

C_{gsi} is the gate-source capacitance, g_{mi} is the transconductance, g_{oi} is the output conductance, and g_L is the load conductance. If M1 and M2 are same, g_{m1} equals to g_{m2}, Furthermore, if $g_{o2} \ll g_{m2} + s\,C_{gs1} + s\,C_{gs2}$, $g_a \approx g_b$, Then, eq. (1) is simplified to eq. (3).

$$v_o = \frac{g_{m1} + g_{o1}}{g_L + (1 + \frac{g_L}{g_c})(g_{o1} + g_{o2})} v_s \qquad (3)$$

This eq. (3) is nearly same as the output voltage relationships of the existing simple gate cross-connected rectifier or the current-mirror type rectifier[8]. If $g_{o1}, g_{o2} \approx 0$, eq. (3) is still more simplified to eq. (4), which is the same as the output voltage relationships of the above two existing rectifiers[8].

$$v_o \approx \frac{g_{m1}}{g_L} v_s \qquad (4)$$

These equations show that the output voltage of proposed rectifier varies in linear for the input voltage alike the above two compared rectifiers. Therefore, the proposed rectifier also has the merit of higher output voltage characteristics as like as the gate cross-connected one than other type rectifiers. In addition, we can see in eq. (1) that if g_{m1} or g_{m5} are increased by raising W/L ratio of M1 or M5, the output voltage of proposed rectifier is increased more.

2.2 Gate leakage current reduction by circuitry method

In the proposed Darlington-pair type rectifier, the theoretical basis for reducing the gate leakage current by circuitry method is as follows.

The gate-source capacitance of MOS transistor is the main path of gate leakage current in high frequencies. Therefore, it has to be reduced to decrease the gate leakage current. In the small-signal equivalent circuit of Fig. 2, C_{gs1} and C_{gs2} are connected in series. Thus, the equivalent capacitance between two antennas $C_{eq(Darlington)}$ is obtained as eq. (5).

$$C_{eq(Darlington)} = \frac{C_{gs1} C_{gs2}}{C_{gs1} + C_{gs2}} < C_{gs1} \quad (5)$$

This equivalent capacitance, $C_{eq(Darlington)}$, is smaller than that of the current-mirror type rectifier, $C_{eq(Mirror)}$, which is obtained as next eq. (6) as well as that of the existing simple gate cross-connected rectifier, C_{gs1}[8].

$$C_{eq(mirror)} = \frac{(C_{gs1} + C_{gs2}) C_{gs3}}{C_{gs1} + C_{gs2} + C_{gs3}} \quad (6)$$

Then, under the same frequency, the impedance between two antennas in the proposed Darlington-pair type rectifier, $|Z_c|_{Darlington} (= \frac{1}{\omega C_{eq(Darlington)}})$, is larger than those of the current-mirror type rectifier, $|Z_c|_{mirror} (= \frac{1}{\omega C_{eq(mirror)}})$, or the existing simple gate cross-connected rectifier, $|Z_c|_{simple} (= \frac{1}{\omega C_{gs1}})$. Therefore, the gate leakage current of the proposed Darlington-pair type rectifier is reduced more than those of the compared two rectifiers. In addition, because the input voltage between antennas was distributed to each gate capacitance of two transistors connected in cascade on input stage, the voltage across each capacitance is reduced, too. Therefore, the gate leakage current is decreased considerably by both the increased impedance of gate capacitance and the reduced gate voltage.

As a result, the proposed Darlington-pair type rectifier shown in Fig. 1 reduces the gate leakage current effectively in high frequency region. So, it may be used as a generic rectifier for supplying DC voltage necessary to drive the tag chips of various RFID systems using the frequency range of 13.56㎒ HF (for ISO 18000-3), 915㎒ UHF (for ISO 18000-6), and 2.45㎓microwave (for ISO 18000-4).

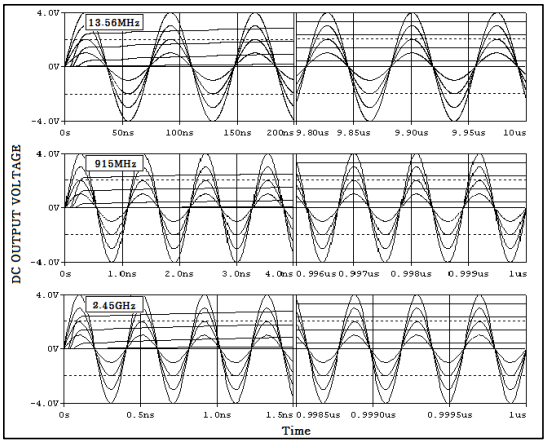
3. Results and Discussion

To verify the reduction of gate leakage current and to show the DC conversion characteristics, the proposed Darlington-pair type rectifier shown in Fig. 1 is simulated by using the MOSIS T28M TSMC 0.18㎛ 1Poly-5Metal CMOS process (Technology: SCN018) and compared with those of the simple gate cross-connected rectifier and the current-mirror type rectifier.

The component values used for simulation are summarized in Table 1.

[Table 1] Component Values (W/L, ㎛)

Component	Value	Component	Value
M1	3.6/0.18	C_L	1㎋ for 13.56㎒ 100㎊ for 915㎒ 10㎊ for2.45㎓
M2	3.6/0.18		
M3	3.6/0.18		
M4	3.6/0.18		
M5	3.6/0.18	R_L	45㏀
M6	3.6/0.18		

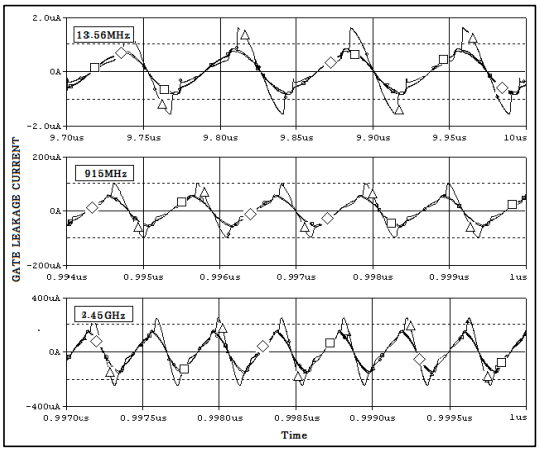


[Fig. 3] Converted DC output voltages for 13.56㎒, 915㎒, 2.45㎓ inputs

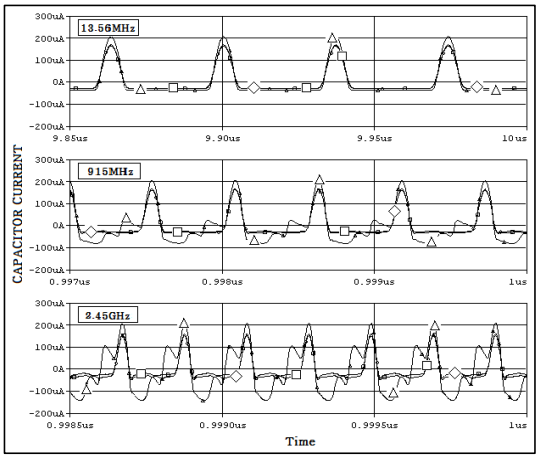
Fig. 3 shows the converted DC output voltages for the frequencies of 13.56㎒ HF, 915㎒ UHF, and 2.45㎓ microwave. These results show that the proposed rectifier converts 1V-4V peak-to-peak input voltages to well-rectified high enough DC output voltages. The obtained percent ripple coefficient is 0.0065%.

The gate leakage currents for the frequency variation at the 2V peak-to-peak input voltage are compared in Fig. 4. For 13.56㎒ HF, the simple gate cross-connected rectifier shows the maximum gate leakage current of 1.56㎂, but the current-mirror type rectifier and the proposed rectifier show nearly same of 0.83㎂. For 915㎒ UHF, the simple

gate cross-connected rectifier shows the maximum gate leakage current of 96.1㎂, but the current-mirror type rectifier shows 58.8㎂ and the proposed rectifier shows 55.7㎂. For 2.45㎓, the simple gate cross-connected rectifier shows the maximum gate leakage current of 244.3㎂, but the current-mirror type rectifier shows 158.1 ㎂ and the proposed rectifier shows 144.3㎂.These results of Fig. 4 show that the proposed rectifier reduces effectively the gate leakage current which is increased in high frequency.

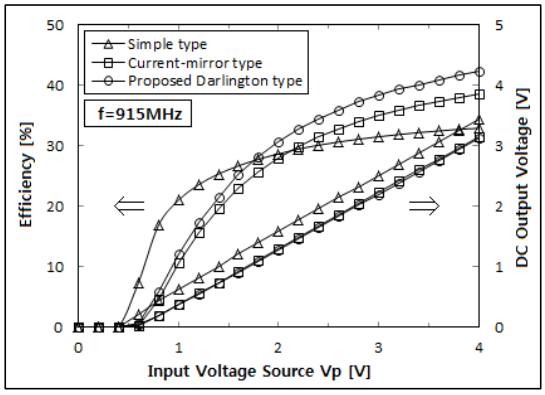


[Fig. 4] Gate leakage current for frequency variation
△ : Existing gate cross-connected rectifier[5]
□ : Existing current-mirror type rectifier[8]
◇ : Proposed Darlington pair type rectifier

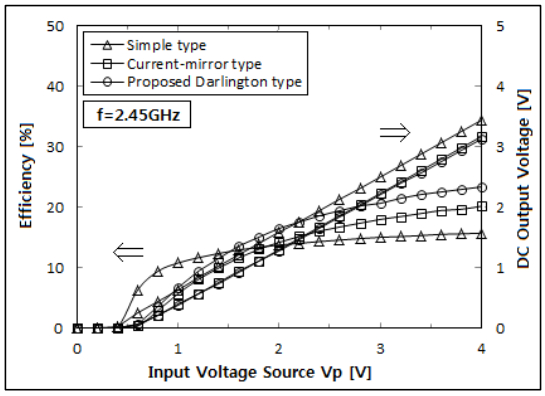


[Fig. 5] Capacitor current I(CL) for frequency variation
△ : Existing gate cross-connected rectifier[5]
□ : Existing current-mirror type rectifier[8]
◇ : Proposed Darlington pair type rectifier

The capacitor current I(C_L) for the frequency variation are shown in Fig. 5. This Fig. 5 shows that the capacitor discharge current flows nearly all through the load resistor R_L in the proposed and the current-mirror type rectifiers. However, the higher frequency is, the larger gate leakage current is in the simple gate cross-connected rectifier.



(a) 915㎒



(b) 2.45㎓

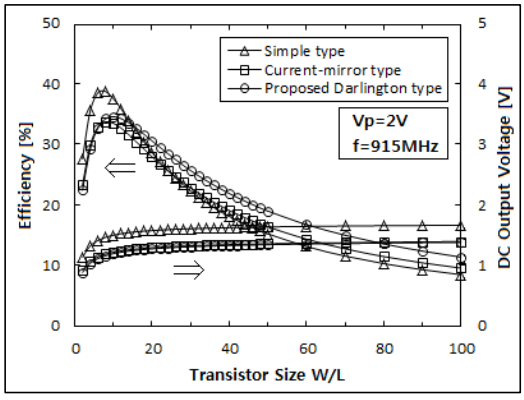
[Fig. 6] Power conversion efficiency and DC output voltage versus Input voltage source

The power conversion efficiency and the DC output voltage versus the input voltage source for frequencies of 915㎒ and 2.45㎓ are shown in Fig. 6. This Fig. 6 shows that the power conversion efficiency of the simple gate cross-connected rectifier is highest in the region of low input voltages. But as the input voltage is increased, the proposed rectifier shows the highest power conversion efficiency. However, the converted DC output voltage of the proposed Darlington-pair type and the current-mirror type rectifiers shows lower values about 0.3V than that of

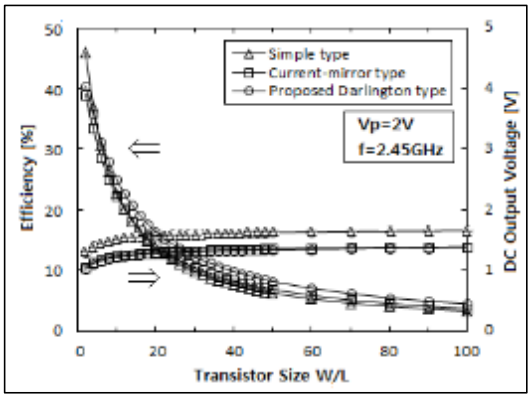
the simple gate cross-connected rectifier. This is caused by the voltage drop effect in bi-level structure of the input stage.

The power conversion efficiency and the converted DC output voltage versus the transistor size W/L are shown in Fig. 7. As the transistor size is increased, the efficiency is decreased rapidly. This comes from that the larger transistor is, the higher gate capacitance is, then the leakage current through the gate capacitance is increased.

As considered in Fig. 4, when the frequency is increased, the impedance of gate capacitance is decreased, then the leakage current is increased.



(a) 915㎒



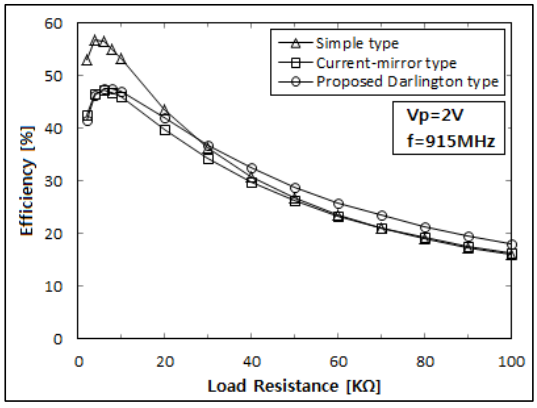
(b) 2.45㎓

[Fig. 7] Power conversion efficiency and DC output voltage versus Transistor size W/L

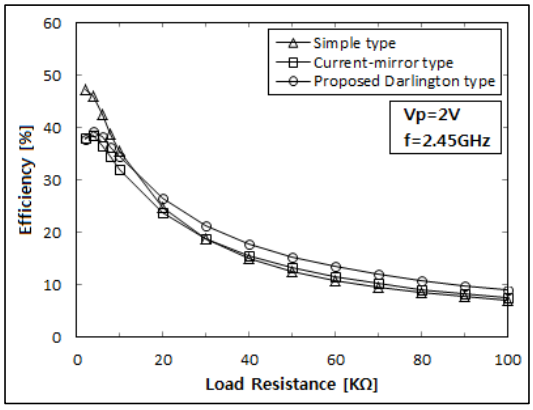
Therefore, in Fig. 7, we can see that the power conversion efficiency for 2.45㎓ is reduced considerably than that for 915㎒. In addition, the proposed Darlington-pair type rectifier shows the highest power conversion efficiency among compared rectifiers in the region of W/L>14 for 915㎒ and W/L>5 for 2.45㎓.

On the other hand, the converted DC output voltage is increased nearly linearly as the W/L ratio is increased in the region of W/L<10, but in the region over that ratio, the converted DC output voltage is increased gradually.

Therefore, considered the power conversion efficiency, the converted DC output voltage, and the whole chip area, it looks like that the transistor size of W/L=20 is optimal from Fig. 7.



(a) 915㎒



(b) 2.45㎓

[Fig. 8] Power conversion efficiency versus Load resistance

The power conversion efficiency versus the load resistance is shown in Fig. 8. From this Fig. 8, we can see that as the load resistance and/or the frequency are increased, the power conversion efficiency is decreased because of the increased leakage current through the gate capacitance. In this Fig. 8, the proposed Darlington-pair type rectifier shows the highest power conversion efficiency among compared rectifiers in the region of load

resistance R_L>30㏀ for 915㎒ and R_L>10㏀ for 2.45㎓.

From these results, we can see that the proposed Darlington-pair type rectifier shows better power conversion efficiency for the variation of load resistance and in the frequency range from 915㎒ UHF to 2.45㎓ microwave.

4. Conclusions

In this paper, a new high-efficiency CMOS bridge rectifier for driving RFID tag chips is proposed. It's input stage is designed as a cascade structure for reducing the gate capacitance by circuitry method, which is the main path of the leakage current that is increased when the frequency is increased. This gate leakage current reduction effect of the proposed Darlington-pair type rectifier is presented theoretically. The output characteristics are analyzed using the high frequency small-signal equivalent circuit and compared with those of the existing simple gate cross-connected rectifier and the current mirror type rectifier. The proposed Darlington-pair type rectifier is designed with the MOSIS T28M TSMC 0.18㎛ 1Poly-6Metal CMOS process (Technology: SCN018) and verified by comparing with existing rectifiers.

From the results, we can see that the gate leakage current is reduced considerably in high frequencies, compared with those of existing rectifiers. For the general load resistance of 50㏀, the proposed rectifier shows better power conversion efficiencies of 28.9% for 915㎒ UHF (for ISO 18000 -6) and 15.3% for 2.45㎓ microwave (for ISO 18000-4) than those of 26.3% and 26.8% for 915 ㎒, and 13.2% and 12.6% for 2.45㎓ of compared other two existing rectifiers. In addition, the proposed rectifier shows more stable power conversion efficiencies than compared other two existing rectifiers for the variation of load resistance.

Therefore, the proposed Darlington-pair type rectifier may be used as a general purpose rectifier for driving various RFID tag chips using the operating frequencies of 13.56㎒ HF for ISO 18000-3, 915㎒ UHF for ISO 18000-6, and 2.45㎓ microwave for ISO 18000-4.

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<Research Interests>
Device modeling, Analog and RF IC design, and RFID.