Bandwidth-Related Optimization in High-Speed Frequency Dividers using SiGe Technology

Chao-Zhou Nan*, Xiao-Peng Yu*, Wei-Meng Lim, Bo-Yu Hu*, Zheng-Hao Lu**, Yang Liu***, and Kiat-Seng Yeo****

Abstract—**In this paper, the trade-off related to bandwidth of high-speed common-mode logic frequency divider is analyzed in detail. A method to optimize the operating frequency, band-width as well as power consumption is proposed. This method is based on bipolar device characteristics, whereby a negative resistance model can be used to estimate the optimal normalized upper frequency and lower frequency of frequency dividers under different conditions, which is conventionally ignored in literatures. This method provides a simple but efficient procedure in designing high performance frequency dividers for different applications. To verify the proposed method, a static divide-by-2 at millimeter wave ranges is implemented in 180 nm SiGe technology. Measurement results of the divider demonstrate significant improvement in the figure of merit as compared with literatures.**

Index Terms—**Frequency divider, simplified models, bandwidth and power optimization, transistor area selection, design flow**

I. INTRODUCTION

The trend to achieve higher data rate in communication systems has been demonstrated in the past decades and will certainly continue in the future. A series of work released recent years on 60-GHz transceivers [1, 2] reveals the advantage of utilizing an unlicensed band at millimeter wave range. However, as current high-speed communications are usually implemented in portable devices, low power consumption is highly desired to maintain a long standby time. The frequency divider in phase-locked loops (PLLs), which is an essential high frequency component in a wireless transceiver, consumes a significant portion of total power consumption. The divide-by-2 stage which follows the output of the voltage controlled oscillator operates at the highest frequency in such a system. Its low power but high-speed operation is a great challenge. Moreover, in nowadays high-speed communication system, there is a trend of wide band operation to accommodate high transfer rate. For example, in IEEE 802.15.3c, defined at 60 GHz, a 10 GHz operation range is required. This set the operation range of a frequency divider for such application. The divide-by-2 at millimeter wave range is therefore commonly considered to be one of the bottlenecks in the implementation of a transceiver.

A substantial work has been done in literatures to overcome the difficulty of high-speed frequency dividers. Several types of dividers have been demonstrated. Static dividers [3], provide a relatively wide range of operation, but only able to work at lower frequencies. Thus, it is not widely used in millimeter wave range applications. The injection-locked dividers [4], on the other hand, offer the highest operation frequency, but usually with narrow operation range. Miller dividers [4], also known as regenerative dividers, act as a compromise of these two cases.

For applications whereby wide bandwidth is required,

Manuscript received Sep. 5, 2011; revised Nov. 11, 2011.
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e.g. the 60 GHz applications, frequency divider based on common mode logic (CML) is a preferred topology. It exhibits a wide operation range and small silicon area since no inductor is needed. Compared with injection-locked or Miller-type frequency dividers which are limited within a narrow range, the CML divider is more robust against process variations and modeling uncertainties in practice. Nevertheless, to design a high performance CML frequency divider, it has trade-offs among power consumption, operating frequency, bandwidth, sensitivity, which is not a straightforward task. Several techniques or optimization methods have been demonstrated in literatures [5-7]. For example, [5] proposed the method to determine the way to determine the highest operating frequency and power consumption trade-offs. [6] summarized the overall considerations in designing CML circuits. But in literatures, no theoretical work has been dedicated to the analysis of the frequency divider bandwidth. Hence it is not easy to precisely determine the bandwidth or the trade-off between bandwidth with other design considerations. In current practice, circuit simulators such as Cadence Spectre RF, are widely used to evaluate the upper and lower frequency of frequency divider circuit. But this solution does not present much of design insight. For designer, optimization is still greatly depending on experience and massive simulation work in EDA tools. These procedures and practices are very time consuming and impractical, especially for large circuits.

The work in this paper provides a theoretical analysis of bandwidth-related tradeoffs in a high-speed BiCMOS frequency divider, which is currently widely used at millimeter wave range frequency. Theoretical work is also verified by implementation on the high performance circuit. The paper is organized as follows: Section 2 discusses the model derivation and theoretical analysis in the divide-by-2. Section 3 describes the optimization of a divide-by-2 circuit. Section 4 presents the 40 GHz static frequency divider design using the proposed bandwidth and power optimized design flow. The conclusions are given in section 5.

II. MODEL DERIVATION AND THEORETICAL ANALYSIS

It is well known that two CML D-latches in a master/Slave can function as a fully differential frequency divider shown in Fig. 1. Each D-latch is triggered by a CLKP and CLKN signal, namely, the input differential signals. The D-latches always operate at two different modes periodically [6]. Conceptually, the operation mode of such a divider can be described as follows: when the clock signal CLKP is logically low, one of the latches is under sensing mode. The D-latch senses the input signal and flips it to the output. On the other hand, when the input CLKP signal is logically high, the D-latch is under latching mode. It latches and holds the current state. This periodical operation makes the input signal divided to be half of the input one.

Note that in this paper, the divider is designed for a certain input frequency first, and then followed by corresponding bandwidth optimization. Considering the identical cascade configuration of the D-latches, the effort of model deviation will focus on a single D-latches block. As the former studies [8] revealed, the upper operation frequency of a D-latch is related to the CML block, while the lower frequency of bandwidth mostly depends on the cross-coupled block. These findings suggest that, the upper frequency and lower frequency can be determined by separately analyzing the sensing and latching modes.

To determine the operating frequency of a divider, propagation delay can be used as an important indicator. In practice, it has been used as a measure of performance and to demonstrate the load driving capability as well as analyze the effects of device scaling [9], while time constant τ of cross-coupled sub-circuit is a norm to evaluate the lower frequency of bandwidth [10]. In this work, the analytical models of CML block, as well as the latching model of cross-coupled block respectively, are

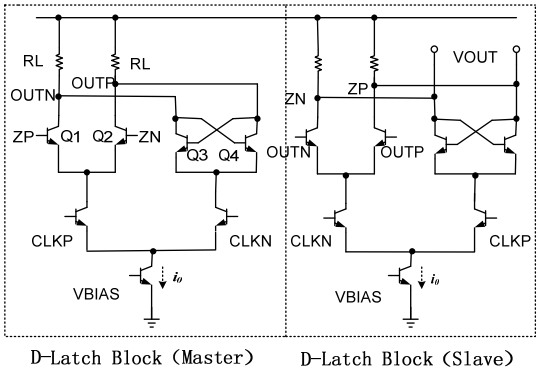


Fig. 1. Schematic of a conventional static frequency divider.

used to determine the optimal biasing current i_o (or load resistor R_L) for a transistor of certain emitter area when driving a source of voltage swing (ΔV) with slew time (t_r).

1. The sensing mode

A simplified circuit, also known as CML architecture with constant loading under sensing mode, is shown in Fig.2. The load capacitors are related to the input parasitic parameters of the cascade cross-coupled block and the CML circuit belongs to next D-latch stage.

When analyzing a bipolar circuit, the Gummel-Poon SPICE bipolar transistor model [11] is considered as a workhorse model, for its time-efficiency and the easily availability of the model parameters. Considering the premise of divider's low current and voltage swing operating environment, a simplified Gummel-Poon SPICE model with linear diode, representing base emitter junction, is adopted. The simplified linear bipolar model is shown in Fig. 3.

For fully description, the five storing elements in the model involve fifth-order characteristic nodal equations, hence analytical solution is impractical. Fortunately, an improved superposition principle, based on MIT's open-circuit time constant theory [12], has been developed [9].

$$t_{pd} = (t_{pdC_d}^2 + t_{pdC_{jci}}^2)^{0.5} + t_{pdC_{js}} + t_{pdC_L} + t_{pdC_{jcx}} \quad (1)$$

Where the five parameters represent five different corresponding delay components, respectively. They are

(1) t_{pdC_d} is the propagation delay caused by transit-time/diffusion capacitance;

(2) $t_{pdC_{js}}$ is the propagation delay caused by collector-substrate capacitance;

(3) $t_{pdC_{jci}}$ is the propagation delay caused by intrinsic base-collector capacitance;

(4) $t_{pdC_{jcx}}$ is the propagation delay caused by extrinsic base-collector capacitance;

(5) t_{pdC_L} is the propagation delay caused by loading capacitance at output node.

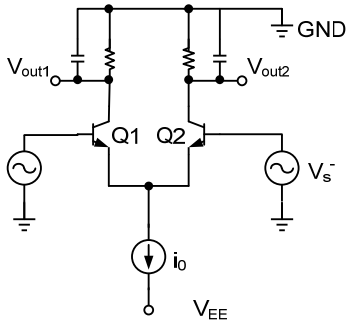


Fig. 2. Circuit diagram of the CML gate.

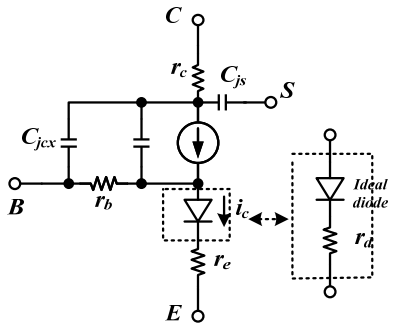


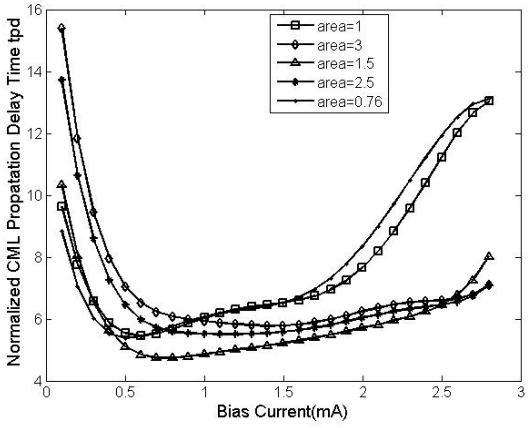
Fig. 3. Linearized bipolar transistor model.

In order to acquire a quantitative description for each case, transient analysis with objective capacitor reserved and other capacitors removed (open-circuited) in time segments has to be carried out. An exhaustive theory [9] analyzing these cases, has been developed.

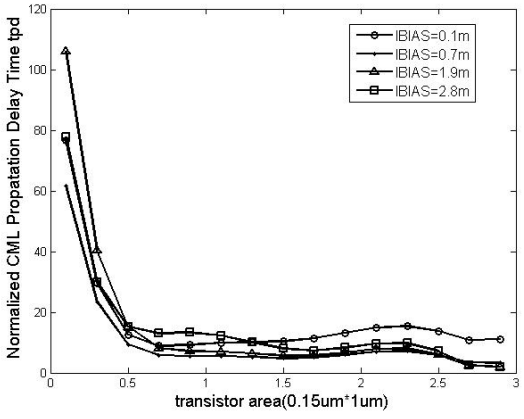
Calculations and simulations, based on Khalef's theory, are carried out using 0.18 μm SiGe technology which are suitable for high frequency divider design. The dependence on the CML propagation delay, normalized by a constant, is illustrated in Fig. 4(a) for different transistor areas. To make capital of technological limitation of the process, it is assumed that the emitter width is always kept at it minimum value (i.e. 0.15 μm in the given SiGe process), whenever the transistor area is recalled. Therefore, an area of 1, 2, 3 refers to 0.15 μm × 1 μm, 0.15 μm × 2 μm, and 0.15 μm × 3 μm, respectively. The delay behavior in Fig. 4(a) indicates that there is always an optimum bias current for a certain transistor area, to achieve the maximum switching speed.

The delay versus transistor emitter area at different values of bias current is shown in Fig. 4(b). In order to gain a deep insight into the delay of a CML cell as a function of bias current and transistor area, a design space in three-dimensional plane has been shown in Fig.

5. Since the propagation delay is used as performance measure, it is reasonable to improve the load sensitivity by operating at large bias currents. However, the degradation due to high-current effects should be considered if the circuit is designed at certain transistor area (e.g, derived from Fig. 5, more than 1.9 ma in a transistor, which is smaller than 0.15 μm × 0.76 μm for this case). The trend of the model agrees perfectly with our estimation.



(a)



(b)

Fig. 4. Normalized propagation delay versus (a) Bias current, at Tr.area=0.76, 1, 1.5, 2.5, 3*0.15 μm*1 μm, (b) Transistor area, at IBIAS=0.1, 0.7, 1.9, 2.8 ma.

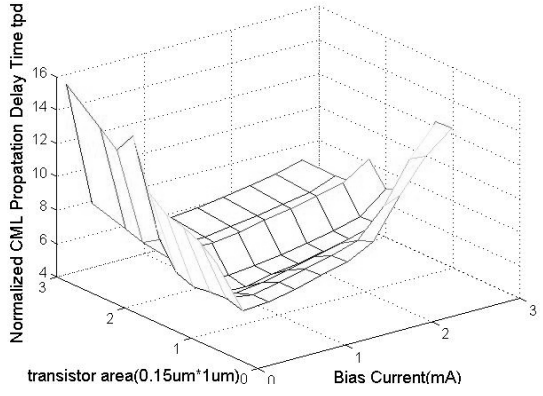


Fig. 5. CML propagation delay versus bias current and Tr. area.

2. The investigated latching mode

Fig. 6 shows a sub-circuit operating under latching mode, which is also known as cross-coupled architecture. The cross-coupled pair configures as a positive feedback to latch the output. This architecture exhibits a parasitic negative resistance, $R_{nr}(v_c)$, across the collector nodes of the cross-coupled transistors, Q_1 and Q_2.

When considering the latching mode from the negative resistance perspective, the first order zero-input response in time-domain, is largely determined by R_p, and also hindered by a nonlinear negative impedance, $-R_{nr}(v_c)$, as shown in Fig. 7(a) and (b).

Consider certain electric energy referred to the capacitance value, zero-input response begins under an initial condition, which is determined by sensing mode. The non-linearity in $R_{nr}(v_c)$ increases the resistance magnitude as the electric energy decreases, taken here by sampling the voltage across the capacitor, $v_c(t)$. The first-order differential equation that describes this model can be expressed as

$$Z(v_c) * C \frac{dv_c(t)}{dt} + v_c(t) = 0 \qquad (2)$$

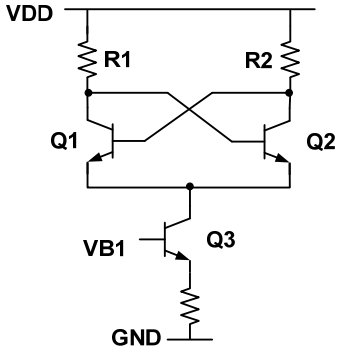


Fig. 6. Circuit diagram of cross-coupled block.

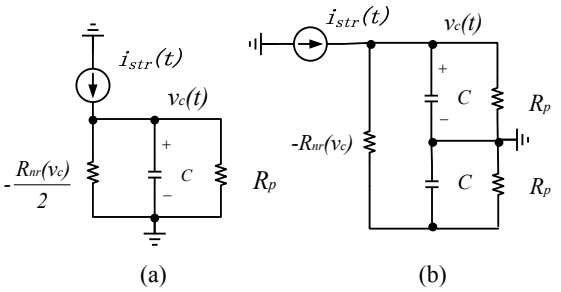


Fig. 7. A simplified behavior model of cross-coupled (a) Single-ended configuration, (b) Differential configuration.

where $Z(v_c)$ is the parallel combination of R_p and $-R_{nr}(v_c)$, and C is total parasitic capacitance at the output node. The unforced state of this model is defined entirely by the initial conditions of the voltage across the capacitor, $v_c(0)$, for a given reference time $t = 0$.

Under small-signal conditions, the negative resistance of this model has been demonstrated as approximately equal to $-2/g_m$, where g_m is the trans-conductance of a HBT in the cross-coupled architecture [13]. Considering the nonlinear behavior mentioned above, it is necessary to replace g_m with its large signal equivalent, $G_M(v_c)$, to express the negative resistance as below,

$$-R_{nr}(v_c) = -\frac{2}{G_M(v_c)} \tag{3}$$

Note that the SiGe HBTs are assumed to operate in the forward-active mode by making this substitution. From (2) and (3), a first-order differential equation for the model under latching mode can be given as:

$$\frac{2R_pC}{2 - R_pG_M(v_c)}\frac{dv_c(t)}{dt} + v_c(t) = 0 \tag{4}$$

The large-signal transfer characteristic, taking the form of a hyperbolic tangent, can be applied to demonstrate a differential pair, simplified from the cross-coupled transistors. Its fourier series expansion shows that this function is odd and is consists of no power in even-numbered harmonics. Referring to the derivation highlighted in [14], an expression for $G_M(v_c)$ can be found as below,

$$G_M(v_c) = \frac{2g_m}{k\pi v_c}\int_{-\pi}^{\pi} \tanh\left(\frac{kv_c}{2}\cos\theta\right)\cos\theta\, d\theta \tag{5}$$

Where k is a constant scaling factor including the ther mal voltage, V_T. And g_m of a HBT has been demonstrated as approximately equal to I_{bias}/V_T. Actually, there is no closed-form solution exist for Eq. (5). It therefore prevents closed-form analysis of transient conditions regardless of any nonlinearity characteristic applied to Eq. (4). So numerical methods and phase-plane analysis tools, such as matlab, become necessary to find solutions to Eq. (5) across v_c, which is a premise to get the solutions to the differential equations describing the model in Fig. 7.

Conventionally, in order to gather insight into the transition rate, we defined a time constant, $\tau = Z(v_c)C$, which has the dimension of time. Since there is inverse exponential relation between τ and the attenuation of first-order zero-input response, it is reasonable to take τ as performance measure.

The dependence of the time constant, τ, predicted by the model on the bias current, is illustrated in Fig. 8 for various emitter area. The graphs show the impact of the bias current on the time constant arising after a certain point. Furthermore, its dependency on bias current becomes weakening as the emitter area grows.

The design space can be represented in a three-dimensional plane to demonstrate the time constant in

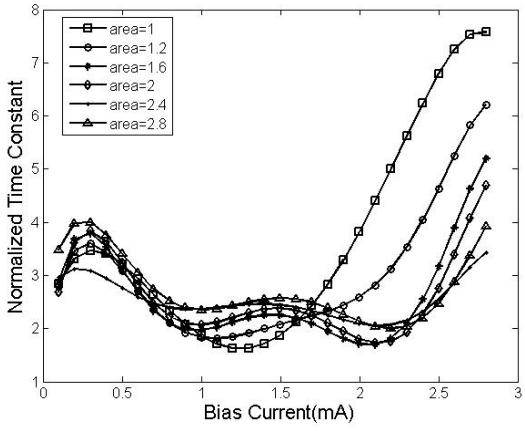


Fig. 8. Normalized time constant versus bias current at Tr.area=1, 1.2, 1.6, 2, 2.4 2.8*0.15 μm*1 μm.

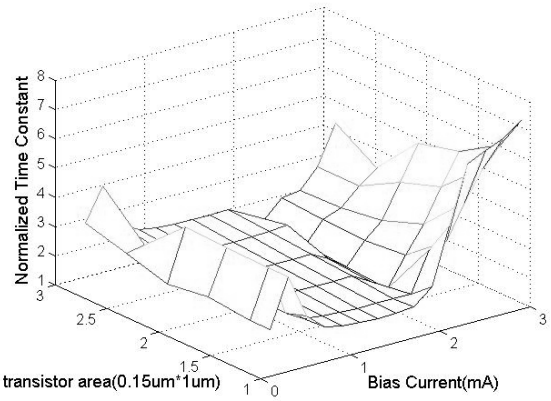


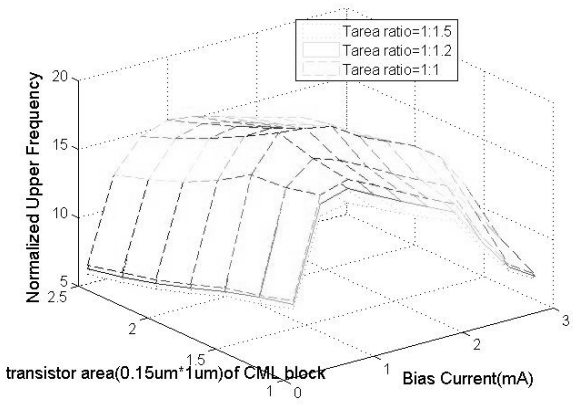
Fig. 9. Normalized time constant versus bias current and Tr. area.

this model as a function of bias current and transistor emitter area in Fig. 9. When the value of the load capacitance increase, initial condition of this model changes, leading the large signal trans-conductance to a different initial value. In the other word, the trend of trans-conductance on the load capacitance induces a non-monotone change.

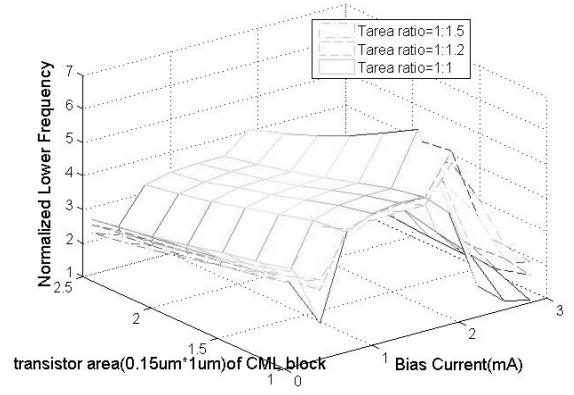
III. BAND-WIDTH AND POWER CONSUMPTION OPTIMIZATION

To accurately describe the interaction between the various concerned performances, it is necessary to present a combined mode analysis. Normalized propagation delay and normalized time constant are shown as a function of transistor area and bias current in Fig. 5 and Fig. 9, respectively, which is under the premise of static loading. It means a fixed transistor area, leading to less representativeness in practical than in theoretical analysis. Therefore, a combined analysis based on different transistor area ratios is presented, in which loading varies with transistor area.

Fig. 10(a) and (b) shows the upper and lower frequency, which is derived from the normalized 1/(propagation delay) and 1/(time constant) respectively. It is a function of the transistor area for CML block and bias current at different values of transistor area ratios between CML block and cross-coupled block. The upper frequency trend demonstrates a monotonically decrease as predicted in the analysis of sensing mode. Nevertheless, the lower frequency exhibits a more complex change. When the cross-coupled block is biased at low current, the lower



(a)



(b)

Fig. 10. (a) Normalized upper frequency, (b) Normalize lower frequency, versus bias current and Tr. area at Tr. area ratios=1:1.5, 1:1.2, 1:1.

frequency decreases monotonically as transistor area expands. However, on the contrast, the function at smaller transistor area ratio experiences a more rapid drop. Thus, a smaller transistor area ratio provides a lower frequency under the operation of latching mode in high current.

Thus, the optimization of both transistor areas should consider many design specifications, such as power dissipation, technology limit of process, and operation range, into consideration. For example, taking operation range as the goal of optimization, transistor area ratio of 1/1.2 provides the best performance under the constraint of low power dissipation.

Fig. 11 shows the normalized operating frequency as a function of transistor area in CML block and bias current at the ratio of transistor area of 1/1.2. Obviously, higher time constant for cross-coupled pair, representing a perfect performance at lower operating frequency, may

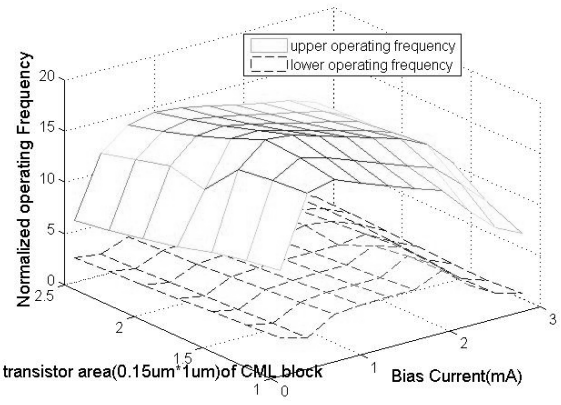


Fig. 11. Normalized operating bandwidth versus Tr. area and bias current at Tr. area ratio equals to 1/1.2.

lead to an unsatisfied upper operating frequency performance, due to larger load capacitor that was introduced by the transistor area of cross-coupled pair. The objective of this paper is to present an optimum bias and device size condition for the bandwidth optimization.

IV. A OPTIMIZED 40 GHZ STATIC FREQUENCY DIVIDER

To verify the proposed method of optimization in bandwidth-related performances, a wide band 40 GHz CML divide-by-2 operates at millimeter wave range is proposed and implemented using SiGe 180 nm technology offer by Tower Jazz. The topology is the conventional type as shown in Fig. 1. But an optimized design flow of RF component in this frequency band in Fig. 12, is followed. This flow provides a complete solution to accommodate the trade-off between the bandwidth and power consumption. Following circuit optimization method, the transistor areas of the differential pair and cross-coupled pair are designed to be 0.15 μm × 1 μm and 0.15 μm × 1.2 μm, respectively. This configuration not only meets the optimized-area ratio for the most broadband operating but also takes the minimum transistor size of the technology into consideration. The reload resistance is set as 140 ohm to make the divider work at 40 GHz with enough output swing and low power consumption.

The frequency divider is integrated with a 50 ohm output buffer for measurement proposes. Fig. 13 shows the die photo of the proposed design. The silicon area of the divide-by-2 is about 79 μm × 55 μm. Measurement is carried out on-wafer using Cascade Elite 300 Probe Station. The input signal is from a signal generator while the output signal is analyzed using a spectrum analyzer.

The measured input sensitivity curve is shown in Fig. 14. Comparing the operation of the design under different bias point, 1.5 ma bias current, which is defined as a

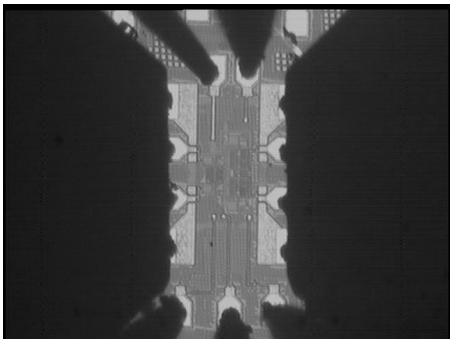


Fig. 13. Die photo.

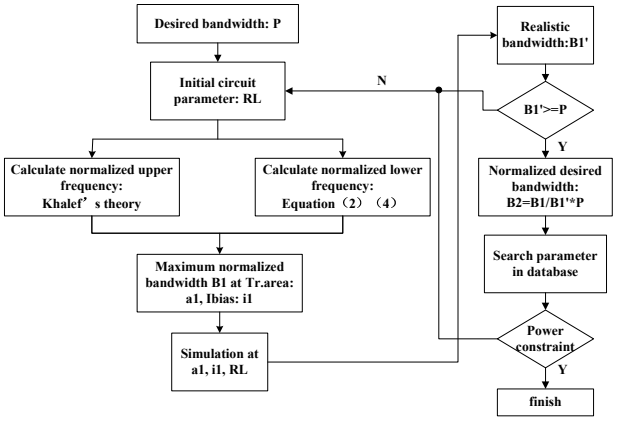


Fig. 12. Flowchart of the overall high-speed frequency divider design.

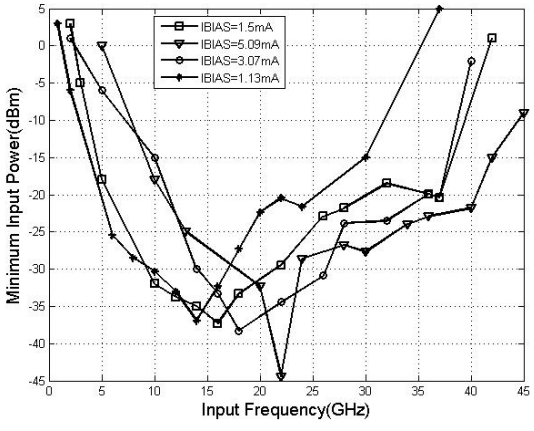


Fig. 14. Measured input sensitivity of the divider.

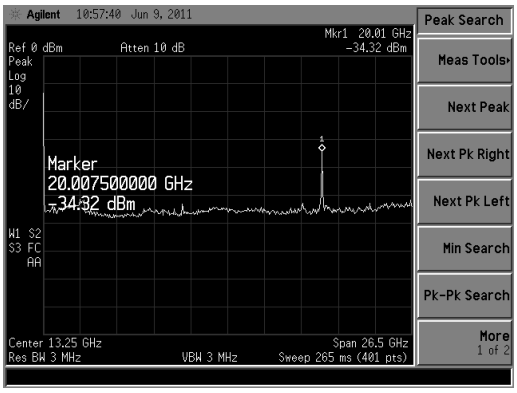


Fig. 15. Spectrum of the 20 GHz output.

Table 1. Comparison with other published results

Reference	Tech (nm)	Fmax (GHz)	PDIS (mW)	Operation Range(GHz)	FOM
[15]	180*	18	1.3	16.5	228.5
[4]	180*	40	31	2.3	2.97
[17]	180*	18	7.2	16	40
[18]	90*	44	5.3	40	332.1
This work	180**	41	2.05	38	760

*CMOS process; **SiGe process

preferred optimized biasing current, provides the broadest bandwidth performance. This measurement effectively verifies the bandwidth optimization method mentioned above.

The 20 GHz output spectrum of the divide-by-2 under a 40 GHz input signal is shown in Fig. 15. To make a fair comparison with literatures, the Figure of Merit (FOM) of the proposed design is calculated as well. The commonly used figure-of-merit (FOM) [19] is defined as below,

$$FOM = \frac{MaximumFrequency(GHz) * \text{Opera}Range(GHz)}{PowerDissipation(mW)}$$

Table 1 shows the FOM of the proposed one compared with other literatures. It can be found that the proposed divider with model analysis provides a remarkable improvement in performances in terms of low power and wide operation range.

V. CONCLUSIONS

This paper reports a new method to optimize bandwidth and power of a static frequency divider. The proposed model of sensing mode and latching mode is based on bipolar SPICE parameters file and can be applied to silicon and HBT process. A combined blocks analysis is presented to provide a more practical design directions. The method not only provides guidelines for a realistic design, but also promotes insight into the behavior of static frequency divider. Various detail impact factor, such as transistor area, bias current, and etc, have been taken into consideration. Based on the proposed method, a divide-by-2 with significant improvements in performances is silicon-verified.

ACKNOWLEDGMENTS

The authors wish to acknowledge the MPW provided by Tower Jazz. This work is supported by National Natural Science Foundation of China under Grant Number 61106034 and 60906017.

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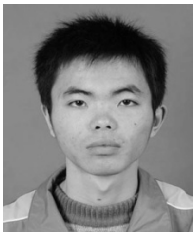

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