http://dx.doi.org/10.5573/JSTS.2012.12.1.18 JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.12, NO.1, MARCH, 2012

# Implementation of Single-Wire Communication Protocol for 3D IC Thermal Management Systems using a Thin Film Thermoelectric Cooler

**Nam-Jae Kim*, Hyun-Ju Lee*, and Shiho Kim****

*Abstract*—**We propose and implement a single-wire communication protocol for thermal management systems using thin film thermoelectric modules for 3D IC cooling. The proposed single-wire communication protocol connects the temperature sensors, located near hot spots, to measure the local temperature of the chip. A unique ID number identifying the location of each hot spot is assigned to each temperature sensor. The prototype chip was fabricated by a 0.13 µm CMOS MPW process, and the operation of the chip is verified.**

*Index Terms*—**3D IC cooling, thermoelectric cooler, single wire, communication, protocol, hot spot**

## I. INTRODUCTION

3D integration technology has recently been proposed to solve the limitations of delay, bandwidth, and power consumption in interconnects of integrated circuits (ICs) [1-4]. The area of the chips can be reduced by stacking in the z-direction and shortening the total wire length as a mix of vertical and horizontal wires is used [1, 4]. In contrast, heat generation problems are exacerbated [5].

Heat generation in chips is an important issue for systems where such differences can easily cause mismatches between signal levels and bias currents, and thus degrade the performance of the analog circuit and also reduce the noise margins [5].

The size/scale of semiconductor devices has increased rapidly over time, leading to a similar increase in the total consumed power. The total power dissipation was reduced without sacrifices of overall system performance by architecture innovation of multi-core system and supply voltage diet, during the period (a) in Fig. 1. However, power consumption has been growing again due to the increased number of cores on a chip while clock speed and power density have remained almost constant. The performance and power trend at period (b) shows that heat generation problem is more getting worse even though innovation of system architecture and supply voltage reduction. Total power and average power densities of chips are critical, but hot spots where the area is only about 100 × 100 $\mu m^2$ and the local power

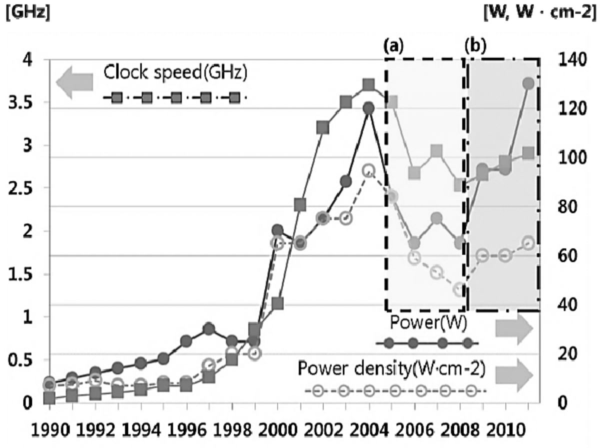


**Fig. 1.** Performance and power trends in the microelectronics [6, 7].

---

Manuscript received Jul. 15, 2011; revised Nov. 11, 2011.

* Department of Electrical Engineering, Chungbuk National Univ.
** School of Integrated Technology and Yonsei Institute of Convergence Technology, Yonsei Univ
E-mail : shiho@yonsei.ac.kr

density approached 600 W·cm$^{-2}$ are more important. The power consumption of a chip is not uniform but is concentrated at the hot spot. Local chip temperatures rise rapidly at the hot spot [8, 9], and these spots can cause reliability problems and increase the overall power consumption due to an increased subthreshold leakage [8].

Hot spot cooling using thermoelectric (TE) devices has attracted the attention of many researchers [6, 8]. The TE device is a solid-state active heat pump that transfers heat from one side of the device to the other against the temperature gradient. The TE cooler (TEC) uses the Peltier effect to create a heat flux between the junctions of two different types of semiconductor materials. This enables the device to manage the operating temperature of an object depending on the power applied to the TEC [10].

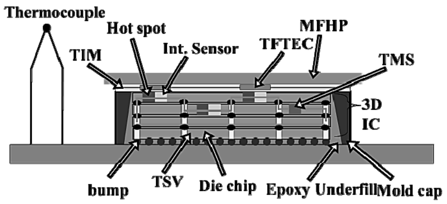
Active cooling using a TEC has recently been reported. When the TEC was powered, the measured temperature in the localized high heat flux region decreased and reached a minimum for a TEC current of about 3 A. On-demand active cooling by the TEC is achieved by powering the device as and when needed [11]. Thus, the TEC power consumption can be reduced. An embedded thin film TEC attached between a die chip and metal plate for Chip-on-Board (CoB) direct assembly has been reported [12].

This paper discusses the implementation of a single-wire communication protocol between the internal sensors for the measurement of the hot spot temperature in real time.

## II. DESIGN AND IMPLEMENTATION OF SINGLE-WIRE COMMUNICATION PROTOCOL

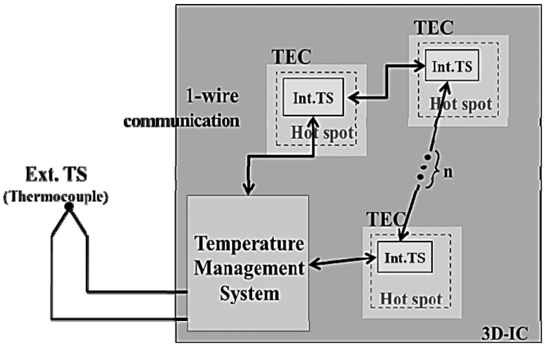
The thermal management system of 3D ICs with a single-wire communication protocol consists of internal and external temperature sensors, TECs, and a thermal management system (TMS) as shown in Figs. 2 and 3. The internal temperature sensor senses the heat generated locally, and the TECs are located near the hot spot. The TMS measures the temperature of each internal sensor. In order to avoid a complex structure, connections between the modules are composed of single wires.

After turning on the power, the TMS automatically measures the temperature of sensors, and the internal temperature is compensated by the difference between the external and the internal sensors. If the temperature of the hot spot is higher than a reference value, the TMS supplies power to the closest TEC to initiate cooling.



**TIM : Thermal Interface Material**
**MFHP : Micro Flat Heat Pipe**
**TFTEC : Thin Film ThermoElectric Cooler**
**TSV : Through-silicon Via**
**TMS : Thermal Management System**

**Fig. 2.** Cross sectional view of the cooling system structure [13].



**※ Int.TS : Internal Temperature Sensor**
**Ext. TS : External Temperature Sensor**

**Fig. 3.** Block diagram of the cooling system.

The internal sensor block consists of three parts as shown in Fig. 4: an RX/TX component, a sensing component to measure the temperature, and a register for storage. We assign unique ID numbers to each module that identifies the location of the hot spots. This location information is then used for active cooling.

The single-wire communication protocol consist of a 2-bit header, a 1-bit command, measured data (8-bit), and a unique ID (N-bit) as shown in Table 1. The sensor block performs two actions in response to “Sensing” and “Read” commands. When the first sensor block receives a sensing command (1XX 000 00000000), the block measures the temperature of the hot spot. The measured data is then stored in the register with a unique ID number and command code (1XX 001 01000110). After storing, the data is transferred to the next sensor block. The operation of next block proceeds in the same order. When the TMS receives the stored data of N-th sensor

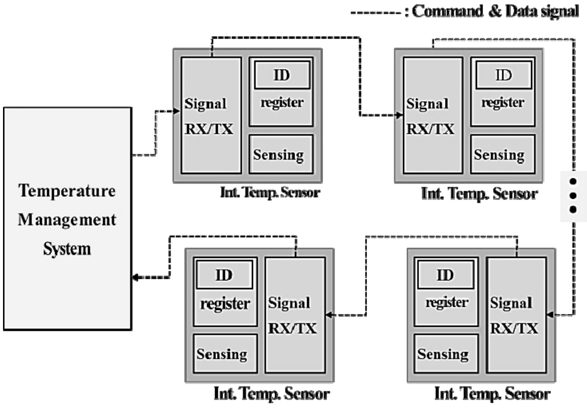


**Fig. 4.** The flow of single-wire communication.

**Table 1.** Single-wire communication command protocol

| Header + Command | ID | Data | Example (ID = 001) |
|---|---|---|---|
| 2bit + 1bit<br>(1XX or 0XX) | N-bit | 8-bit | Commands, ID, data<br>(1XX 001 01000110) |

block, the sensing command is terminated. In the case of a “Read” command (0XX 000 00000000), the first sensor block sends the stored data and command code (0XX 001 01000110) to the next sensor block. The new data (0XX 000 00000000) is then stored in the register. If the TMS receives the original read command (0XX 000 0000000), the command is terminated on N-th read cycle.

## III. EXPERIMENTAL RESULTS

Fig. 5 shows the setup for the measurement. The evaluation board was configured to an alternative environment because the 3D IC structure cooling system is actually difficult to implement. The evaluation board consists of a TMS chip, 4 temperature sensors, and a thermocouple temperature sensor (external sensor). The unique ID of each internal temperature sensor is 000, 010, 011, and 111, respectively.

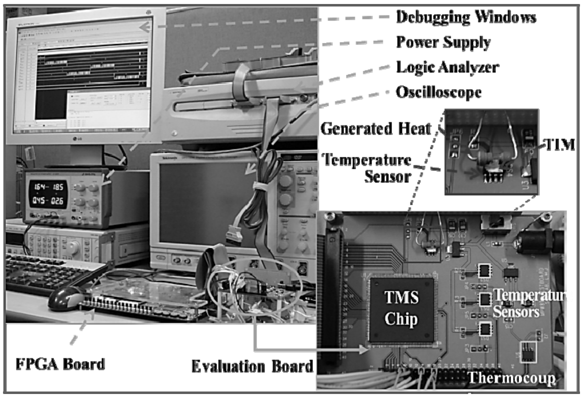


**Fig. 5.** Setup for the measurement.

The TMS chip was designed and fabricated by using a Samsung’s 0.13 μm CMOS process. The chip consists of four internal sensor blocks, and each block is connected by a single wire. The connected temperature sensor on the chip is substituted “sensing” component. The chip area is 4.0 mm × 4.0 mm, but the core area of the chip is about 0.3 mm × 0.3 mm. The operating frequency is 1 MHz.

Fig. 6 shows the block diagram of internal temperature sensor used in the experiment. An accurate current reference using temperature and process compensation current mirror (TPC-CM) is used [14]. The temperature independent reference current is generated by summing PTAT (proportional to absolute temperature) current and CTAT (complementary to absolute temperature) current. The temperature coefficient and magnitude of the reference current are influenced by the process variation. To calibrate the process variation, the proposed TPC-CM uses two binary weighted current mirrors which control the temperature coefficient and magnitude of the reference current. After the PTAT and CTAT currents are measured, the switch codes of the TPC-CM are fixed in order that the magnitude of reference current is independent to temperature. The area of the internal temperature sensor is 0.72 mm × 0.08 mm [14].

The input/output chip signals were measured by a logic analyzer and temperature data from the fabricated TMS were displayed on the PC monitor. We placed a heating resistor below a temperature sensor having ID of 001) to make a hot spot.

The temperature sensor has a range of −55 to +125°C with a resolution of ±0.5°C. As a response of a starting

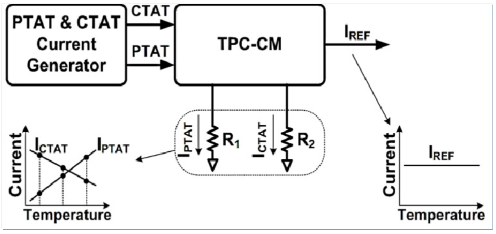
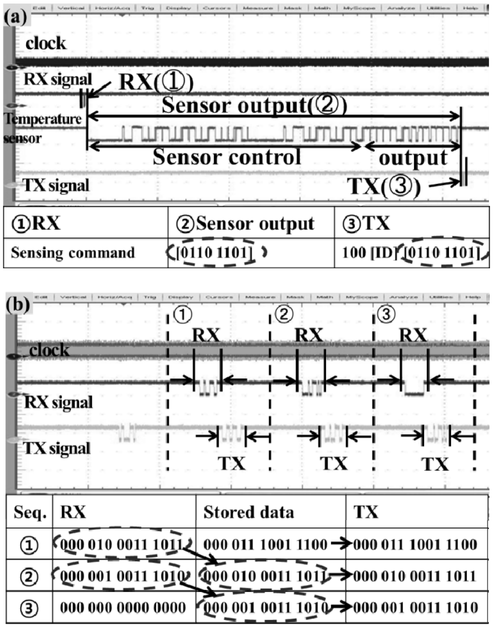


**Fig. 6.** The block diagram of internal temperature sensor of the chip [14].



| ①RX | ②Sensor output | ③TX |
|---|---|---|
| Sensing command | [0110 1101] | 100 [ID] [0110 1101] |

| Seq. | RX | Stored data | TX |
|---|---|---|---|
| ① | 000 010 0011 1011 | 000 011 1001 1100 | 000 011 1001 1100 |
| ② | 000 001 0011 1010 | 000 010 0011 1011 | 000 010 0011 1011 |
| ③ | 000 000 0000 0000 | 000 001 0011 1010 | 000 001 0011 1010 |

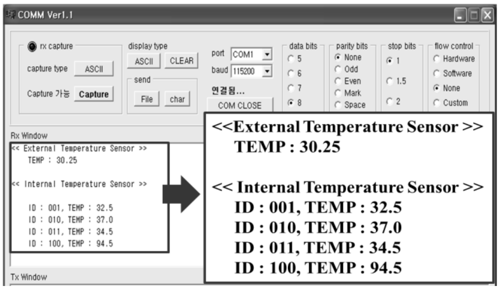
**Fig. 7.** Measured waveforms for (a) “Sensing,” and (b) “Read” commands.

signal from the TMS, the sensor in the fabricated evaluation board measures the hot spot temperature and store it to the internal register.

We checked the proper operation of “Read” and “Sensing” commands. Fig. 7 shows the measured waveforms when we apply “Sensing” and “Read” command to the chain of sensor block in the fabricated evaluation board. Fig. 7(a) shows waveform of internal temperature sensor having ID of (100), when the RX part of the sensor receives “Sensing” command. The sensor measures the temperature of the hot spot, then, the measured data(0110 1101) is stored in the internal register with sensor ID(100) and command code(100). The TX part of the sensor block sends stored data (100 100 0110 1101) to next sensor block.

Fig. 7(b) shows the waveform of internal temperature sensor(ID : 011), when the RX part of the sensor receives “Read” command. In the cycle ①, the stored data(000 011 1001 1100) is transmitted to next block, and the incoming data(000 010 0011 1011) is stored in the register. In the next cycle ②, RX receives “Read” command(000 001 0011 1010), the stored data (000 010 0011 1011) is immediately transmitted to next block, and incoming data(000 001 0011 1010) is stored in a register.

Fig. 8 shows measured temperature data displayed on the PC monitor, and Fig. 9 shows an infrared image of the evaluation board when hot spot of ID 100 is heated. As we can see, there is good agreement between the two data sets.



port COM1
baud 115200
data bits ○ 5 ○ 6 ○ 7 ● 8
parity bits ● None ○ Odd ○ Even ○ Mark ○ Space
stop bits ● 1 ○ 1.5 ○ 2
flow control ○ Hardware ○ Software ● None ○ Custom

```
<< External Temperature Sensor >>
  TEMP : 30.25

<< Internal Temperature Sensor >>

  ID : 001, TEMP : 32.5
  ID : 010, TEMP : 37.0
  ID : 011, TEMP : 34.5
  ID : 100, TEMP : 94.5
```

<<External Temperature Sensor >>
TEMP : 30.25

<< Internal Temperature Sensor >>
ID : 001, TEMP : 32.5
ID : 010, TEMP : 37.0
ID : 011, TEMP : 34.5
ID : 100, TEMP : 94.5

**Fig. 8.** Measured temperature data displayed on the PC monitor.

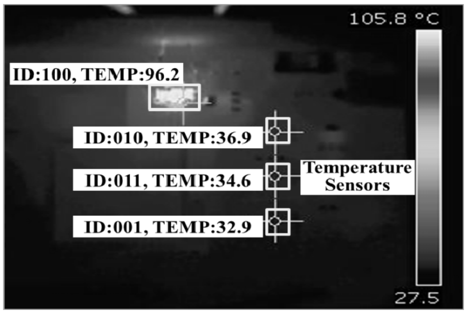


**Fig. 9.** Infrared image of the evaluation board when the resistor is powered.

## IV. CONCLUSIONS

We have proposed and implemented a single-wire communication protocol for TMS with a thin film thermoelectric module for 3D IC cooling. The chip was designed and fabricated by using a Samsung 0.13 μm CMOS process. The test board was fabricated using the chip, and the operation of the chip was verified.

The proposed single-wire communication protocol is designed to measure the temperature during operation of the circuit. The internal sensor interface, connected by a single wire, measures the temperature at all hot spots. The TEC is cooled by the measured temperature.

## ACKNOWLEDGMENTS

This research was supported in part by the MKE, Korea, under the “IT Consilience Creative Program” support program supervised by the NIPA (NIPA-2010-

C1515-1001-0001), and by the IT R&D program of MKE/KEIT. [KI002134, Wafer level 3D IC Design and Integration]. The authors thank IDEC for supporting EDA tools and MPW shuttle service.

## REFERENCES

[1] "International Technology Roadmap for Semiconductors (ITRS)," Semiconductor Industry Association 2007.

[2] F. Zanini, M. M. Sabru, D. Atienza, D. Michieli, "Hierarchical Thermal management Policy for High-Performance 3D Systems With Liquid Cooling," *IEEE Journal of Emerging and Selected Topics in Circuits and systems*, Early Access. Doi:10.1109/JETCAS.2011.2158272.

[3] R. J. Gutmann, A. Y. Zeng, S. Devarajan, J. -Q. Lu, and K. Rose, "Wafer Level 3-Dimensional Monolithic Intergration for Interllignet Wireless Termianls," *Journal of Semiconductor Techonology and Science*, Vol.4, No.3, pp.196-203, Sep., 2004.

[4] Hyewon Kim, Dongchul Kim, and Yungseon Eo, "Experimental Characterization and Signal Integrity Verification of Interconnect Lines with Inter-layer Vias," *Journal of Semiconductor Techonology and Science*, Vol.11, No.1, pp.15-22, Mar., 2011.

[5] M. Pedram, and S. Nazarian, "Thermal modeling, analysis and management in VLSI circuits : principles and methods," *Proceedings of the IEEE*, Vol.94, No.8, pp.1487-1501, Aug., 2006.

[6] A. Majumdar. "Thermoelectric devices : helping chips to keep their cool," *Nature Nanotechnology*, Vol 4, pp.214-215, Jan., 2009.

[7] E. Pop, S. Sinha, and K. E. Goodson, "Heat generation and transport in nanometer-scale transistors," *Proceedings of the IEEE*, Vol.94, Issue. 8, pp.1587-1601, Aug., 2006.

[8] G. J. Snyder, M. Soto, R. Alley, D. Koester, and B. Conner, "Hot Spot Cooling Using Embedded Thermoelectric Coolers," *22nd Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, pp.135-143, 2006.

[9] R. Mahajan, C-P. Chiu, and G. Chrysler, "Cooling a Microprocessor Chip," *Proceedings of the IEEE,* Vol.94, Issue. 8, pp.1476-1486, Aug., 2006.

[10] L. E. Bell, "Cooling, Heating, Generating Power, and Recovering Waste Heat with Thermoelectric Systems," *Science*, Vol.321, pp.1457-1461, 2008.

[11] I. Chowdhury, R. Prasher, K. Lofgreen, G. Chrysler, S. Narasimhan, R. Mahajan, D. Koester, R. Alley and R. Venkatasubramanian, "On-chip cooling by superlattice-based thin-film thermoelectrics," *Nature Nanotechnology*, Vol.4, pp.235-238, Jan., 2009.

[12] S. Kim, H. Lee, N. Kim and J. Yoo, "A thin film thermoelectric cooler for Chip-on-Board assembly," *IEICE Electronics Express*, Vol.7, No.21, pp.1615-1621, Nov., 2010.

[13] N. Kim, Y. Gim, J. Jung, and S. Kim, "The Cooling system of 3-Dimensional integrated circuits using Thin Film Thermoelectric Cooler," *The 30th International Conference on Thermoelectrics*, Jul., 17-21, 2011, Traverse city, MI, USA.

[14] B. Yang, Y. Shin, J. Lee, Y. Lee, and K. Ryu, "An Accurate Current Reference using Tmperature and Process Compensation Current Mirror," *IEEE Asian Solid-State Circuits Conference*, Nov., 16-18, 2009, Taipei, Taiwan.

**NamJae Kim** received the B.S. degrees in the Department of Electrical Engineering from Chungbuk National University, Cheongju, Korea, in 2010. He is currently pursuing the M.S. degree in Department of Electrical Engineering from Chungbuk National University. He has worked at Yonsei University as a research assistant and participated in 3DIC cooling projects since 2011. His current interests include cooling system of 3D IC, thermal management system and analog circuit design.

**HyunJu Lee** received the B.S. and M.S. degrees in Electrical Engineering from Chungbuk National University, Cheongju, Korea, in 2009 and 2011, respectively..

He is currently working for Hynix semiconductor. His research interests include 3D IC, and NAND flash reliability algorithm.

**Shiho Kim** is a professor in the school of integrated technology at Yonsei University, where he is a vice-director of Yonsei Institute of Convergence Technology(YICT). He received the B.S. degree in Electronic Engineering from Yonsei University in 1986, and M.S. and Ph.D. degrees in Electrical Engineering from KAIST in 1988 and 1995, respectively. From 1986 to 1991, and 1995 to 1996, he worked at LG Semicon Ltd., where he involved in design projects of DRAM and Flash memories. From 2005 to 2010, he was a professor at Chungbuk National University. In 2009, he found RAVERS(Research center for Advanced Hybrid Electric Vehicle Energy Recovery System) which is a government supported IT research center. His main research interests include cooling system of 3DIC, vehicular electrics and HVAC system of next generation electric vehicles, and seamless transportation system. He has been an A-SSCC technical program chair of student design contest since 2008. He is a member of IEEK, IEICE and a senior member of IEEE.