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Soft Switching Bridgeless PFC Buck Converters

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Abstract

Based on the standards that limit the harmonic pollution of electronic systems, the use of PFC converters is mandatory. In this paper, a new resonant bridgeless PFC converter is introduced. By eliminating the input bridge diodes, the efficiency is improved. Moreover, soft switching conditions for all of the semiconductor elements are achieved without adding any extra switches. As a result, high efficiency is attained. The proposed converter is analyzed and the theoretical and simulation results of the proposed converter are presented. In order to verify the validity of the analysis, a 40 w prototype converter is implemented and experimental results are presented. The experimental results show that high efficiency is attained while achieving a high power factor.

Key words: Bridgeless PFC, Power Factor Correction (PFC), Resonant converter, Soft switching

I. INTRODUCTION

Nowadays, electronic devices are applied in vast numbers. In order to provide constant voltage to electronic devices, diode rectifiers are usually used. By applying more and more diode rectifiers for converting input AC voltage into DC voltage, harmonic pollution will increase drastically [1]. To overcome this problem, standards like IEC61000-3-2 have been enacted [2]. To satisfy these standards, employing power factor correction circuits is unavoidable. Usually, conventional PFC converters apply a boost converter to increase the power factor. Fig.1 (a) shows a block diagram of a conventional power supply with a PFC stage. Using PFC converters as extra stages will result in high power losses and low efficiency [3].

To improve the efficiency of AC-DC converters, two methods have been proposed in the literature. The first method is the bridgeless PFC converter. In bridgeless PFC converters, the PFC converter is combined with input rectifier diodes. The schematic of a bridgeless PFC converter is shown in Fig.1 (b) [3-7]. The other method is the so-called single stage PFC converter (S^2PFC). In a S^2PFC, the PFC stage and the DC-DC converter are integrated. In this method, although the applied topology is simpler and has fewer semiconductor elements the switch current and the voltage rating are high. This method is widely used in medium and low power applications. The schematic of a S^2PFC converter is shown in Fig.1(c).

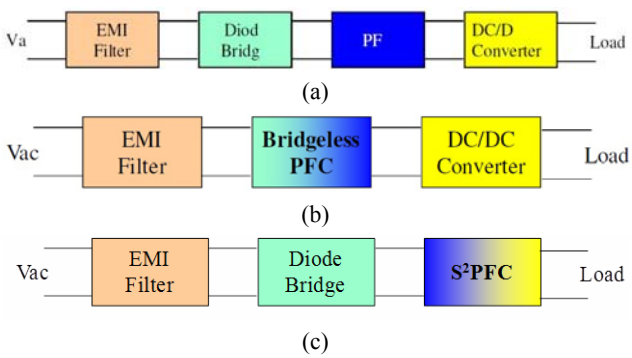

Fig. 1. (a) Conventional Power supply with PFC. (b) Power supply with bridgeless PFC. (c) Power supply with S^2PFC.

For higher power applications, a bridgeless PFC boost converter is usually applied. The converter is followed by an isolated stage to reduce the high output voltage of the PFC stage and to achieve tight regulation. When isolation is not necessary, a PFC buck converter is a better choice. The output voltage of a PFC buck converter is low enough that an isolated DC/DC converter is not required to attain the required voltage gain. Several studies have been carried out to improve the efficiency of PFC buck converters.

In [8], a current source buck converter with coupled inductors is applied as a PFC converter. However, due to the CCM operation, the control circuit is complex. Employing large inductors and hard switching are the other disadvantages of this converter. In [9], a bridgeless buck converter was introduced which is also hard switched and

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thus the operating frequency is limited. DCM converters are widely applied for power factor correction due to their inherent PFC capability [10]. Also, in order to improve power converters efficiency, soft switching techniques are usually applied [10]-[13]. Soft switching techniques reduce the switching losses and electromagnetic interferences as well as the converter volume and weight [6] and [10].

In this paper, a new bridgeless PFC buck converter is introduced. Due to the resonant operation of the converter, a high switching frequency can be achieved. As a result, the value of the passive elements is small. Therefore, the volume and net weight of the converter are low. The soft switching condition is achieved without any auxiliary switches due to the resonant operation of the converter which results in a high current peak through the switches. Furthermore, the proposed converter exhibits inherent PFC due to the DCM operation. In the next section, the operation principles are explained and the theoretical analysis is presented. In section III, the design considerations are introduced. The converter is designed for a 110 V_{RMS} AC input voltage, a 30 V_{DC} output voltage and a 40 watt nominal load. The simulation results are presented in section IV to show the validity of the theoretical analysis. A prototype of the proposed converter with the mentioned specifications is implemented and the experimental results are presented in the fifth section to verify the validity of the analysis and simulations.

II. Proposed Soft Switching Bridgless Circuit Operation

The proposed PFC converter is shown in Fig. 2(a). The converter is composed of two unidirectional switches S_{m1} and S_{m2}, four diodes D_a, D, D_1 and D_2, two resonant inductors L_m and L_a and a resonant capacitor C_r. The capacitor C is also employed as an output filter. In order to simplify the converter analysis, it is assumed that the converter is operating in the steady state and that all of the circuit elements are ideal. In addition, the output capacitance is assumed to be sufficiently large to be considered as an ideal DC voltage source (V_{Out}), as shown in Fig. 2(b). In Fig. 2(b), depending on the line voltage polarity, S_m can be either S_{m1} or S_{m2}. Furthermore, the input voltage is assumed constant and equal to V_s in a switching cycle.

Based on the above assumptions, the circuit operation in a switching cycle can be divided into five modes, as shown by the equivalent circuits in Fig. 3. Also, the converter theoretical waveforms are illustrated in Fig. 4. Prior to the first mode, it is assumed that all of the semiconductor devices are off, the C_r voltage is $-V_{out}$ and the capacitor C is providing the load current.

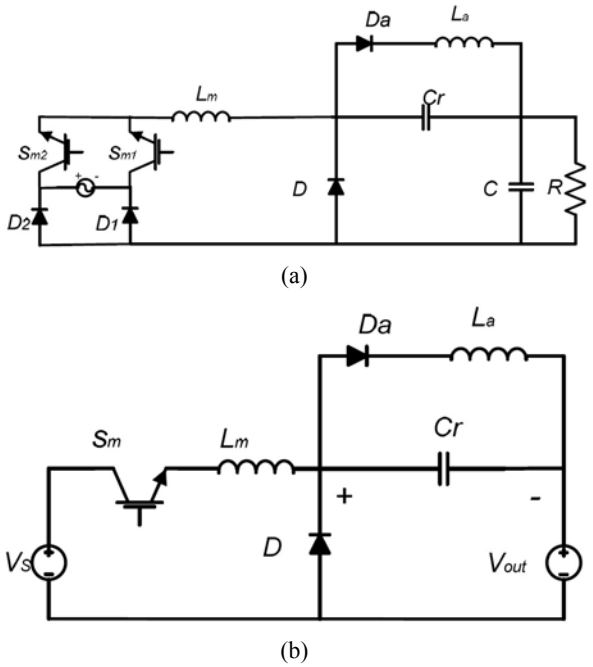


Fig. 2. (a) Proposed bridgeless PFC. (b) Equivalent circuit of the proposed PFC in a switching cycle.

➢ Mode I [$t_1 - t_2$] (Fig. 3(a))

At t_1, S_m is turned on under zero current switching (ZCS) and C_r charges through a resonance with L_m. Thus, the C_r voltage increases in a resonant fashion. When V_{Cr} reaches zero, D_a turns on under zero voltage zero current switching (ZVZCS).

$$i_{Lm}(t) = \frac{V_S}{Z_1}\sin(\omega_1(t-t_1)) \tag{1}$$

$$v_{Cr}(t) = V_S - V_{out} - V_S\cos(\omega_1(t-t_1)) \tag{2}$$

where

$$Z_1 = \sqrt{\frac{L_m}{C_r}} \tag{3}$$

$$\omega_1 = \frac{1}{\sqrt{L_m C_r}} \tag{4}$$

$$v_{Cr}(t_2) = 0 \tag{5}$$

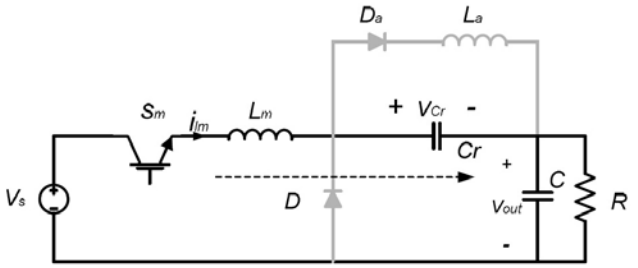
$$t_2 - t_1 = \frac{1}{w_1}\cos^{-1}\left(\frac{V_S - V_{out}}{V_S}\right) \tag{6}$$

➢ Mode II [$t_2 - t_3$] (Fig. 3(b))

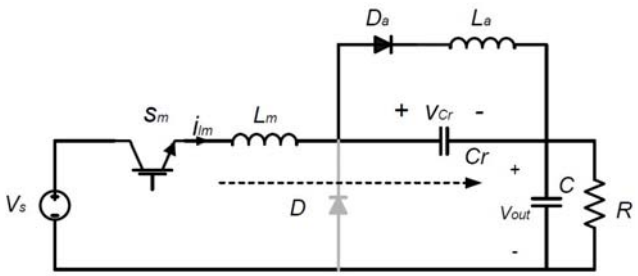
At t_2, D_a turns on and L_a is added to the resonant circuit. Therefore, during this mode C_r is charged through L_m and is discharged through L_a. Important equations for this mode are:

$$v_{Cr}(t) = A\sin\omega_2(t-t_2) + B\cos\omega_2(t-t_2) + \frac{V_S - V_{out}}{L_m C_r \omega_2^{\,2}} \tag{7}$$

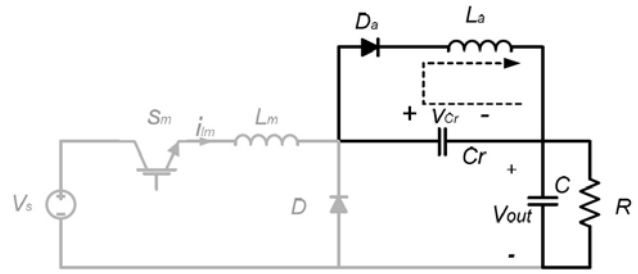
$$i_{Cr}(t) = \omega_2 C_r A\cos\omega_2(t-t_2) - w_2 C_r B\sin\omega_2(t-t_2) \tag{8}$$



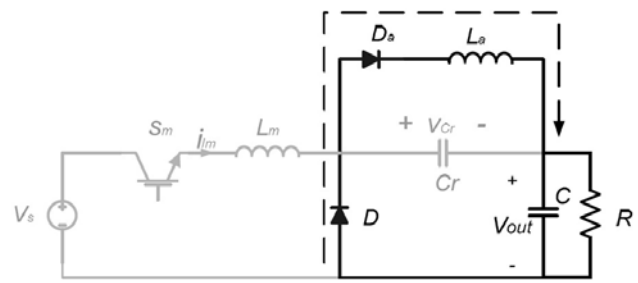
(a) Mode I



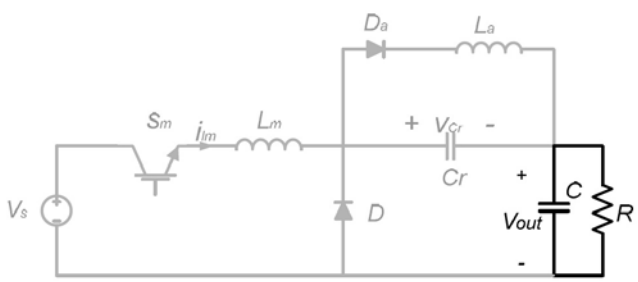
(b) Mode II



(c) Mode III



(d) Mode IV



(e) Mode V

Fig. 3. Equivalent circuit for each operating mode.

$$\omega_2^{\ 2} = \frac{1}{L_a C_r} + \frac{1}{L_m C_r} \tag{9}$$

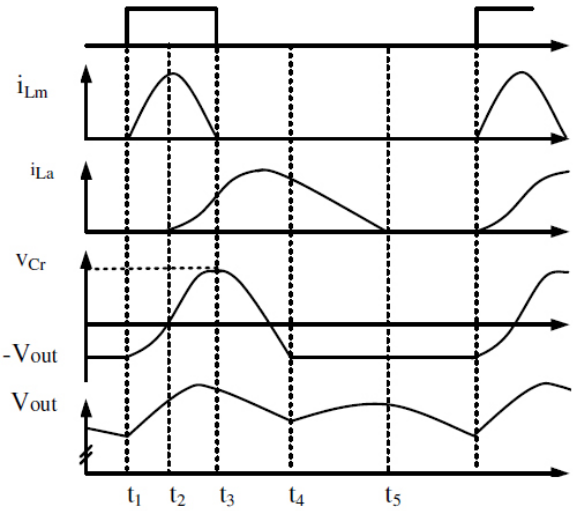


Fig. 4. Steady state waveforms of converter.

$$B = -\frac{V_S - V_{out}}{L_m C_r \omega_2^{\ 2}} \tag{10}$$

$$A = \frac{i_{Lm}(t_2)}{C_r \omega_2} \tag{11}$$

$$i_{Lm}(t_2) = \frac{V_S \sin(\omega_1(t_2 - t_1))}{Z_1} \tag{12}$$

$$i_{Lm}(t) = A(C_r\omega_2 + \frac{-1}{L_a w_2})\cos(\omega_2(t-t_2)) - B(C_r\omega_2 - \frac{1}{L_a\omega_2})\sin(\omega_2(t-t_2)) - \frac{B}{L_a}(t-t_2) + \frac{A}{L_a\omega_2} \tag{13}$$

$$i_{Lm}(t) = \sqrt{C^2 + D^2}\,\sin(\omega_2(t-t_2)+\phi) - \frac{B}{L_a}(t-t_2) + \frac{A}{L_a\omega_2} \tag{14}$$

$$C = A(C_r\omega_2 + \frac{-1}{L_a\omega_2}) \tag{15}$$

$$D = -B(C_r\omega_2 - \frac{1}{L_a\omega_2}) \tag{16}$$

$$\varphi = \sin^{-1}(\frac{C}{\sqrt{C^2 + D^2}}) \tag{17}$$

In order to turn S_m off under ZCS condition, I_{Lm} should reach to zero during this mode. Therefore, the first term of equation (14) should become negative. Therefore:

$$\sin(\omega_2(t-t_2)+\phi) < 0 \tag{18}$$

$$\pi < \omega_2(t-t_2)+\phi < 2\pi \tag{19}$$

$$(t-t_2) > \frac{\pi-\phi}{\omega_2} \tag{20}$$

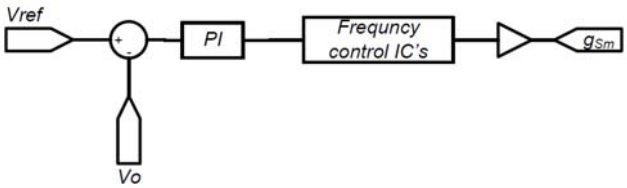
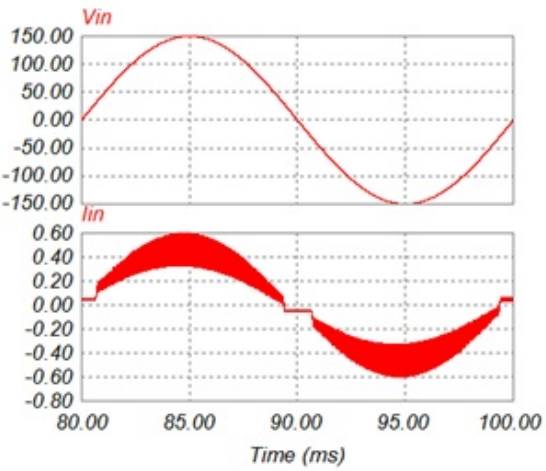
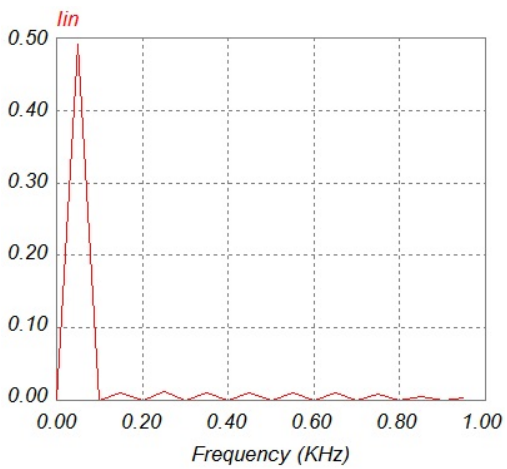


Fig. 5. Control circuit block diagram.



(a)



(b)

Fig. 6. Simulation results. (a) top: line voltage. (V) and bottom: input line current. (A) (b) Input current harmonics.

Also, the sum of the second and third terms of (14) should be less than the amplitude of the first part (sinusoidal coefficient) to guarantee that $I_{Lm}(t)$ will become zero. Thus:

$$\frac{V_S - V_{out}}{L_m L_a C_r \omega_2^2}\left(\frac{3\pi/2-\phi}{\omega_2}\right) + \frac{I_{Lm}(t_2)}{L_a C_r \omega_2^2} \le \sqrt{C^2 + D^2} \qquad (21)$$

At t_3, the main switch current reaches zero and S_m is turned off under ZCS. C_r , L_a and L_m should be designed to guarantee that I_{Lm} becomes zero at t_3.

$$i_{Lm}(t_3) = 0 \qquad (22)$$

$$i_{Cr}(t) = i_{La}(t) \qquad (23)$$

➢ Mode III [$t_3 - t_4$] (Fig. 3(c))

At t_3, the resonance between C_r and L_a continues (with initial values of $V_{cr}(t_3)$ and $I_{La}(t_3)$) and C_r discharges through L_a until its voltage reaches $-V_{out}$. At t_4, the diode D turns on under ZVS and the resonant capacitor voltage remains constant and equal to V_{out}.

$$v_{Cr}(t) = \frac{i_{cr}(t_3)}{C_r \omega_3}\sin\omega_3(t-t_3) + v_{Cr}(t_3)\cos\omega_3(t-t_3) \qquad (24)$$

$$i_{Cr}(t) = i_{Cr}(t_3)\cos\omega_3(t-t_3) - C_r\omega_3 v_{Cr}(t_3)\sin\omega_3(t-t_3) \qquad (25)$$

$$\omega_3 = \frac{1}{\sqrt{L_a C_r}} \qquad (26)$$

Where $i_{Cr}(t_3)$ and $v_{Cr}(t_3)$ can be calculated from equations (7) and (8).

➢ Mode IV [$t_4 - t_5$] (Fig. 3(d))

At t_4, the diode D turns on under ZVS and the L_a energy is transferred to the load and its current linearly decreases to zero.

$$t_5 - t_4 = \frac{L_a}{V_{out}} \times i_{Cr}(t_4) \qquad (27)$$

where $I_{cr}(t_4)$ can be obtained from equation (24).

➢ Mode V [$t_5 - t_6$] (Fig. 3(e))

At t_5, diodes D_a and D turn off under ZCS. In this interval the load is supplied by the output capacitor.

III. Design Procedure

Based on the theoretical analysis of the proposed converter in the previous section, the design considerations are explained in four steps.

A. Resonant elements (L_a, L_m and C_r)

In order to simplify the analysis, it is assumed that $L_a >> L_m$. Thus the relation between the power transferred to the load and the frequency in a switching cycle can be approximated with following equation:

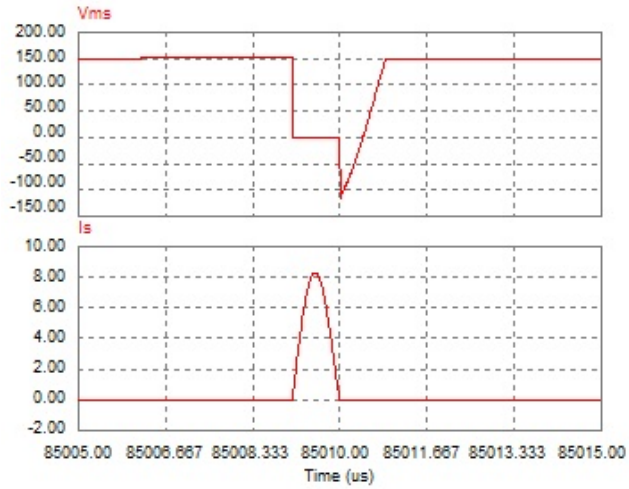


Fig. 7. Simulation results of current (A) and voltage (V) of S_m .

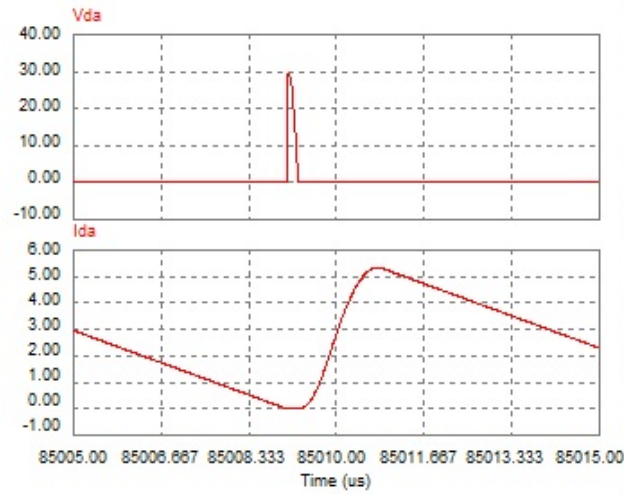


Fig. 8. Simulation results of Current (A) and voltage (V) of D_a .

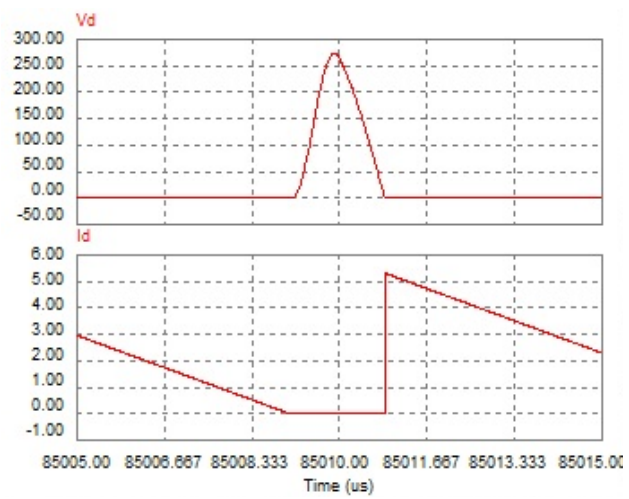


Fig. 9. Simulation results of Current (A) and voltage (V) of diode D.

$$\varepsilon_{in,s} = \int_{t_1}^{t_6} V_S \times i_{Lm}(t)dt = \int_{0}^{\omega_1 t=\pi} V_S \frac{V_S}{Z_1}\sin(\omega_1 t)dt = 2C_r V_S^{\,2} \quad (28)$$

$$p_{in,s} = 2C_r V_S^{\,2} f_{sw} \quad (29)$$

where $P_{in,s}$ is the average input power in a switching cycle.

The input voltage is varied by line frequency. Therefore, the average input energy is:

$$p_{in,avg} = \int_{0}^{wt=\pi} 2C_r f_{sw} V_m^2 \sin^2(wt)dt = f_{sw} C_r V_m^{\,2} \quad (30)$$

$$P_{\text{out}} = \eta P_{in} \quad (31)$$

where η and ω are the converter efficiency and the input line frequency, respectively.

$$C_r = \frac{P_{out}}{\eta f_{sw} V_m^2} \quad (32)$$

Based on the above approximation, the duration of the converter operation modes are approximately equal to:

$$\alpha_1 = t_3 - t_1 \approx \pi\sqrt{L_m C_r} \quad (33)$$

$$\alpha_2 = t_4 - t_3 \approx \frac{\pi\sqrt{L_a C_r}}{2} \quad (34)$$

$$\alpha_3 = t_5 - t_4 \approx \frac{L_a I_{La,P}}{V_O} \quad (35)$$

where $I_{La,p}$ is the auxiliary inductor peak current. In the steady state, the average of the resonant capacitor current is zero. Therefore, the average of the output current is equal to the average of the auxiliary inductor current. Therefore:

$$I_{La,avg,MAX} = I_{O,avg,MAX} = \frac{P_{O,MAX}}{V_O} \quad (36)$$

The auxiliary inductor average current can be approximately calculated using the following equation:

$$I_{La,avg,MAX} \approx I_{La,p} \frac{\frac{L_a I_{La,P}}{V_O} + \frac{\pi\sqrt{L_a C_r}}{2}}{2(\alpha_3 + \alpha_2 + \alpha_1)} = \frac{1}{2} I_{La,p} f_{sw,MAX} \left(\frac{L_a I_{La,P}}{V_O} + \frac{\pi\sqrt{L_a C_r}}{2} \right) \quad (37)$$

The converter maximum switching frequency can be calculated using (33), (34), (35) and (37).

$$T_{sw} = \frac{1}{f_{MAX}} > \alpha_1 + \alpha_2 + \alpha_3 \quad (38)$$

C_r should be designed by considering the converter maximum power (32). L_m and L_a are chosen to meet the desired switching frequency (equation (38)).

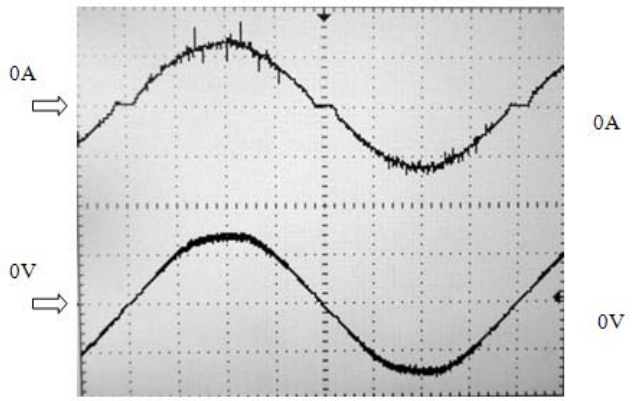


Fig. 10. Top: input line current (0.4A/div) and bottom: input line voltage (100V/div and time scale is 2.5ms/div).

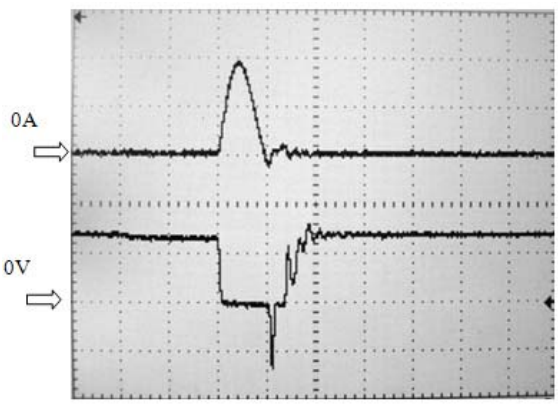


Fig. 11. Current and voltage of S_m (time scale is 1μs/dv). Top: Current waveform (4A/div) Bottom: Voltage waveform (100V/div).

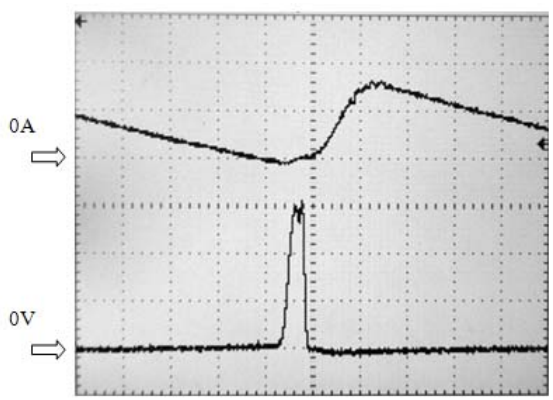


Fig. 12. Current and voltage of D_a (time scale is 1μs/dv). Top: Current waveform (4A/div) Bottom: Voltage waveform (10V/div).

B. Semiconductor elements ratings (S_m, D_a and D)

The peak current and the voltage stresses are obtained from following equations:

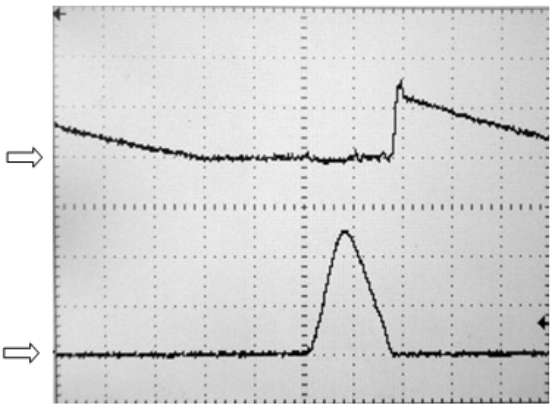


Fig. 13. Current and voltage of diode D (time scale is 1μs/dv). Top: Current waveform (4A/div) Bottom: Voltage waveform (100V/div).

$$I_{SWm,MAX} = \frac{V_S}{Z_1},\ V_{SWm,MAX} = V_s \tag{39}$$

$$I_{D,MAX} << I_{La,p}\ ,V_{D,MAX} = 2V_S \tag{40}$$

$$I_{Da,MAX} = I_{La,p},\ V_{Da,MAX} = V_o \tag{41}$$

C. Input filter

A small filter to reduce the switching frequency harmonics should be applied in series with the line voltage. For this purpose, a small LC filter is suitable.

D. Control circuit

The proposed converter has inherent PFC operation. Therefore, to control this converter, there is no need to control the input current. The controller must control the output voltage at a desired value. To control the proposed converter, conventional frequency controller IC's, like the TL497, can be used. A block diagram of the controller is shown in Fig. 5.

IV. Simulations Results

The proposed converter is designed and simulated by PSIM software. The input and output voltages are $110V_{rms}$ and $30V_{DC}$, respectively. The output power is about 40 W. The circuit frequency is about 110 kHz at a nominal load. The L_a and L_m inductors are 40μH and 5μH, respectively. The resonant capacitor is 15nF. The output capacitor is chosen to be 2200μF for a 1% ripple in the output voltage. A small LC filter is used at the input of the converter to filter the high frequency switching ripple. The values of the filter components are 20μH and 400nF, respectively.

Fig.6(a) shows the input current and voltage under a full load. It can be observed from this figure that the input current is in phase with the input voltage and the total harmonic distortion (THD) is about 0.09 and the power factor (PF) is

about 96%. Fig. 6(b) shows the input current in the frequency domain. It can be observed from this figure that the input current harmonics are below the IEC61000-3-2 standard.

Fig.7 and Fig.8 show the voltage and current of S_m and D_a which indicate that the ZCS condition has been achieved. Fig. 9 shows the current and voltage of the diode D which indicates that the zero voltage switching (ZVS) condition has been achieved.

V. EXPERIMENTAL RESULTS

In order to verify the validity of the theoretical analysis and the simulation results, a 40 W prototype of the proposed converter has been constructed. The same values mentioned in the previous section are used for the resonant elements. The switch and the diode are an IRF640 and a BYW29, respectively. In order to create a unidirectional switch, a MUR460 diode is added in series with S_{m1} and S_{m2}. Fig. 10 shows the waveforms of the line voltage and line current at 110V AC input and 40W output power. Figs. 11-13 show the switching waveforms of semiconductor elements. These waveforms show that the soft switching condition has been achieved for all of the semiconductor elements as explained in the previous sections. The presented experimental results confirm the theoretical analysis and the simulation results provided in the previous sections.

VI. CONCLUSIONS

In this paper, a new soft switching bridgeless PFC circuit is presented. By eliminating the input bridge diodes, the efficiency is improved. Moreover, soft switching conditions for all of the semiconductor elements is achieved without adding any extra switches, which results in a further efficiency improvement. Due to the soft switching, the proposed converter can be employed at higher switching frequencies in comparison to its hard switching counterparts. As a result it can achieve a greater power transfer density. The circuit is implemented and the presented experimental results confirm the theoretical analysis. The measured power factor is about 96%.

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