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레이아웃 기반 온-칩 전력 분배 격자 구조의 인덕턴스 모델 개발 및 적용

(Layout-Based Inductance Model for On-Chip Power Distribution Grid Structures)

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요 약

전원 전압이 낮아지고, 칩의 동작 속도가 빨라짐에 따라 온-칩 인덕턴스를 포함한 power distribution network (PDN) 분석이 중요해 질 것으로 예측된다. 본 논문에서는 일반적인 온-칩 전력 격자 구조에 적용시킬 수 있는 효과적인 인덕턴스 추출 방법에 대해 제안한다. Chip layout에 적용할 수 있는 loop 인덕턴스 모델을 제시하고, 그 모델을 사용하여 post layout RC extraction netlist로 부터 인덕턴스를 포함한 netlist를 추출할 수 있는 tool을 개발하였다. 제안된 loop 인덕턴스 모델과 개발된 tool의 정확성은 회로 simulation을 통해 PEEC 모델과 비교하여 검증하였다. 인덕턴스 추출 방법을 실제 chip layout에 적용시켜 on-chip inductance를 포함한 PDN의 voltage fluctuation을 예측하였다. 패키지와 PCB 모델을 포함한 co-simulation 모델을 구성하여 on-chip inductance의 영향을 분석하였다.

Abstract

With the lower supply voltage and the higher operating frequency in integrated circuits, the analysis of the power distribution network (PDN) including on-chip inductances becomes more important. In this paper, an effective inductance extraction method for a regular on-chip power grid structure is proposed. The loop inductance model applicable to chip layout is proposed and the inductance extraction tool using the proposed inductance model based on post layout RC circuits is developed. The accuracy of the proposed loop model and the developed tool is verified by comparing the test circuit simulation results with those from the partial element equivalent circuit (PEEC) model. The voltage fluctuation from the RLC circuits extracted by the developed tool was examined for the analysis of on-chip inductance effects. The significance of on-chip power grid inductance was investigated by the co-simulation of chip-package-PCB.

Keywords : Layout extraction, inductance, modeling, on-chip power distribution grid, co-simulation

Ⅰ. Introduction

With the advance of process technology, the analysis of power distribution networks becomes more important[1]. In particular, the lower power voltage and the faster transition time result in the critical issue of the inductive voltage drop (Ldi/dt) on power distribution grids[2] as shown in Fig. 1. We

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need to analyze the on-chip inductance effects of power distribution grids in a real-chip environment.

The analysis of a multi-layer interdigitated power and ground network is introduced in [1] including the on-chip inductance of power distribution grids. The significance of on-chip inductance is discussed in [2]. This work presents a inductance screening tool to select interconnects with significant inductance effects. Reference[3] shows that the arrangement of on-chip decoupling capacitors can be determined by analyzing on-chip power distribution networks.

In previous work, the partial equivalent element circuit (PEEC) model[4~5] and the loop inductance model[6~9] were used for on-chip inductance analysis. The PEEC method can be applied to construct a circuit model without predetermination of current loops where the return current paths are unknown in the chip environment[4]. The accuracy is also an advantage of the PEEC model[5]. However, it is difficult to apply in full-chip analysis due to a dense RLC circuit matrix requiring long SPICE simulation times[6]. In addition, it is known that it is difficult to use the PEEC model to analyze the frequency-dependent impedance characteristics[7]. Compared to the PEEC model, the simplicity of the loop model leads to fast simulation times[8], making it applicable in post-layout inductance extraction. The loop inductance model for power grid structure was proposed in [9], however, this model can not be applied to chip layout since it does not consider the 3D structures of power distribution grids. It was not verified against the PEEC model in layout-based simulation. In this paper, we propose an analytical loop inductance model for power distribution grids that is more accurate than the traditional model in that it predicts multiple return current paths.

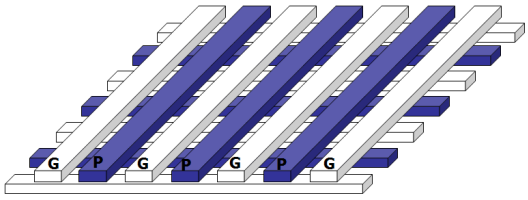


그림 1. 온-칩 전력 분배 격자 구조
Fig. 1. On-chip power grid structure.

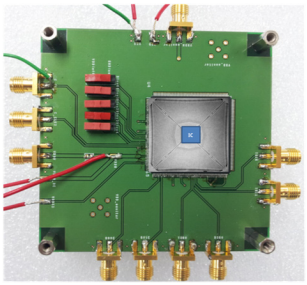


그림 2. 칩-패키지-PCB
Fig. 2. Chip-Package-PCB.

To analyze the power distribution grids of IC chips considering on-chip inductances, a layout-based RLC extraction tool is necessary. Although some extraction tools can perform inductance extraction, the process technology files from foundries are not up to date to support L extractions. In addition, the size of the power/ground grid extraction netlists is too large to be handled. We developed this effective inductance extraction tool using the proposed loop inductance model based on post-layout RC extraction circuits generated by layout extraction tools such as Mentor Graphics' Calibre xRC[10]. By using our inductance extraction tool, we can perform the co-simulation of the chip, package (PKG) and printed circuit board (PCB), as shown in Fig. 2. It can provide a more accurate analysis of power distribution networks considering whole power distribution network structures including PKG and PCB.

Section II describes the proposed loop inductance model for power grid structures and the inductance extraction flow of the developed tool. In Section III, the proposed inductance model is validated by comparing the results with those of the PEEC model and the significance of on-chip power grid inductance is discussed in the context of a layout-based test case. Section IV shows the analysis of on-chip inductance effects from the co-simulation of chip-PKG-PCB using several test models including

on-chip parasitic RC and RLC extraction circuits. Finally, conclusions are summarized in Section V.

Ⅱ. On-chip Inductance Model and Extraction Tool

1. Proposed on-chip loop inductance model for the power grid structure

In Fig. 3(a), the PEEC model includes a mutual inductance model between every two metal line pairs. It has to include $\frac{n(n-1)}{2}$ mutual inductance components for simulation when the number of metal lines is n as shown in Fig. 4. However, the loop inductance model does not need to include mutual inductance components due to the pre-calculation of effective inductances including partial and mutual inductances based on the assumption of current return paths shown in Fig. 3(b). Hence, the loop inductance model is preferable to the PEEC model for simpler modeling and faster simulation.

Figure 4 shows the possible current directions that

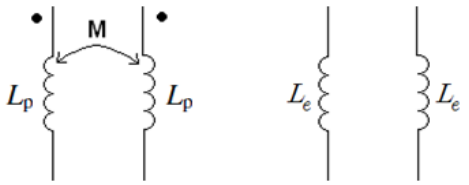


그림 3. 두 라인의 인덕턴스 모델:
(a) PEEC 모델, (b) Loop 모델
Fig. 3. Inductance models of two lines:
(a) PEEC model, (b) Loop model.

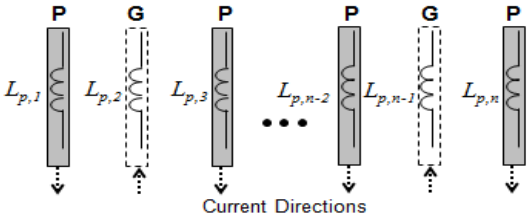


그림 4. n개 라인을 가진 Interdigitated power/ground 라인들의 전류 방향 예측
Fig. 4. Assumption of the current direction in the number of n parallel metal lines.

can occur in parallel power/ground metal lines. These current directions are based on the assumption that the switching circuit is connected to the nearest power and ground location, respectively, and hence the current directions of power and ground lines are opposite[8]. The loop inductance is calculated as in (1), where L_p is the partial inductance and M is the mutual inductance. The equation of the effective inductance is proposed as in (2) by dividing the loop inductance by the number of parallel metal lines, n.

$$L_{loop} = L_{p,tot} + M_{loop} = \sum_{i=1}^{n} L_{p,i} + \sum_{k=2}^{n}\sum_{i=k}^{n} (-1)^{k+1} M_{(n-i+k),(n-i+1)} \quad (1)$$

$$L_e(n) = \frac{L_{loop}}{n} = \sum_{i=1}^{n} \frac{L_{p,i}}{n} + \sum_{k=2}^{n}\sum_{i=k}^{n} \frac{(-1)^{k+1} M_{(n-i+k),(n-i+1)}}{n} \quad (2)$$

The partial and mutual inductance formulae are (3) and (4) where l is the length, w is the width, t is the thickness of the metal line and d is the distance between two parallel lines[11].

$$L_p = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.2235(w+t)}{l}\right] \quad (3)$$

$$M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{d} + \sqrt{1+\frac{l^2}{d^2}}\right) - \sqrt{1+\frac{d^2}{l^2}} + \frac{d}{l}\right] \quad (4)$$

The assumption of current direction shown in Fig.

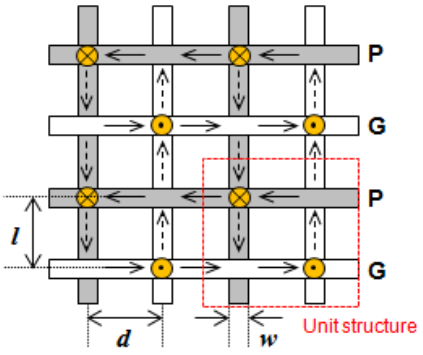


그림 5. 전력 분배 grid 구조에서의 전류방향 예측
Fig. 5. Assumption of the current direction in the power distribution grid structure.

4 can be applied to the interdigitated power distribution grids as depicted in Fig. 5. In power distribution grids, it can be assumed that the distance to two return current paths is length l due to the via locations and the metal crossing points. The effective inductances of grid structures can be derived from (2) as in Equation (5). The mutual inductance formula shown in (4) is modified by replacing d with ml. It is expressed by the function of m, where m is the product constant of the distance between two metal lines as (6).

$$L_e(n) = L_p + \sum_{m=1}^{n-1} \frac{(-1)^m (n-m) \times M(m)}{n} \quad (5)$$

$$M(m) = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{1}{m} + \sqrt{1+\frac{1^2}{m^2}}\right) - \sqrt{1+m^2} + m\right] \quad (6)$$

$$L_{grid} = 2 \times L_e(n) \quad (7)$$

However, the resistances of the grid structures extracted by 'Calibre xRC' are located between two vias where the line length is $2l$. To arrange RLC equivalent circuits of grid structures, the inductances have to be located between two vias as shown in Fig. 5. For this reason, the grid inductances of extracted RLC networks, L_{grid}, are twice the effective inductance, L_e, expressed as in (7), where n is the number of parallel metal lines of the grid structures.

2. Inductance extraction flow

The chip layout design with the on-chip interdigitated power grid is shown in Fig. 6(a). It is designed by Magnachip/Hynix 0.18 um process (1.8 V). The on-chip power grid structures are located in the top two metals, metal 5 (M5) and thick metal (TKM). The RC extraction circuit of the grid structure generated by 'Calibre xRC' from the layout is described as in Fig. 6(b). It includes not only the resistances and capacitances of grid metal lines, but also the resistances of the vias connecting the two

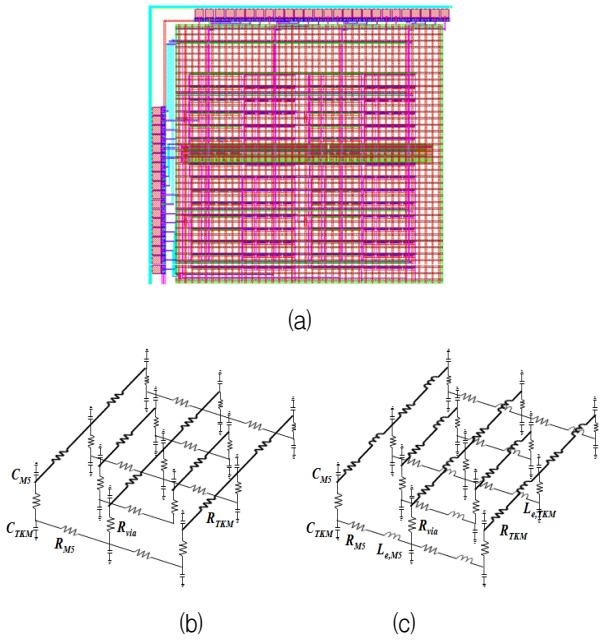


그림 6. 온칩 전력 격자 구조 모델: (a) 레이아웃 디자인, (b) RC 추출 회로, (c) 인덕턴스 추출 tool로부터 재구성된 RLC 추출 회로

Fig. 6. Model of the on-chip power grid: (a) layout design, (b) RC extraction circuit, (c) RLC extraction circuit reconstructed by the inductance extraction tool.

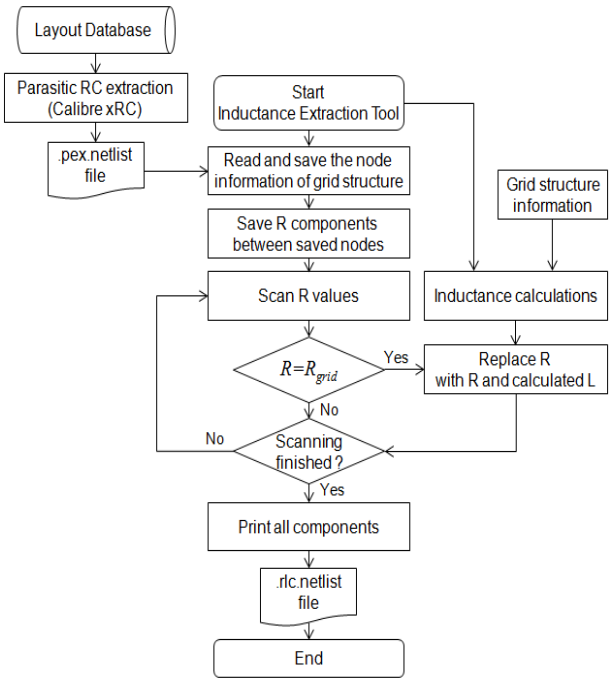


그림 7. 제안된 loop 인덕턴스 모델을 사용한 인덕턴스 extraction flow

Fig. 7. Inductance extraction flow using the proposed loop inductance model.

metal layers. The resistances and capacitances between M5 and TKM have different values because the thicknesses of those, t_{M5} and t_{TKM}, are different. If we include the inductance model in the power/ground netlist, then the RLC netlist will be as shown in Fig. 6(c). The effective inductances calculated from our proposed model between M5 and TKM are different due to the metal thicknesses.

Figure 7 describes the inductance extraction flow of the developed tool based on the proposed loop inductance model. The inputs are the layout-based RC extraction file (.pex.netlist) and the grid structure information such as the sizes of on-chip grid structures. The current version of the tool is based on the Calibre output format, but it can be easily modified to take input from layout extraction tools from other CAD vendors. The proposed inductance model can be applied in 'Inductance calculations' step to calculate inductance values. The output of the tool is a RLC netlist file (.rlc.netlist) that includes the SPICE netlist as shown in Fig. 6(c). It can be used for HSPICE simulation.

Ⅲ. Proposed Model Validation and Applications to Chip Layout

1. Proposed inductance model validation

The proposed inductance loop model was validated by comparing it with the PEEC model using HSPICE simulation. It was performed with RLC circuits extracted from the layout design of grid structures without transistors. Table 1 shows two cases of the grid structures used for model validation.

표 1. 모델 검증을 위한 grid 구조의 2 가지 case
Table 1. Two cases of the grid structures used for model validation.

	Number of metal lines, n	Width, w (um)	Distance, d (um)	Length, l (um)
Case 1 (20x20)	40	10	50	50
Case 2 (30x30)	60	4	30	30

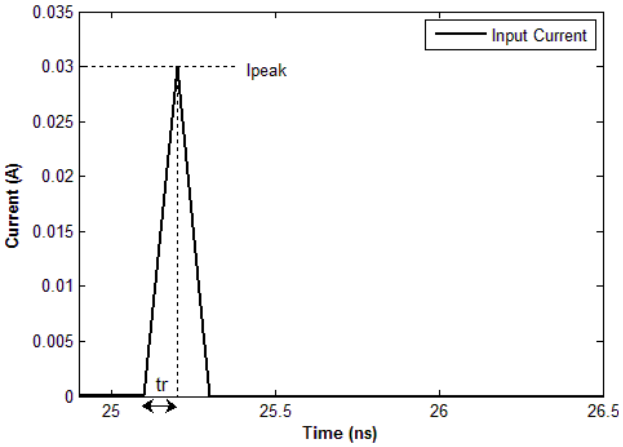
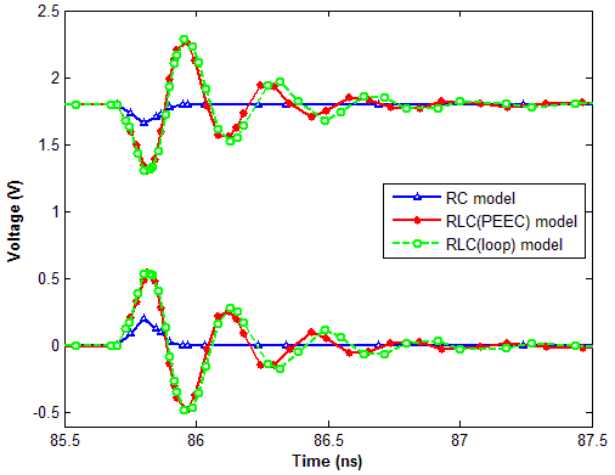
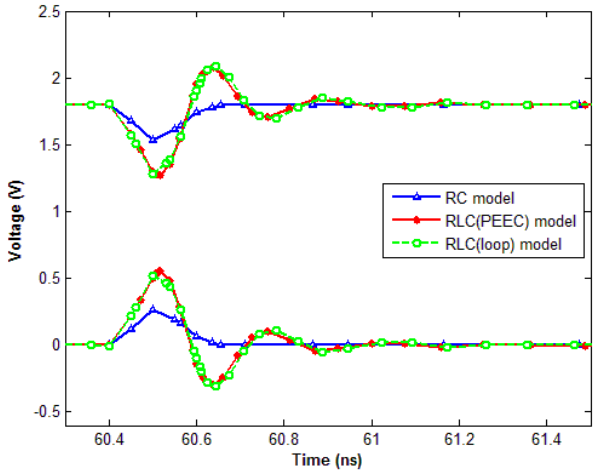


그림 8. Simulation을 위한 입력 전류원
Fig. 8. Input current source used for simulation.

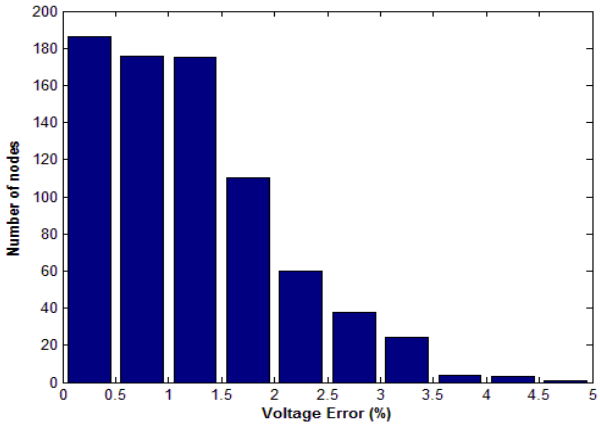


(a)

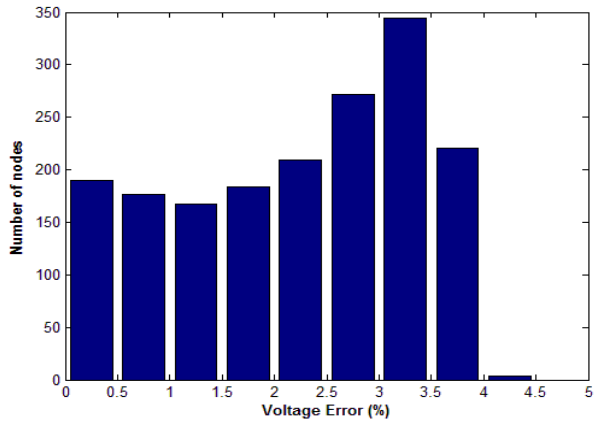


(b)

그림 9. PEEC model과 loop model을 비교하기 위한 전압 변동 plot (a) case 1 (b) case 2
Fig. 9. Voltage fluctuation plot for comparison between PEEC and the proposed loop model: (a) case 1, (b) case 2.



(a)



(b)

그림 10. 제안된 loop 모델과 PEEC 모델의 오차율: (a) case 1, (b) case 2

Fig. 10. Voltage errors between the proposed loop model and the PEEC model: (a) case 1, (b) case 2.

To simulate conditions such as switching currents caused by switching gates in power distribution networks, the input current source, as shown in Fig. 8, was used where tr is the rising/falling time (0.1 ns) and I_{peak} is the peak current value (0.03 A) of the triangular source. Nine current sources were randomly located between the power and ground lines.

The simulation results are shown in Fig. 9. In both cases, the power and ground voltage fluctuation are larger in the RLC model compared to those in the RC model. The voltage ringing that appeared in the RLC model is due to on-chip inductance effects. The results of the proposed effective loop inductance model and those of the PEEC model match well.

To compare the accuracy of the proposed model versus the PEEC model, voltage errors can be calculated as follows, where V_{pp} is the peak-to-peak voltage:

$$Error(\%) = \left| \frac{V_{pp,loop} - V_{pp,PEEC}}{V_{pp,PEEC}} \right| \times 100 \qquad (8)$$

The grid structure of case 1 (20x20) and case 2 (30x30) have a total of 800 nodes and 1800 nodes, respectively. The peak-to-peak voltage of all nodes was measured and the % errors were calculated using (8). The voltage errors of case 1 and case 2 are shown in Fig. 10. Both cases had errors under 5 %. The average error of case 1 was 1.2 % and that of case 2 was 2.2 %.

The simulation memory usage and execution time between the loop model and the PEEC model are compared in Table 2. The memory usage of the proposed loop model was an average of 1.2 times smaller than that of the PEEC model, and the execution time of the proposed loop model was more than 4 times faster than that of the PEEC model. This proves that the proposed loop inductance model provides a simpler model and faster simulation time.

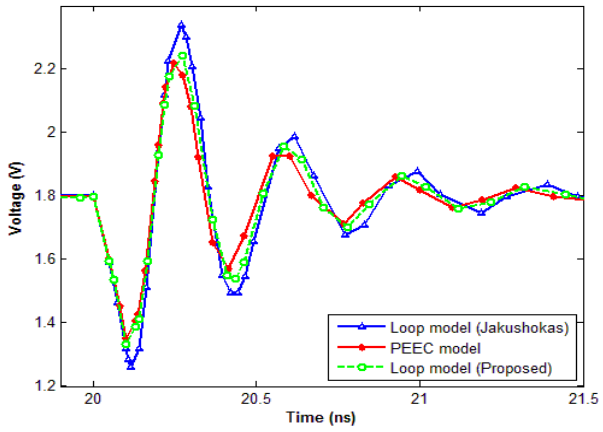
The accuracy of the proposed loop inductance model is compared with the loop inductance model for interdigitated power grid structures developed by *Jakushokas*[9]. The *Jakushokas* model is based on the effective inductance calculation considering only one pair of power and ground lines, then expanding the formula for N pairs. In deriving the model, the length

표 2. Loop 모델과 PEEC 모델 비교

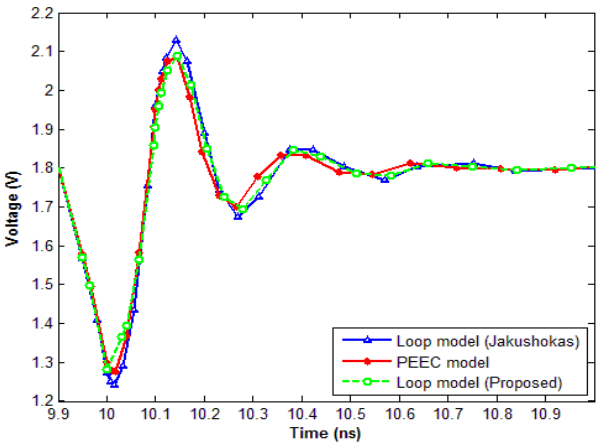
Table 2. Comparison between the loop model and the PEEC model.

	Case 1		Case 2	
	Proposed loop model	PEEC model	Proposed loop model	PEEC model
Simulation memory usage (KBytes)	6060	7154	13545	16556
Simulation execution time (sec)	171.16	1113.53	260.37	1239.42

of grid metal lines is assumed to be much longer than the distance between them, and the converging value for the infinite series is calculated. In Fig. 11, the VDD fluctuation predicted by the PEEC model, the proposed loop model, and the *Jakushokas* model are compared. The *Jakushokas* model overestimates the voltage fluctuation compared to our proposed model.



(a)



(b)

그림 11. 세 model을 비교하기 위한 VDD 전압 변동 plot: (a) case 1, (b) case 2
Fig. 11. VDD voltage fluctuation comparison among three models: (a) case 1, (b) case 2.

표 3. 평균 오차율 비교
Table 3. Comparison of average errors.

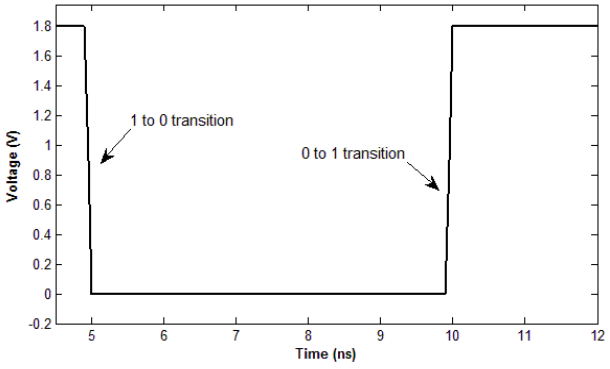
Average Error (%)	Loop model (Proposed)	Loop model (*Jakushokas*)
Case 1	1.2 %	6.5 %
Case 2	2.2 %	6.7 %

In Table 3, the average errors calculated by Equation (8) are shown. In case of the *Jakushokas* model, the average error of case 1 was 6.5 % and that of case 2 was 6.7 %. The results prove that the proposed loop model is more accurate than the *Jakushokas* loop model using the PEEC model as a reference.

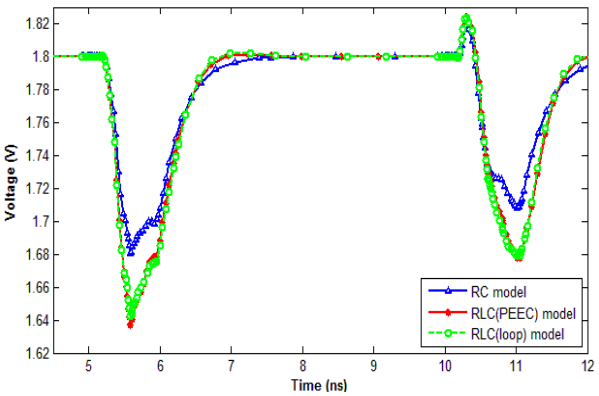
2. Application of the proposed inductance model to chip layout

The inductance extraction tool developed in this work can be applied to the chip layout shown in Fig. 6. The RLC circuits are extracted from the layout of the 20x20 power/ground grid structure and transistors of several circuits such as I/O buffers.

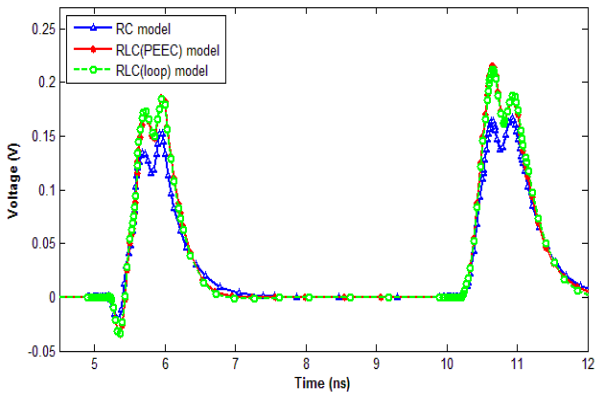
The simulated VDD and VSS noise results generated from the extracted RLC circuits are shown in Fig. 12. Fig. 12(a) shows the input clock of I/O buffers that make switching noises at each clock



(a)



(b)



(c)

그림 12. Chip layout에서 추출된 RLC circuit의 시뮬레이션 결과: (a) I/O 버퍼의 입력 클락, (b) 격자 구조의 power (VDD), (c) 격자 구조의 gound (VSS)

Fig. 12. Simulation results of the RLC circuit extracted by chip layout: (a) Input clock of I/O buffer, (b) Power (VDD) of grid structure, (c) Ground (VSS) of grid structure.

transition point[12]. Fig. 12(b)-(c) shows the voltage fluctuation on power distribution grids that occurs due to switching noises. Compared to the voltage fluctuation shown in Fig. 9, voltage ringing caused by additional device capacitors included in the extraction did not happen in this post-layout simulation. In these cases, the peak-to-peak voltage fluctuation of the RC model was also smaller than that of the RLC model and the proposed loop model results were well fit to the PEEC model results.

Ⅳ. Chip-Package-Board Co-simulation

Using the RLC extraction netlist generated by our developed tool from the chip layout in Section III-2, it is possible to perform chip-package-PCB co-simulation. As the off-chip inductances such as those of PKG and PCB are also significant[7], it is necessary to analyze the significance of the on-chip inductance effects through co-simulation considering a variety of chip test environments. The equivalent circuit of chip-PKG-PCB is described in Fig. 13.

The model of the PCB PDN (power distribution

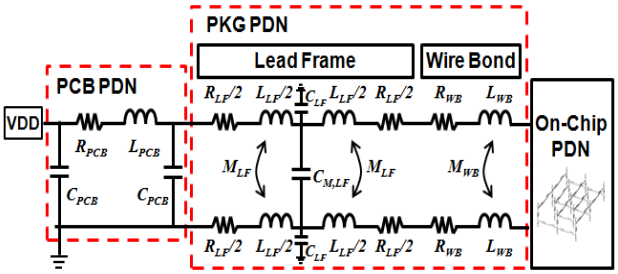


그림 13. 칩-패키지-PCB 등가 회로 모델

Fig. 13. Equivalent circuit of chip-PKG-PCB.

표 4. Metal line 길이에 따른 PCB 모델

Table 4. PCB models of different metal lines.

	R_{PCB} (Ω)	L_{PCB} (nH)	C_{PCB} (pF)
PCB Model A	0.01	1.25	4.52
PCB Model B	0.03	3.74	13.6

network) was calculated by the formulae from [13] as in (9), where w is width (1 cm), t is thickness (17 um), l is the length of metal lines and h is height (110 um) between the metal lines and the ground plane of the PCB. In Table 4, two different PCB models having two different trace lengths, l, are defined. We assume that the length of PCB model A is 0.01 m and that of PCB model B is 0.03 m.

$$R_{PCB}=\frac{\rho\cdot l}{w\cdot t},\quad L_{PCB}=\frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{8h}{w+t}+1\right)\right],$$
$$C_{PCB}=\varepsilon_0\varepsilon_r l\left[1.13\left(\frac{w}{h}\right)+1.44\left(\frac{w}{h}\right)^{0.11}+1.46\left(\frac{t}{h}\right)^{0.42}\right]. \quad (9)$$

The models of PKG PDN referenced by [14] are shown in Table 5 and the on-chip PDN is an on-chip parasitic RC and RLC extraction circuits

표 5. 3개의 다른 패키지 모델

Table 5. Three different package models.

	Lead Frame					Wire Bond		
	R_{LF} (Ω)	L_{LF} (nH)	M_{LF} (nH)	C_{LF} (pF)	$C_{M,LF}$ (pF)	R_{WB} (Ω)	L_{WB} (nH)	M_{WB} (nH)
Model 1 (QFP)	0.8	2.4	1.4	0.05	0.2	0.2	2.57	1.46
Model 2 (BGA)	0.2	0.9	0.3	0.04	0.1	0.1	1.09	0.55
Model 3 (CSP)	0.03	0.4	0.1	0.08	0.07	0.1	0.78	0.39

from the chip layout.

To analyze the effects of on-chip inductances on the impedance of the whole PDN impedance, the self impedance at the VDD node in Fig. 13 is examined. The self impedance in terms of different PCB models are shown in Fig. 14. At higher frequencies over 1 GHz, each resonance point in each PCB model with on-chip RLC circuits move to the left compared with on-chip RC circuits due to additional on-chip inductances. The resonance frequencies are larger for model A than for model B due to the smaller PCB inductances and capacitances. The larger PCB

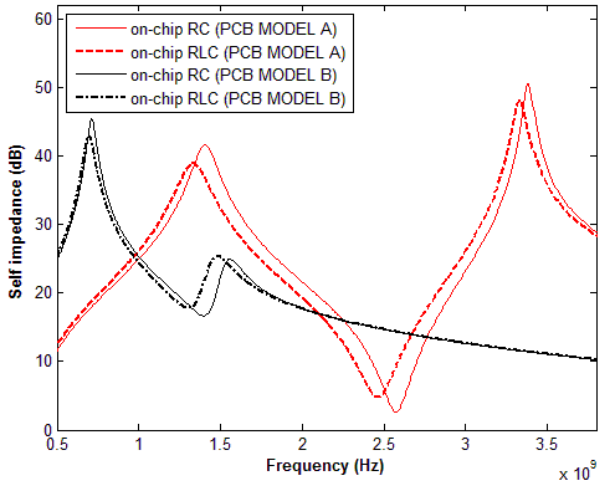


그림 14. Off-chip/on-chip PDN을 포함한 셀프 임피던스
Fig. 14. Self impedance including off-chip/on-chip PDN.

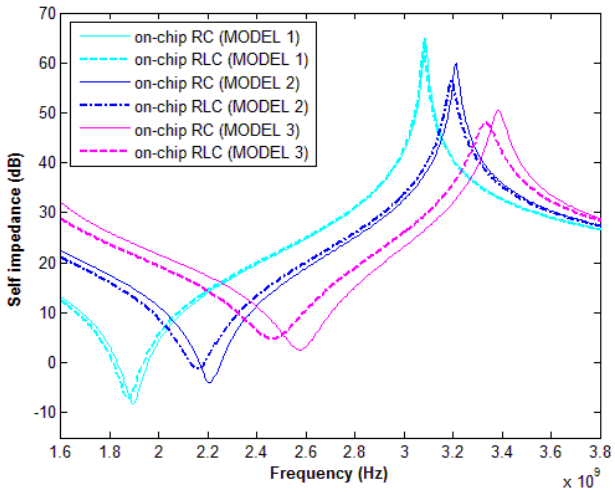


그림 15. Package model의 차이에 따른 Self impedance
Fig. 15. Self impedance in terms of the difference in package models.

inductance makes smaller the effects of the chip-PKG as the PCB components are dominant at low frequency. However, as the PCB inductance decreases due to shorter traces on board, the chip-PKG model will be dominant, and the on-chip inductance effects increase at high frequency.

In Fig. 15, the self impedance in terms of different PKG models are shown. As the PKG inductance decreases from model 1 to model 3, the resonance points move to the right and the on-chip inductance effects increase. For these reasons, the on-chip inductance effects are important at high frequencies because of the miniaturization of test systems including PKG and PCB. In high speed chips, the high frequency components of the switching noises will affect the power integrity of on-chip power distribution grids.

Ⅴ. Conclusion

An effective loop inductance model for power grid structures was proposed in this paper. The power grid RLC netlist generation flow and tool based on the proposed inductance model were developed.

The accuracy of the proposed model was verified by comparing the proposed loop model to the PEEC model using HSPICE simulation. The average errors were under 2%. Circuit simulation time and memory usage were reduced significantly when the proposed model was used.

The developed inductance extraction tool can be applied to layout-based RLC extraction using the proposed loop inductance model. The peak-to-peak voltage fluctuation of the RLC circuits was larger than that of the RC circuits due to on-chip inductance effects. The difference in voltage fluctuation between the RC and RLC circuits from layout-based extraction was not significant because device capacitors act as decoupling capacitors. However, the voltage fluctuation due to on-chip inductances can be a problem in the lower supply

voltages with advanced technologies.

The significance of on-chip inductance effects was investigated through the co-simulation of chip-PKG-PCB including post-layout RLC extraction circuits. The smaller inductances of PCB and PKG due to miniaturization made the on-chip inductance effects more significant. As the switching speed increases in high-speed circuits, post-layout RLC simulations are encouraged for the power integrity analysis of on-chip power distribution grids. The proposed inductance model and extraction tool will be beneficial in performing co-simulation of the real chip environment considering on-chip inductances.

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