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Maritime radar display unit based on PC for safe ship navigation

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Abstract

A prototype radar display unit was implemented using inexpensive off-the-shelf components, including a nonlinear estimation algorithm for the target tracking in a clutter environment. Two custom designed boards; an analog signal processing board and a DSP board, can be plugged into an expansion slot of a personal computer (PC) to form a maritime radar display unit. Our system provided all the functionality specified in the International Maritime Organization (IMO) resolution A422(XI). The analog signal processing board was used for A/D conversion as well as rain and sea clutter suppression. The main functions of the DSP board were scan conversion and video overlay operations. A host PC was used to run the tracking algorithm of targets in clutter, using the discrete-time Bayes optimal (nonlinear, and non-Gaussian) estimation method, and the graphic user interface (GUI) software for Automatic Radar Plotting Aid (ARPA). The proposed tracking method recursively found the entire probability density function of the target position and velocity by converting into linear convolution operations.

Keywords: Radar; DSP; Personal Computer (PC); Discrete-time Bayes optimal estimation; Graphic user interface (GUI); Automatic Radar Plotting Aid (ARPA)

1. Introduction

Maritime radars play a vital role in ship navigation and collision avoidance. Typical maritime radar is a track-while-scan (TWS) radar, composed of three units: a slotted waveguide antenna unit, a transmitter/receiver unit, which deals with RF and IF signals, and a display unit, where major signal and data processing take place. Our display unit was tested with a commercial TWS radar, with an 8 ft slotted waveguide antenna, operating at a frequency of 9 GHz (X-band) (which is down-converted once to 60 MHz IF). This particular radar had three different transmitting pulse length/PRF's (Pulse Repetition Frequencies), as shown in Fig. 1.

A photograph of the radar display unit is shown in Fig 2. The functionality of our display unit can be conveniently dissected into four blocks (see Fig. 3): (1) the analog signal processing block for Sensitivity Time Control (STC) and Fast Time Constant (FTC) operations, and for A/D conversion, (2) ADSP 21060 SHARC chip (and surrounding circuitry) for data processing and PC interface, (3) RAMDAC and overlay controller block, and finally (4) the PC, which is in charge of the multi-target tracking, and runs the software for the mouse and key-board event processing [1].

Pulse Type	Pulse Length(㎲)/PRF(㎐) nominal
Short Pulse	0.05/1200
Medium Pulse	0.25/1200
Long Pulse	1.00/600

Fig. 1. Transmitting pulse length/PRF's.

Here we shall first take a closer look at the operations in the DSP chip and the host PC. Various operations in these two blocks are performed in parallel, and their outputs (video and VGA) are combined at

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the final stage by an overlay chip (see [2] for a different approach). The PC and DSP chip communicate with each other through the dual port RAM, on which detects and track-related information are periodically read and written. Fig. 4 shows the flowcharts of the operations executed by the host PC and DSP chip.

The host PC offers a Graphic User Interface (GUI) environment so that the operator can interactively communicate with the system via the keyboard and mouse (see Fig. 4(a)). If the operator designates a target among many detects in the radar scope using a click of mouse, during the next scan period the DSP chip supplies the PC with the near by validated detects so that the target tracking filter (see Sec. 4.2) can be initialized. After selecting "the best" detects out of those validated (i.e. after associating a detect with each track) the host PC can obtain the filtered estimate of target's position and velocity. During the next scan period, the host PC sends the predicted estimate of the target's position and velocity to the DSP chip, and another cycle begins. The tracker in the clutter environment (sea and rain etc.) proposed in this paper was based on the Bayes optimal estimation theory [3, 4], which recursively finds the conditional probability density function (conditioned on the entire measurement history) of the position and velocity of the target. With multiple detects at each sampling time, the obtained conditional probability density functions would initially have several Gaussian-shaped peaks at the locations of the clutter points as well as at the target.

Fig.4(b) illustrates the sequence of operations that take placed in the DSP chip, including averaging, scan conversion, Stationary Track Filter (STF), detect validation and host PC interface. This sequence of operations was repeated at the beginning of every Pulse repetition time (PRT) [5].

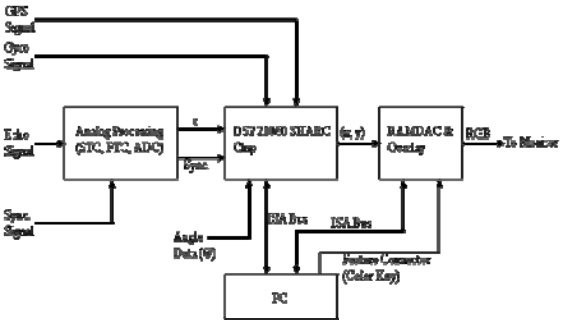
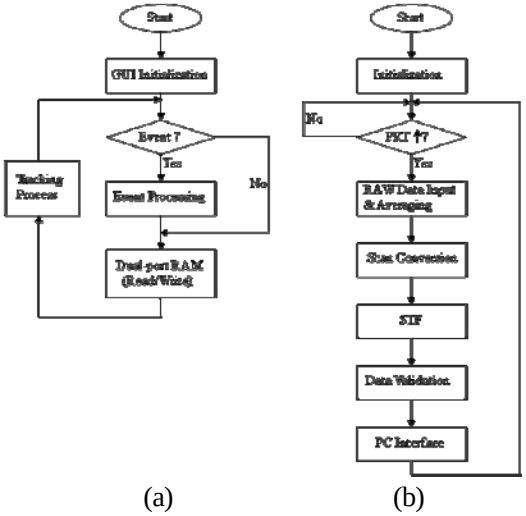


Fig. 3. Overall block diagram.



(a) (b)

Fig. 4. Flow charts for PC and DSP.

2. Analog signal processing

A photograph of our analog signal processing board is shown in Fig. 5. The analog signal processing board performs the clutter rejection operation, A/D conversion and trigger generation (see Fig. 6).

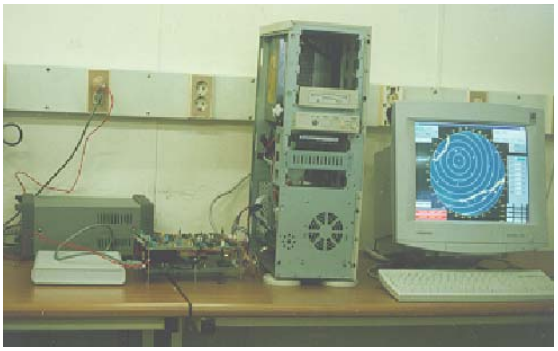


Fig. 2. Photography of the prototype system.

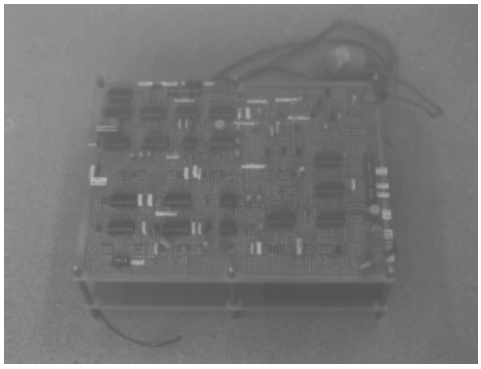


Fig. 5. The Analog Signal Processing board.

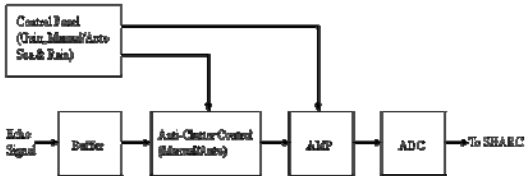
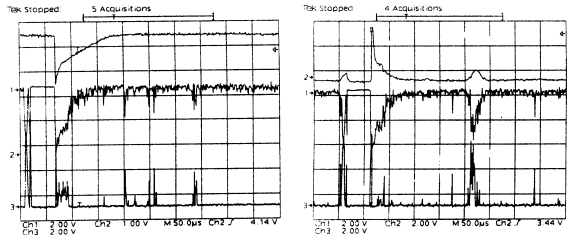


Fig. 6. Analog Processing block diagram.

The purpose of the clutter rejection operation was to reduce the clutter points appearing on the radar scope, which are caused by the echo signals reflected from the sea surface and rain drops. The STC circuit rejected the sea clutter and the FTC circuit rejected the rain clutter. These anti-clutter operations can be performed either manually or automatically. Test results under the two different modes were recorded with our board using an oscilloscope, which are shown in Fig. 7.



(a) (b)

Fig. 7. (a)Manual Anti-Clutter Mode. (b) Auto Anti-Clutter Mode.

The A/D converter sampled the returned echo at a rate of 10 MHz, with 4 bit-quantization accuracy. Fig. 8 shows the output of the A/D converter that appeared on the oscilloscope (only three MSB's are shown here).

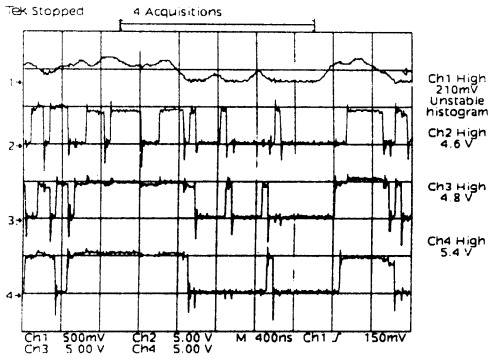


Fig. 8. Measurement of the ADC output.

3. Signal processing in the DSP board

A simulation program was developed using the proposed sampled echo data obtained from the analog signal processing block via a sequence of processes in the DSP board, including averaging, scan conversion, STF, thresholding and measurement validation. The photograph of the DSP board is shown in Fig. 9.

Fig.10 illustrates the functional block diagram of the digital signal processing in the DSP board.

Fig. 9. The DSP board.

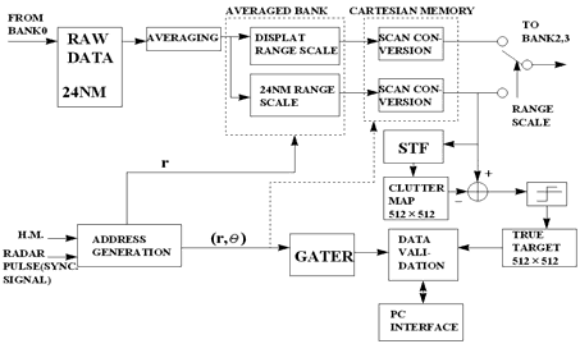


Fig. 10. Functional Block Diagram.

The timing diagram is shown in Fig 11. Note: the duration of the Heading Mark (HM), i.e. one scan period of the antenna, spans 120 vertical sync pulses of the monitor. One scan period (2 sec) also corresponded to 2400 PRTs in the case of 1200Hz PRF (see Fig.1). During one PRT period, the antenna rotated 0.15 degree, with 3384 echo data obtained because the sampling frequency was 10 MHz.

The ADSP 21060 SHARC DSP chip had 4 Mega bits of internal SRAM which can be used to store programs and data. The instruction rate of the chip was 40 MIPS (25 ns). Input data to the DSP chip were the Heading Mark (HM) of the own-ship (standard NMEA 0183), which was obtained from the Global Positioning Satellite System (GPS), the gyro compass signal, the synchronization pulses, indicating the leading edges of each transmitted radar pulse (trigger pulse), digitized radar echo signal and the azimuth angle stepping pulses.

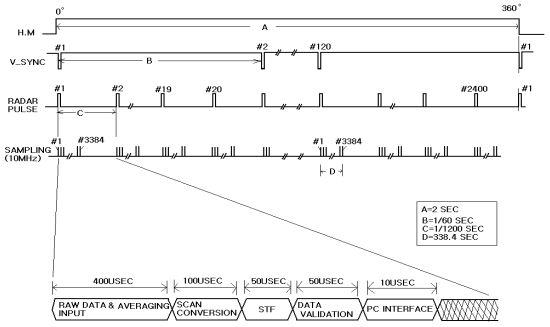


Fig.11. Timing diagram.

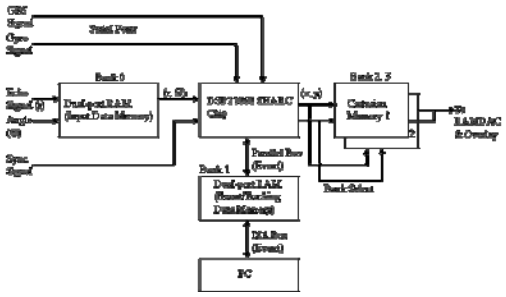


Fig. 12. Data Processing and PC interface.

The block diagram that implemented the functions shown in Fig. 10 is shown in Fig. 12.

The DSP chip performed operations, such as communication between the host PC and the DSP board, detection of targets under noise, scan-conversion for the rasterized display, averaging of the nearby pixel values to match the resolution of the image to that of the monitor.

The host PC and the DSP board communicated with each other through an ISA bus, using the I/O mapped I/O. A dual-port RAM (Bank 1) was also used as a buffer to prevent the loss of data. The DSP chip handled some of the events generated by a keyboard or mouse attached to the host PC, and also provided information to show the Automatic Radar Plotting Aids (ARPA) [5] information on the monitor.

Bank 0 dual-port Ram (bank0) was used as the retiming buffer memory. The role of this memory was to alleviate the load of the DSP chip under a heavy data stream from the analog signal processing board (4bits 10 MHz).

Unlike the more traditional Plan Position Indicator (PPI) display, our rasterized displays requires scan conversion. Namely, the detect locations represented in the polar coordinate must be converted to Cartesian coordinate, for which two Cartesian memories were used. The functions in Fig. 10 are explained in more detail in the following sections.

3.1 Initialization

The initialization routine sets up the necessary system environments, including the writing of the blue background image on Banks 2 and 3, which will ultimately be displayed on the radar scope, and the initialization of the V-Sync interrupt service routine. The occurrence of this interrupt initiates a sequence of tasks; sampling of echo data inputting, averaging, scan conversion, STF, data association and the PC interfacing. The final results were alternately written to Banks 2 and 3.

3.2 Averaging

An operator can choose one of the six different range scales from 0.75NM (Nautical Miles) to 24.0NM, with a mouse click. The total number of echo samples for each different range scale is shown in Fig. 13.

Range(NM)	# of sample	Range(NM)	# of sample
0.75	105	6.00	846
1.50	211	12.00	1692
3.00	423	24.00	3384

Fig. 13. Number of sample by range.

Our system had a VRAM (Video RAM) frame buffer size of 512-by-512; consequently, the radar scope on the monitor had a diameter of 512 pixels. Because the radius of the scope was able to accommodate only 256 pixels, some samples were decimated or averaged for the range scales beyond 1.50NM. Although the display range scale can vary from PRT to PRT, it is should be noted that it was necessary to perform the tracking (including the STF and data association) with the 24NM range scale data. Therefore, two averages; one for the display and the other for tracking were needed. To be able to instantly change the display range scale, the chained averaging scheme was used, which simultaneously gave the sets of averaged samples for all range scales.

Fig 14 shows the chained averaging scheme, which was composed of 1/2 and 1/1.65 averages. The former can be achieved simply by taking the mean of two consecutive samples, while the latter has to be performed in two phases; 1/1.5 averaging followed by the deletion of every 11th sample (see Fig. 14).

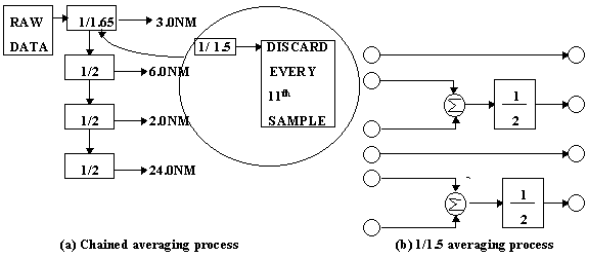


Fig. 14. Chained averaging scheme.

Referring to Fig. 10, note both the 24NM range scale data (for tracking) and current display range scale data were separately and simultaneously stored in the averaged banks, which had 256 address spaces.

3.3 Scan conversion

The target location measured by the radar was in polar coordinates, which should be converted to Cartesian coordinates to be displayed on the radar scope and track targets using the proposed tracker.

The two sets of 256 samples obtained from the previous averaging method were then ready for the scan conversion. Note: the addresses of the averaged banks can be regarded as range bins. Also, recalling that one PRT corresponds to a bearing of 0.15 degrees (in the case of 1200Hz PRF), the transformation formula can be written as:

$$x = r\cos\Theta$$
$$y = r\sin\Theta$$
$$\Theta = \text{Number of PRF's} \times 0.15$$

where r is the address (1- 256) of the sample. Note: two scan conversions were needed for the data sets corresponding to the current display range scale and the 24 NM range scale. Scan converted data for the current display range scale were written to memory Banks 2 and 3 (see Fig. 12), while the data for the 24 NM range scale were sent to the STF.

3.4 Stationary track filter (STF)

The STF acted as a velocity discriminator for the scan converted detect stream. Detects that appeared to be stationary or slowly moving from scan to scan were stored in the clutter map. The STF was made of a 1st degree IIR filter as shown in Fig. 15.

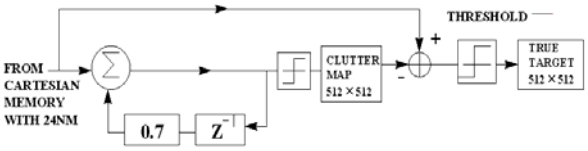


Fig. 15. Stationary Tracking Filter.

Each new incoming detect was compared with the content of the clutter map. An appropriate threshold should be chosen by considering the nominal speed of the targets under consideration. The threshold can vary from PRT to PRT.

3.5 Detection and measurement validation

Measurements were detected using the threshold corresponding to the Constant False Alarm Rate (CFAR). The detects were then validated using a rough rectangular gate, whose diameter was three times longer than the distance for which the fastest target could travel during one scan period (2 sec). Validated detects were sent to the host PC.

4. Operation in the PC

If the operator designates a detect on the radar scope as a target using a mouse, a tentative track is formed. If there are nine consecutive scans, all with validated detects, then the tentative track becomes the firm track, as shown in Fig. 16.

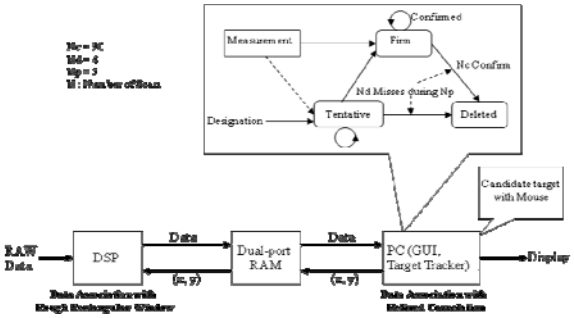


Fig. 16. Tracking and Data Association.

A tentative track or a firm track was deleted if there were four scans, but with no validated detects out of five scans. A tentative track was also formed automatically (without the mouse clicking) if a detect entered the guard zone. For each firm tracks, information, such as Closest Point of Approach (CPA), Time to the Closest Point of Approach (TCPA), target speed, were available on request.

4.1 Data association

If the host PC sends the predicted target state of a track to the DSP chip, via the dual-port RAM, the DSP chip sets a rough validation gate around the target state (see Sec. 3.5). If detects were present in the rough validation gate, the validated detects were sent back to the host PC via the dual-port RAM. The, PC then set a more refined validation gate for them, and chose "the best" detect, which was then used for the measurement update. The size of the refined gate was two times longer than the distance for which the fastest target could travel during one scan period for tentative tracks, but 1.5 times for firm tracks.

4.2 Tracking algorithm

Target motion on a radar scope can be described using the four-dimensional state space model [3]

$$\begin{matrix} s_{k+1} = Fs_k + G\tilde{w}_k, \\ z_k = \tilde{h}(s_k) + u_k, \end{matrix} \quad F = \begin{bmatrix} I & \Delta I \\ \mathrm{O} & I \end{bmatrix}, \; G = \begin{bmatrix} (\Delta^2/2)I & \Delta I \end{bmatrix}^T, \tag{1}$$

where the state $s_k \equiv [x_k, y_k, v_{x,k}, v_{y,k}]^T$ represents the position and velocity of the target, $z_k \equiv [z_{1,k}, z_{2,k}]^T$ are detects, $\tilde{w}_k$ the white Gaussian process noise, u_k the white Gaussian measurement noise, I the 2×2 identity matrix, and Δ the sampling interval. Our radar display unit, had nonlinear measurements. $z_{1,k} = (x_k^2 + y_k^2)^{1/2} + u_{1,k}$ and $z_{2,k} = \tan^{-1}(y_k / x_k) + u_{2,k}$.

At time k, there were m_k detects, $Z_k \equiv [z_k^{(1)}, z_k^{(2)}, \cdots, z_k^{(m_k)}]^T$, Each $z_k^{(i)}$ could be the true target originated detect, with a probability $P\{z_k = z_k^{(i)}\} = P_D / m_k$, where P_D is the probability of detection. If the cumulative set $Z^{(k)}$ of detects is defined by $Z^{(k)} \equiv [Z_1, Z_2, \cdots, Z_k]^T \in R^{2\times(\sum_{i=1}^{k} m_i)}$, the predicted probability density of the state, $p(x_{k+1} \mid Z^{(k)})$ and the filtered probability density of the state, $p(x_{k+1} \mid Z^{(k+1)})$ can then be obtained recursively starting from $p(x_0) \equiv p(x_k \mid Z^{(k)})$ as shown below.

If the densities $p(x_{k+1} \mid Z^{(k)})$ and $p_{d_k}(x_k)$ are known; then, because x_{k+1} is the sum of three independent random variables, the time-update recursion can be obtained:

$$f_{k+1}^{p} = f_k^{f} \otimes p_{d_k} \otimes p_{w_k}, \tag{2}$$

where $f_{k+1}^{p}(x_{k+1}) \equiv p(x_{k+1} \mid Z^{(k)})$, $f_k^{f}(x_k) \equiv p(x_k \mid Z^{(k)})$, and "⊗" denote the two-dimensional convolution operation.

To obtain the measurement-update recursion, the following first need to be defined

$\theta_{k+1}^{(i)} =$ the event that $z_{k+1}^{(i)}$ is the target-originated detect, $1 \le i \le m_{k+1}$,

$\theta_{k+1}^{(0)} =$ the event that none of the detects is target-originated.

Now, repeatedly using the Bayes' formula, the identity is obtained [6],

$$p(x_{k+1} \mid Z^{(k+1)}) = \frac{1}{c} \cdot p(Z_{k+1} \mid x_{k+1}) \cdot p(x_{k+1} \mid Z^{(k)}), \tag{3}$$

where $p(Z_{k+1} \mid x_{k+1})$ can be obtained by:

$$\begin{aligned} p(Z_{k+1} \mid x_{k+1}) &= \sum_{i=0}^{m_{k+1}} p(Z_{k+1} \mid x_{k+1}, \theta_{k+1}^{(i)}) P\{\theta_{k+1}^{(i)}\}, \\ &= \left\{ \sum_{i=1}^{m_{k+1}} p_{u_{k+1}}(z_{k+1}^{(i)} - h(x_{k+1})) \cdot \frac{P_D}{m_{k+1}} \right\} + (1 - P_D) \end{aligned} \tag{4}$$

The term inside the curly brackets in (5) represents the sum of m_{k+1} Gaussian functions when *h* is linear, and the sum of skewed Gaussian functions when *h* is nonlinear.

The density function, p_{d_k}, required in (3) can be estimated using two consecutive filtered probability densities, by noting $\hat{d}_k = x_k - x_{k-1}$, so that:

$$\hat{p}_{d_k} = f_k^{f} \otimes g_{k-1} \tag{5}$$

where $g_{k-1} \equiv p(-x_{k-1} \mid Z^{(k-1)})$.

When there was a stationary clutter point, the stationary point obeyed model (1) even more faithfully than the moving target and; therefore, the density functions of the state obtained as above may build on the stationary clutter point, and not track the moving target. If the target is moving, the stationary clutter points can be rejected using two techniques; velocity gating and density limiting. The resulting tracker then becomes a moving target indicator (MTI). The first forces $\hat{p}_{d_k}$ to become zero near the origin (i.e. $\hat{p}_{d_k}(x) = 0$, for ||x|| ≤ R), before $\hat{p}_{d_k}$ convolves with the filtered density function in (3). This technique helps the peak of the predicted density to not dwell on the stationary clutter point. With density limiting, the

value of the filtered density function was trimmed off below a certain threshold, so that the probability mass was not dominated by a single detect. This also helped the tracker to be responsive to a newly appeared target.

4.3 GUI software

The International Maritime Organization (IMO) issued the ARPA specification for the safe navigation and collision avoidance of merchant vessels. The purpose of this specification was to (1) reduce the workload of operators by enabling them to automatically obtain information on multiple targets, and (2) provide continuous, accurate and rapid evaluation of changing situations.

The host PC runs the Windows XP operating system, and for each designated target the radar display unit gives the following ARPA information:
(1) filtered ranges and bearings to the target,
(2) predicted target ranges to the closest point of approach (CPA),
(3) estimated time to CPA (TCPA),
(4) true course and speed of the targets.

The GUI software is written using Microsoft Visual Basic 4.0, and some of its functions are:
(1) EBLs (electric bearing lines) drawing,
(2) VRMs (variable range markers) drawing,
(3) range scaling (maximum displayable ranges between 0.75 NM and 24.0 NM),
(4) range-off function which moves the center of the radar scope,
(5) guard zones drawing,
(6) target designation function using the mouse,
(7) detection threshold control for reduction of rain and sea clutter.

The typical monitor screen of the display unit is show in Fig. 17.

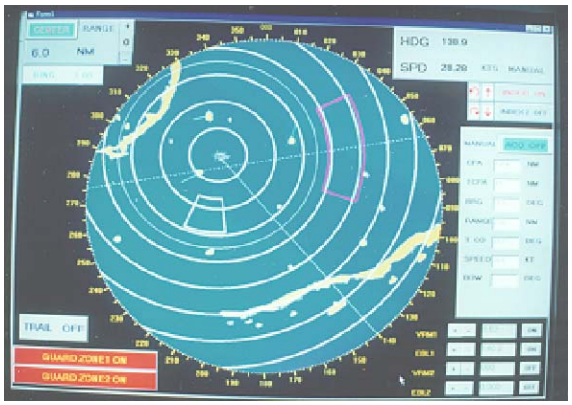


Fig. 17. Screen of the Radar Display Unit.

5. RAMDAC and overlay controller

This RAMDAC and overlay controller resides in the DSP board. The role of this part was to display the processed data and GUI panel in the monitor screen in a well coordinated way.

Our system used the MVP 133A1 chip [7] as an overlay controller and the 74HC4053 chip as an analog multiplexer, and Bt121 as the VideoDac, which converts the 16 bit digital data (R:5bits, G:6bits, B:5bits) to an RGB signal. Fig. 18 shows the block diagram of the RAMDAC and overlay controller.
The MVP 133A1 chip supports the color key (VGA Chroma key) function and was used to overlay video data (radar scope) on the VGA graphics data (GUI). An MVP 133A1 receives timing signal and color key data from the feature connector on the VGA card, and allows the

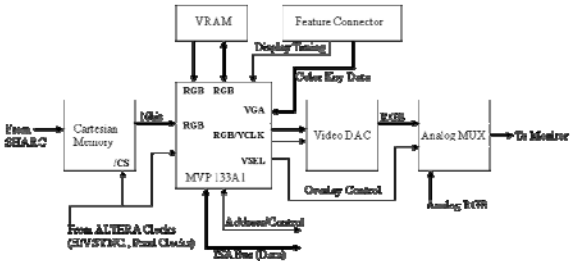


Fig. 18. Block diagram of the RAMDAC and the Overlay Controller.

VSEL(Video Select) clock to choose between the video data and the analog RGB from the PC. An MVP 133A1 chip also transmits RGB formatted digital data to the video DAC. Video memory (VRAM) with the size 2×256K×8 was used to store images of size 512-by-512. In graphic controller applications, the serial shift register port of the VRAM was generally the path via which the screen refreshed data flows, which allowed practically unrestricted access of the host CPU into the frame buffer memory.

6. Conclusions

A cost-effective hardware design for a maritime radar display unit, using the discrete-time Bayes optimal (nonlinear, and non-Gaussian) estimation method, has been suggested. The system was composed of two custom-designed boards, and an industrial Pentium PC. Our unit was able to track up to thirty targets, and provided ARPA functionality.

Acknowledgments

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